

FEATURES

- Monolithic CMOS Construction
- Full Four-Quadrant Multiplication
- Excellent Stability Over Temperature and Time
- TTL/5 V CMOS Compatible
- Guaranteed Monotonic

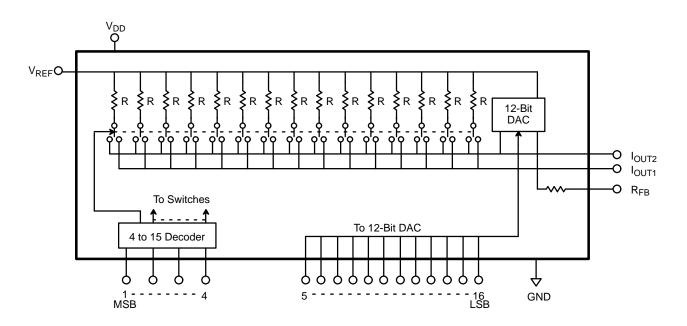
- Low Sensitivity to Output Amplifier Vos
- Low Glitch Energy
- Buffered Version: MP7626
- 5 V Version: MP7616B

GENERAL DESCRIPTION

The MP7616 is a high density 16-bit CMOS multiplying Digital-to-Analog Converter. Silicon nitride passivation and untrimmed silicon chromium resistors have been combined to provide long term stability and reliability. Using the most significant bit (MSB) segmentation technique, the MP7616 features 13-bit (0.012%) differential and 12-bit (0.01%) integral linearity.

To achieve 13-bit linearity without laser trim, the MP7616 digitally decodes the four MSB's into 15 equal current sources, rather than the standard binary-weighted sources. Each resistor contributes only 1/16 full scale output thus reducing the matching accuracy requirement of the resistor and CMOS switches from 0.0015% to 0.024%.

The decoding technique achieves an eightfold improvement in differential linearity stability over temperature, an eightfold improvement in relative accuracy due to aging effects (long term stability), a fourfold improvement in glitch amplitude, and a tenfold reduction in sensitivity to output amplifier offset voltage.



SIMPLIFIED BLOCK DIAGRAM



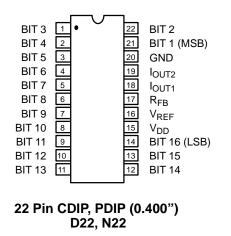
ORDERING INFORMATION

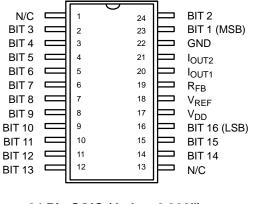
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP7616JN	<u>+</u> 14	<u>+</u> 16	<u>+</u> 0.8
Plastic Dip	–40 to +85°C	MP7616KN	<u>+</u> 7	<u>+</u> 8	<u>+</u> 0.8
SOIC	–40 to +85°C	MP7616JS	<u>+</u> 14	<u>+</u> 16	<u>+</u> 0.8
SOIC	–40 to +85°C	MP7616KS	<u>+</u> 7	<u>+</u> 8	<u>+</u> 0.8
Ceramic Dip	–40 to +85°C	MP7616JD	<u>+</u> 14	<u>+</u> 16	<u>+</u> 0.8
Ceramic Dip	–40 to +85°C	MP7616KD	<u>+</u> 7	<u>+</u> 8	<u>+</u> 0.8
Ceramic Dip	–55 to +125°C	MP7616TD*	<u>+</u> 7	<u>+</u> 8	<u>+</u> 0.8

*Contact factory for non-compliant military processing

PIN CONFIGURATION

See Packaging Section for Package Dimensions





24 Pin SOIC (Jedec, 0.300") S24

PIN OUT DEFINITIONS

DIP	SOIC	NAME	DESCRIPTION		DIP	SOIC	NAME	DESCRIPTION
	1	N/C	No Connection	1		13	N/C	No Connection
1	2	BIT 3	Data Input Bit 3		12	14	BIT 14	Data Input Bit 14
2	3	BIT 4	Data Input Bit 4		13	15	BIT 15	Data Input Bit 15
3	4	BIT 5	Data Input Bit 5		14	16	BIT 16	Data Input Bit 16 (LSB)
4	5	BIT 6	Data Input Bit 6		15	17	V _{DD}	Positive Power Supply
5	6	BIT 7	Data Input Bit 7		16	18	V _{REF}	Reference Input Voltage
6	7	BIT 8	Data Input Bit 8		17	19	R _{FB}	Internal Feedback Resistor
7	8	BIT 9	Data Input Bit 9		18	20	I _{OUT1}	Current Output 1
8	9	BIT 10	Data Input Bit 10		19	21	I _{OUT2}	Current Output 2
9	10	BIT 11	Data Input Bit 11		20	22	GND	Ground
10	11	BIT 12	Data Input Bit 12		21	23	BIT 1	Data Input Bit 1 (MSB)
11	12	BIT 13	Data Input Bit 13		22	24	BIT 2	Data Input Bit 2







ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	Min	25°C Typ	Max	Tmin to Min	Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE ¹								FSR = Full Scale Range
Resolution (All Grades)	N	16			16		Bits	
Integral Non-Linearity ⁵ (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
Ј К, Т				<u>+</u> 14 <u>+</u> 7		<u>+</u> 14 <u>+</u> 7		
Differential Non-Linearity ⁵ J K, T	DNL			<u>+</u> 16 <u>+</u> 8		<u>+</u> 16 <u>+</u> 8	LSB	
Gain Error	GE		<u>+</u> 0.8				% FSR	Using Internal R _{FB}
Gain Temperature Coefficient ²	TC _{GE}					<u>+</u> 2.0	ppm/°C	∆Gain/∆Temperature
Non-Linearity Tempco ²						<u>+</u> 0.5	ppm/°C	
Differential Linearity Tempco ²						<u>+</u> 0.5	ppm/°C	
Power Supply Rejection Ratio	PSRR		<u>+</u> 5	<u>+</u> 50		<u>+</u> 50	ppm/%	$ \Delta Gain/\Delta V_{DD} \Delta V_{DD} = \pm 5\%$
Output Leakage Current ⁶	I _{OUT}		<u>+</u> 1	<u>+</u> 10		<u>+</u> 200	nA	
DYNAMIC PERFORMANCE ²								
Current Settling Time	ts		2				μs	To 0.01% of FSR; all digital inputs low to high and high to low
Feedthrough at I _{OUT1}	F_{T}		1	2			mV p-p	$V_{REF} = 10$ kHz, 20 Vp-p
REFERENCE INPUT								
Input Resistance	R _{IN}	1	3	10	1	10	kΩ	
DIGITAL INPUTS ³								
Logical "1" Voltage Logical "0" Voltage Input Leakage Current	V _{IH} V _{IL} I _{LKG}	3.0	2.4	0.8 <u>+</u> 1.0	3.0	0.8 <u>+</u> 1.0	V V μA	
ANALOG OUTPUTS ²								
Output Capacitance								
	C _{OUT1} C _{OUT1} C _{OUT2} C _{OUT2}		100 50 50 100				pF pF pF pF	DAC Inputs all 1's DAC Inputs all 0's DAC Inputs all 1's DAC Inputs all 0's
POWER SUPPLY ⁴								
Functional Voltage Range ² Supply Current	V _{DD} I _{DD}	4.5	15 0.4	16 4	4.5	16 4	V mA	All digital inputs = 0 V or all = 5 V





ELECTRICAL CHARACTERISTICS (CONT'D)

NOTES:

- ¹ Full Scale Range (FSR) is 10V for unipolar mode.
- ² Guaranteed but not production tested.
- ³ Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
- ⁴ Specified values guarantee functionality. Refer to other parameters for accuracy.
- ⁵ Linearity error is degraded by 65μV for every mV of voltage offset at output amplifier.
- ⁶ Output leakage current refers to I_{OUT1} . One LSB of current constantly flows into I_{OUT2} (30nA at 5k Ω input impedance, $V_{REF} = +10$ V) due to ladder termination into I_{OUT2} .

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)^{1, 2}

V _{DD} to GND	0 to +17 V
Digital Input Voltage to GND	GND –0.5 to V_DD +0.5 V
I _{OUT1} , I _{OUT2} to GND	GND –0.5 to V_DD +0.5 V
V _{REF} to GND	<u>+</u> 25 V
V _{RFB} to GND	<u>+</u> 25 V

Storage Temperature65°C to +150°C
Lead Temperature (Soldering, 10 seconds) +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 1000mW
Derates above 75°C 13mW/°C

NOTES:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

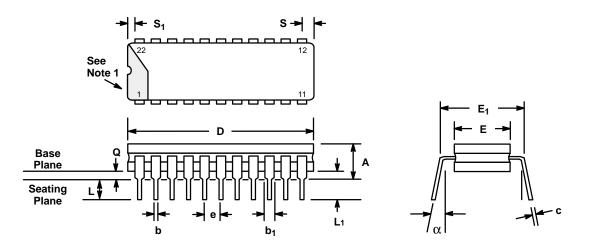
Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

APPLICATION NOTES Refer to Section 8 for Applications Information









	INCHES		MILLIN		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
А		.225		5.72	
b	0.014	0.023	0.356	0.584	_
b ₁	0.038	0.065	0.965	1.65	2
с	0.008	0.015	0.203	0.381	_
D		1.111		28.22	4
E	0.350	0.410	8.89	10.41	4
E ₁	0.390	0.420	9.91	10.67	7
е	0.1	00 BSC	2.5	4 BSC	5
L	0.125	0.200	3.18	5.08	_
L ₁	0.150		3.81		_
Q	0.015	0.070	0.381	1.78	3
S		0.080		2.03	6
S ₁	0.005		0.13		6
α	0°	15°	0°	15°	_

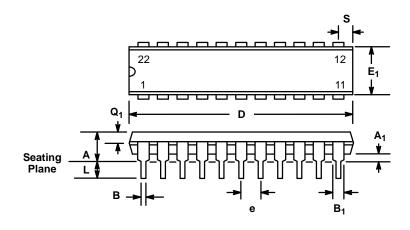
NOTES

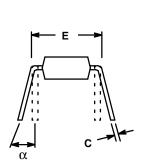
- 1. Index area; a notch or a lead one identification mark is located adjacent to lead one and is within the shaded area shown.
- 2. The minimum limit for dimension b_1 may be 0.023 (0.58 mm) for all four corner leads only.
- 3. Dimension Q shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-center lid, meniscus and glass overrun.
- 5. The basic lead spacing is 0.100 inch (2.54 mm) between centerlines.
- 6. Applies to all four corners.
- 7. This is measured to outside of lead, not center.











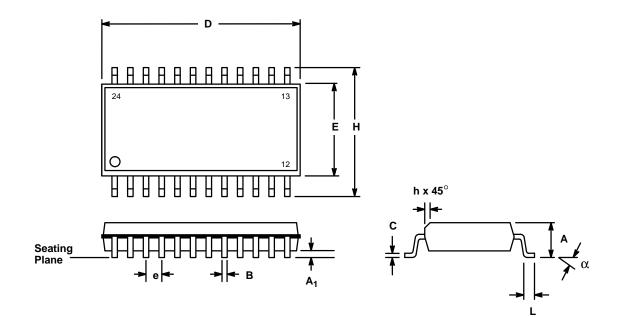
	INC	HES	MILLIN	IETERS
SYMBOL	MIN	MAX	MIN	MAX
А		0.225		5.72
A ₁	0.015		0.38	
В	0.014	0.023	0.356	0.584
B ₁ (1)	0.038	0.065	0.965	1.65
С	0.008	0.015	0.203	0.381
D	1.050	1.110	26.67	28.19
E	0.385	0.425	9.78	10.80
E ₁	0.330	0.380	8.38	9.65
е	0.1	00 BSC	2.5	4 BSC
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q ₁	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.









	INC	CHES	MILLIN	IETERS	
SYMBOL	MIN	MAX	MIN	MAX	
А	0.097	0.104	2.464	2.642	
A1	0.0050	0.0115	0.127	0.292	
В	0.014	0.019	0.356	0.483	
С	0.0091	0.0125	0.231	0.318	
D	0.602	0.612	15.29	15.54	
E	0.292	0.299	7.42	7.59	
е	0.0	50 BSC	1.27 BSC		
н	0.400	0.410	10.16	10.41	
h	0.010	0.016	0.254	0.406	
L	0.016	0.035	0.406	0.889	
α	0°	8°	0°	8°	





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