DF6811

8-bit FAST Microcontrollers Family

ver 2.08

OVERVIEW

Document contains brief description of DF6811 core functionality. The DF6811 is a advanced 8-bit MCU IP Core with highly sophisticated, on chip peripheral capabilities. DF6811 soft core is binary-compatible with the industry standard 68HC11 8-bit microcontroller and can achieve a performance **45-100 million instructions** per second. DF6811 has FAST architecture that is 3.8 times faster compared to original implementation. Core in standard configuration has integrated on chip major peripheral function.

There are two serial interfaces: an asynchronous serial communications interface (SCI) and a separate synchronous serial peripheral interface (SPI).

The main 16-bit, free-running timer system has implemented three input capture lines, five output-compare lines, and a real-time interrupt function.

An 8-bit pulse accumulator subsystem can count external events or measure external periods.

Self-monitoring circuitry is included on-chip to protect against system errors. A computer operating properly (COP) watchdog system protects against software failures. An illegal opcode detection circuit provides a non-maskable interrupt if illegal opcode is detected.

Two software-controlled power-saving modes, WAIT and STOP, are available to conserve additional power. These modes make the DF6811 IP Core especially attractive for automotive and battery-driven applications.

The DF6811 have built in the development support features designed into DF6811. The LIR signal is intended as a debugging aid. This signal is driven to active low for the first bus cycle of each new instruction, making it easy to reverse assemble (disassemble) instructions from the display of a logic analyzer.

DF6811 is **fully customizable**, which means it is delivered in the exact configuration to meet users requirements. *There is no need to pay extra for not used features and wasted silicon.* It includes **fully automated testbench** with **complete set of tests** allowing easy package validation at each stage of SoC design flow.

CPU FEATURES

- FAST architecture, 3,8 times faster than the original implementation
- Software compatible with industry standard 68HC11
- 10 times faster multiplication
- 16 times faster division
- 64 bytes of remapped System Function Registers space (SFRs)
- Up to 16M bytes of Data Memory
- De-multiplexed Address/Data Bus to allow easy connection to memory
- Two power saving modes: STOP, WAI

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- User programmable External Data Memory Write and Read pulses between 1 to 8 clock periods
- Fully synthesizable, static synchronous design with no internal tri-states
- No internal reset generator or gated clock
- Scan test ready
- Technology independent HDL source code
- Core can be fully customized

DESIGN FEATURES

♦ ONE GLOBAL SYSTEM CLOCK

♦ SYNCHRONOUS RESET

The DF6811 has 3 reset vectors sources, which easy identify a cause of system reset.

♦ ALL ASYNCHRONOUS INPUT SIGNALS ARE SYNCHRONIZED BEFORE INTERNAL USE

♦ DATA MEMORY:

The DF6811 can address up to 16M bytes of Data Memory via the function interconnect signals. The 64 bytes of Data Memory in every 64k page is reserved for the Function Registers. Extra DPP (Data Page Pointer) register is used for segments swapping. Data Memory can be implemented as synchronous or asynchronous.

PERIPHERALS

The peripherals listed below are not implemented in standard configuration of DF6811. They can be integrated in Core as a option.

- Four 8-bit I/O Ports
- Interrupt Controller
  - *20 interrupt sources*
  - *17 priority levels*
  - *Dedicated Interrupt vector for each interrupt source*
- Main16-bit timer/counter system
  - *16 bit free running counter*
  - *Four stage programmable prescaller*
  - *Timer clocked by internal source*
  - *Real Time Interrupt*
- 16-bit Compare/Capture Unit
  - *Three independent input-capture functions*
  - *Five output-compare channels*
  - *Events capturing*
  - *Pulses generation*
  - *Digital signals generation*
  - *Gated timers*
  - *Sophisticated comparator*
  - *Pulse width modulation*
  - *Pulse width measuring*
- 8-bit Pulse accumulator
  - *Two major modes of operation*
    - *Simple event counter*
    - *Gated time accumulation*
  - *Clocked by internal source or external pin*
- Full-duplex UART - SCI
  - *Standard Nonreturn to Zero format (NRZ)*
  - *8 or 9 bit data transfer*
  - *Integrated baud rate generator*
  - *Enhanced receiver data sampling technique*
  - *Noise, Overrun and Framing error detection*
  - *IDLE and BREAK characters generation*
  - *Wake-up block to recognize UART wake-up from IDLE condition*
  - *Three SCI related interrupts*
- SPI – Master and Slave Serial Peripheral Interface
  - *Supports speeds up ¼ of system clock*
    - *Mode fault error*
    - *Write collision error*
  - *Software selectable polarity and phase of serial clock SCK*
  - *System errors detection*
  - *Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)*
  - *Interrupt generation*

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

CONFIGURATION

The following parameters of the DF6811 core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

• Data Memory size	- 64 kB - 16 MB
• Data Memory wait-states	- used (0-7) - unused
• Power saving STOP mode	- used - unused
• WATCHDOG Timer	- used - unused
• Timer system	- used - unused
• Compare Capture channels	- used - unused
• Pulse Accumulator	- used - unused
• PORTS A, B, C, D	- used - unused
• SCI – UART Interface	- used - unused
• SPI Interface	- used - unused
• Support for IDIV Instruction	- used - unused
• Support for FDIV Instruction	- used - unused
• Support for MUL Instruction	- used - unused
• Support for DAA Instruction	- used - unused

LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted,or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

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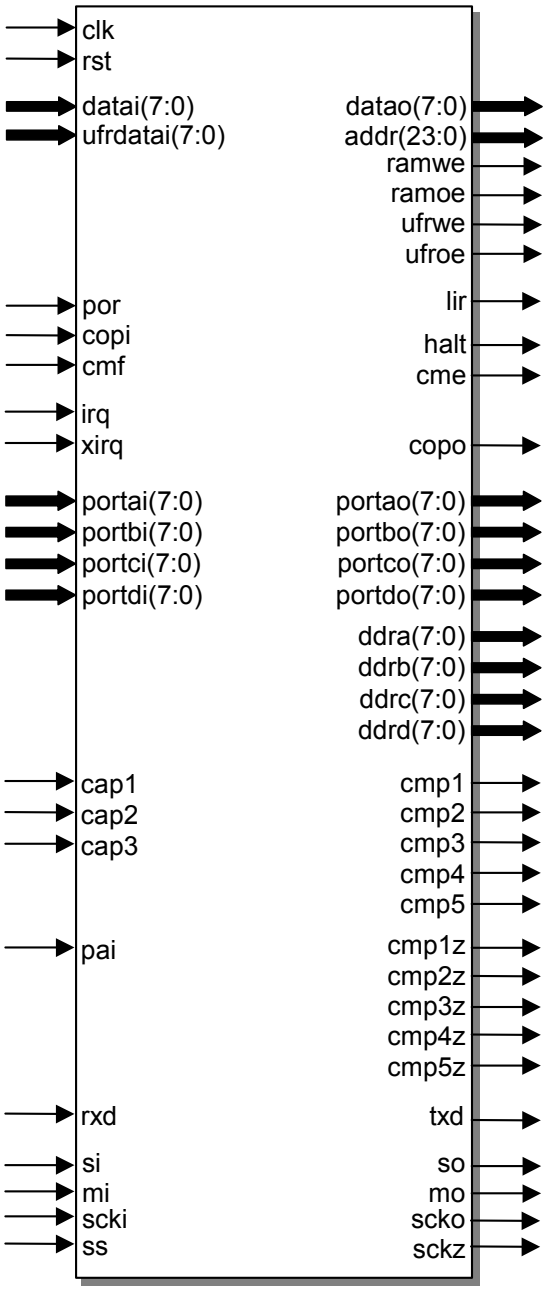
PINS DESCRIPTION

PIN	ACTIVE	TYPE	DESCRIPTION
clk	-	input	Global system clock
rst	Low	input	Global system reset
datai[7:0]	-	input	External memory bus input
ufrdatai[7:0]	-	input	UFRs data bus input
por	Low	input	Power on reset vector fetch
copi	Low	input	COP timeout vector fetch
cmf	Low	input	Clock monitor fail vector fetch
datai[7:0]	-	input	External memory bus input
ufrdatai[7:0]	-	input	UFRs data bus input
irq	*	input	Interrupt input
xirq	Low	input	Non-maskable interrupt input
portai[7:0]	-	input	Port A input
portbi[7:0]	-	input	Port B input
portci[7:0]	-	input	Port C input
portdi[7:0]	-	input	Port D input
cap1,2,3	Low	input	Capture inputs
pai	*	input	Pulse accumulator input
rxd	Low	input	SCI receiver data input
si	High	input	SPI slave input
mi	High	input	SPI master input
scki	*	input	SPI clock input
ss	Low	input	SPI slave select
datao[7:0]	-	output	Data memory & UFR bus output
addr[23:0]	-	output	Data memory & FR address bus
ramwe	Low	output	Memory write enable
ramoe	Low	output	Memory output enable
ufrwe	Low	output	UFRs write enable
ufroe	Low	output	UFRs output enable
lir	Low	output	Load instruction register
halt	High	output	Halt clock system (STOP inst.)
cme	High	output	Clock monitor enable
copo	Low	output	WATCHDOG timeout output
cmp1,2,3,4,5	*	output	Compare outputs
cmp1z,2,3,4,5	High	output	Disconnect output compare
portxo[7:0]	-	output	Port A, B, C, D output
ddrx[7:0]	-	output	Port A, B,C,D data direction control
cmp1,2,3,4,5	*	output	Compare outputs
cmp1z,2,3,4,5	High	output	Disconnect output compare
txd	Low	output	SCI transmitter data output
so	High	output	SPI slave output
mo	High	output	SPI master output
scko	*	output	SPI clock output
sckz	High	output	Disconnect SPI clock output

**** Kind of activity is configurable***

SYMBOL

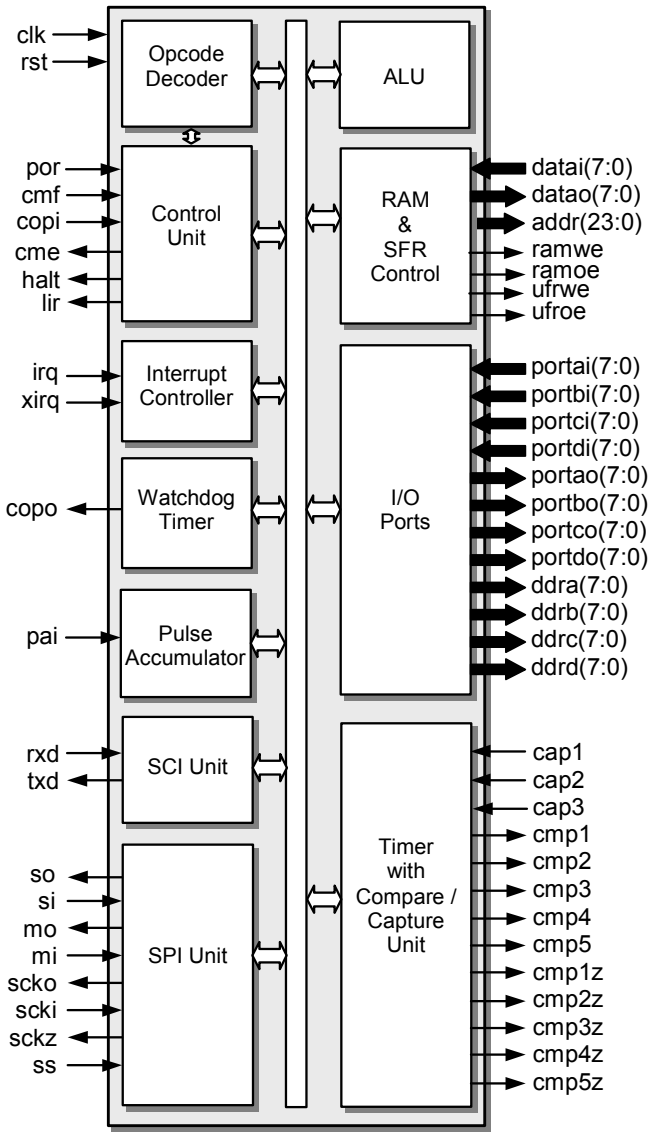


BLOCK DIAGRAM

Control Unit - Performs the core synchronization and data flow control. This module manages execution of all instructions. The Control Unit also manages execution of STOP instruction and waking-up the processor from the STOP mode.

Opcode Decoder - Performs an instruction opcode decoding and the control functions for all other blocks**.**

ALU - Arithmetic Logic Unit performs the arithmetic and logic operations during execution of an instruction. It contains accumulator (A, B), Condition Code Register (CCREG), Index registers X, Y and related logic such as arithmetic unit, logic unit, multiplier and divider.



RAM & SFR Controller - Data Memory & SFR (Special Function Register) interface controls access into the internal and external program and data memories and special registers. It contains Stack Pointer (SP) register, INIT register (INIT), Data Page Pointer (DPP), Stretch register (ST) and related logic.

Interrupt Controller - DF6811 extended IC has implemented 17-level interrupt priority control. The interrupt requests may come from external pins (IRQ and XIRQ) as well as from particular peripherals. The DF6811 peripheral systems generate maskable interrupts, which are recognized only if the global interrupt mask bit (I) in the CCR is cleared. Maskable interrupts are prioritized according to default arrangement (look at the table below) established during reset. However any one source may be elevated to the highest maskable priority position using HPRIO register. When interrupt condition occurs, an interrupt status flag is set to indicate the condition. and divider.

Timer, Compare Capture & COP Watchdog - This timer system is based on a free-running 16-bit counter with a 4-stage programmable prescaler. A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. Three independent input-capture functions are used to automatically record the time when a selected transition is detected at a respective timer input pin. Five output-compare functions are included for generating output signals or for timing software delays. Since the input-capture and output-compare functions may not be familiar to all users, these concepts are explained in greater detail. A programmable periodic interrupt circuit called RTI is tapped off of the main 16-bit timer counter. Software can select one of four rates for the RTI, which is most commonly used to pace the execution of software routines. The COP watchdog function is loosely related to the main timer in that the clock input to the COP system (clk*2^{17}) is tapped off the free-running counter chain.
The timer subsystem involves more registers and control bits than any other subsystem on the MCU. Each of the three input-capture functions has its own 16-bit time capture latch (input-capture register) and each of the five output-compare functions has its own 16-bit compare register. All timer functions, including the timer overflow and RTI, have their own interrupt controls and separate interrupt vectors. Additional control bits permit software to control the edge(s) that trigger each input-capture function and the automatic actions that result from output-compare functions. Although hardwired logic is included to automate many timer activities, this timer architecture is essentially a software-oriented system. This structure is easily adaptable to a very wide range of applications although it is not as

efficient as dedicated hardware for some specific timing applications. and divider.

SCI - The SCI is a full-duplex UART type asynchronous system, using standard non return to zero (NRZ) format : 1 start bit, 8 or 9 data bits and a 1 stop bit. The DF6811 resynchronizes the receiver bit clock on all one to zero transitions in the bit stream. Therefore differences in baud rate between the sending device and the SCI are not as likely to cause reception errors. Three logic samples are taken near the middle of data bit time, and majority logic decides the sense for the bit. For the start and stop bits seven logic samples are taken. Even if noise causes one of these samples to be incorrect, the bit will still be received correctly. The receiver also has the ability to enter a temporary standby mode (called receiver wakeup) to ignore messages intended for a different receiver. Logic automatically wakes up the receiver in time to see the first character of the next message. This wakeup feature greatly reduces CPU overhead in multi-drop SCI networks. The SCI transmitter can produce queued characters of idle (whole characters of all logic 1) and break (whole characters of all logic 0). In addition to the usual transmit data register empty (TDRE) status flag, this SCI also provides a transmit complete (TC) indication that can be used in applications with a modem.

SPI Unit – it's a fully configurable master/slave Serial Peripheral Interface, which allows user to configure polarity and phase of serial clock signal SCK. It allows the microcontroller to communicate with serial peripheral devices. It is also capable of interprocessor communications in a multi-master system. A serial clock line (SCK) synchronizes shifting and sampling of the information on the two independent serial data lines. SPI data are simultaneously transmitted and received. SPI system is flexible enough to interface directly with numerous standard product peripherals from several manufacturers. Data rates as high as CLK/4. Clock control logic allows a selection of clock polarity and a choice of two fundamentally different clocking protocols to accommodate most available synchronous serial peripheral devices. When the SPI is configured as a master, software selects one of four different bit rates for the serial clock. SPI automatically drives slave select outputs SSO[7:0], and address SPI slave device to exchange serially shifted data. Error-detection logic is included to support interprocessor communications. A write-collision detector indicates when an attempt is made to write data to the serial shift register while a transfer is in progress. A multiple-master mode-fault detector automatically disables SPI output drivers if more than one SPI devices simultaneously attempts to become bus master.

Pulse Accumulator – This system is based on an 8-bit counter and can be configured to operate as a simple event counter or for gated time accumulation. Unlike the main timer, the 8-bit pulse accumulator counter can be read or written at any time (the 16-bit counter in the main timer cannot be written). Control bits allow the user to configure and control the pulse accumulator subsystem. Two maskable interrupts are associated with the system, each having its own controls and interrupt vector. The PAI pin associated with the pulse accumulator can be configured to act as a clock (event counting mode) or as a gate signal to enable a free-running E divided by 64 clock to the 8-bit counter (gated time accumulation mode). The alternate functions of the pulse accumulator input (PAI) pin present some interesting application possibilities.

I/O Ports - All ports are 8-bit general-purpose bi-directional I/O system. The PORTA, PORTB, PORTC, PORTD data registers have their corresponding data direction registers DDRA, DDRB, DDRC, DDRD to control ports data flow. It assures that all DF6811's ports have full I/O selectable registers. Writes to any ports pins cause data to be stored in the data registers. If any port pins are configured as output then data registers are driven out of those pins. Reads from port pins configured as input causes that input pin is read. If port pins is configured as output, during read data register is read. Writes to any ports pins not configured as outputs do not cause data to be driven out of those pins, but the data is stored in the output registers. Thus, if the pins later become outputs, the last data written to port will be driven out the port pins.

OPTIONAL PERIPHERALS

There are also available an optional peripherals, not included in presented DF6811 Microcontroller Core. The optional peripherals, can be implemented in microcontroller core upon customer request.

- PWM – Pulse Width Modulation Timer
  - *2 independent 8-bit PWM channels, concatenated on one 16-bit PWM channel*
  - *Software-selectable duty from 0% to 100% and pulse period*
  - *Software-selectable polarity of output waveform*
- I2C bus controller - Master
  - *7-bit and 10-bit addressing modes*
  - *NORMAL, FAST, HIGH speeds*
  - *Multi-master systems supported*
  - *Clock arbitration and synchronization*
  - *User defined timings on I2C lines*
  - *Wide range of system clock frequencies*
  - *Interrupt generation*
- I2C bus controller - Slave
  - *NORMAL speed 100 kbs*
  - *FAST speed 400 kbs*
  - *HIGH speed 3400 kbs*
  - *Wide range of system clock frequencies*
  - *User defined data setup time on I2C lines*
  - *Interrupt generation*
- Programmable Watchdog Timer
- Fixed-Point arithmetic coprocessor
  - *Multiplication - 16bit * 16bit*
  - *Division - 32bit / 16bit*
  - *Division - 16bit / 16bit*
  - *Left and right shifting - 1 to 31 bits*
  - *Normalization*
- Floating-Point arithmetic coprocessor IEEE-754 standard single precision
  - *FADD, FSUB - addition, subtraction*
  - *FMUL, FDIV- multiplication, division*
  - *FSQRT- square root*
  - *FUCOM - compare*
  - *FCHS - change sign*
  - *FABS - absolute value*
- Floating-Point math coprocessor - IEEE-754 standard single precision real, word and short integers
  - *FADD, FSUB- addition, subtraction*
  - *FMUL, FDIV- multiplication, division*
  - *FSQRT- square root*
  - *FUCOM- compare*
  - *FCHS - change sign*
  - *FABS - absolute value*
  - *FSIN, FCOS- sine, cosine*
  - *FTAN, FATAN – tangent arcs tangent*

PERFORMANCE

The following tables give a survey about the Core area and performance in the ASICs and Programmable Logic Devices after Place & Route (all CPU features and peripherals have been included):

Device	Speed grade	F_{max}
ORCA 3T	-7	8 MHz
ORCA 4E	-3	31 MHz
ispXPGA	-5	30 MHz

Core performance in LATTICE® devices

Area utilized by the each unit of DF6811 core in vendor specific technologies is summarized in table below.

Component	Area [LC / PFU]	Area [FFs]
CPU*	2300 / 340	311
Main Timer	83 / 14	50
COM/CAP	501 / 86	196
Watchdog	72 / 13	30
Pulse Acc.	48 / 9	19
SPI Interface	135 / 24	60
UART - SCI	326 / 60	131
I/O Ports	157 / 28	96
Total area	3300 / 574	893

*CPU – consisted of ALU, Control Unit and Instruction Decoder, Bus Controller with support for 16MB RAM, External IRQ and XIRQ pin Interrupt Controller

Core components area utilization

IMPROVEMENT

For user the most important is application speed improvement. The most commonly used arithmetic functions and theirs improvement are shown in table below.

Improvement was computed as {M68HC11 clock periods} divided by {DF6811 clock periods} required to execute an identical function. More details are available in core documentation

Function	Improvement
8-bit addition (*immediate data*)	**4**
8-bit addition (*direct addressing*)	**4**
8-bit addition (*indirect addressing*)	**4**
8-bit subtraction (*immediate data*)	**4**
8-bit subtraction (*direct addressing*)	**4**
8-bit subtraction (*indirect addressing*)	**4**
16-bit addition (*immediate data*)	**5,3**
16-bit addition (*direct addressing*)	**5**
16-bit addition (*indirect addressing*	**4,8**
16-bit subtraction (*immediate data*)	**5,3**
16-bit subtraction (*direct addressing*)	**5**
16-bit subtraction (*indirect addressing*	**4,8**
Multiplication	**10**
Fractional division	**14,9**
Integer division	**16.4**

DF6811 FAMILY OVERVIEW

The main features of each DF6811X family member have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application. User can specify its own peripheral set (including listed below and the others) and requests the core modifications.

Design	Physical Linear memory space	Paged Data Memory space	Motorola Memory Expansion Logic	Interrupt sources	Interrupt levels	Real Time Interrupt	Data Pointers	Main Timer System	Compare\Capture	SCI (UART)	I\O Ports	SPI M/S Interface	Watchdog Timer	Pulse accumulator	Interface for additional SFRs
DF6811	64k	16M	-	20	17	✓	1*	1*	5/3*	1*	4	✓*	✓*	✓*	✓
DF6811CPU	64k	16M	-	3	3	+	1*	+	+	+	+	+	+	+	✓

DF6811X family of High Performance Microcontroller Cores

\+ optional
* configurable

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