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October 2010

FSLV16211 — 24-Bit Bus Switch

Features

- 5Ω Switch Connection between Two Ports
- Minimal Propagation Delay through the Switch
- Low I_{CC}
- Zero Bounce in Flow-Through Mode
- Packaged in Thin-Shrink Small Outline Package (TSSOP)

Description

The FSLV16211 is a 24-bit, high-speed, low-voltage bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

This design can be used as a 12- or 24-bit bus switch. When /OE1 is LOW, port 1A is connected to Port 1B. When /OE2 is LOW, port 2A is connected to Port 2B.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FSLV16211MTDX	-40°C to 85°C	56-Lead, Thin Shrink Small Outline Package (TSSOP), JEDEC M0-153, 6.1mm Wide	Tape and Reel
		1A1 1A1 1A12 /OE1 /OE1	
		2A ₁ 2B ₁ 2A ₁₂ /OE ₂ 2B ₁₂ 2B ₁₂	
		Figure 1. Logic Diagram	

∇		_
	56	
	55	- OE2
	54	— 1B ₁
	53	— 1B ₂
	52	— 1B ₃
	51	— 1B ₄
	50	— 1B ₅
	49	- GND
	48	— 1B ₆
	47	— 1B ₇
	46	— 1B ₈
	45	— 1B ₉
	44	— 1B ₁₀
	43	- 1B ₁₁
	42	- 1B ₁₂
	41	- 2B1
	40	- 2B ₂
	39	- 2B ₃
	38	- GND
	37	— 2B ₄
	36	- 2B ₅
	35	- 2B ₆
	34	- 2B7

Figure 2. Pin Assignments for TSSOP (Top Through View)

33 - 2B₈ 32 - 2B₉

31 - 2B₁₀

30 - 2B₁₁ 29 - 2B₁₂

NC 1A₁ 1A₂ 1A3 1A4 1A5 1A₆ GND -1A7• 1A₈ -10 1A₉ 11 1A₁₀-12 1A₁₁-13 1A₁₂ 14 2A1-15 2A2-16 V_{CC}-17 2A3-18 GND-19 2A4 20 2A5-21 2A6-22 2A7-23

2A8-24

2A₉ 25 2A₁₀ 26

2A11 27

2A12-28

Pin Description

Connection Diagram

Pin Name	Description
$\overline{OE}_1, \overline{OE}_2$	Bus Switch Enables
1A, 2A	Bus A
1B, 2B	Bus B
NC	No Connect

Truth Table

Inp	uts	Inputs/0	Dutputs
OE ₁	OE ₂	1A,1B	2A, 2B
Low	Low	1A=1B	2A=2B
Low	High	1A=1B	Z
High	Low	Z	2A=2B
High	High	Z	Z

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	-0.5	4.6	V
Vs	DC Switch Voltage ⁽¹⁾	-0.5	4.6	V
V _{IN}	DC Input Voltage	-0.5	4.6	V
I _{IK}	DC Input Diode Current		-50	mA
I _{OUT}	DC Output Sink Current		128	mA
I _{CC} /I _{GNG}	DC V _{CC} /GND Current		±100	mA
T _{STG}	Storage Temperature Range	-65	150	°C

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.⁽²⁾

Symbol	Parameter		Min.	Max.	Unit
Vcc	Power Supply Operating Voltage		2.3	3.6	V
V _{IN}	Input Voltage		0	3.6	V
V _{OUT}	Output Voltage		0	3.6	V
4 4	t _r , t _f Input Rise and Fall Time	Switch Control Input	0	4.0	ns/V
ι _r , ι _f		Switch I/O	0	DC	ns/V
T _A	Free Air Operating Temperature		-40	85	°C

Note:

2. Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Not all conditions may appear on all switch types.

Ourseland	Parameter	Conditions	V _{cc}	T _A = -	40°C to	+85°C	11
Symbol		Conditions	(V)	Min.	Тур.	Max.	Unit
VIK	Clamp Diode Voltage	I _{IN} = -18mA	3.0			-1.2	V
V _{IH}	HIGH Level Control Input Voltage		2.3-2.7 2.7-3.6	1.7 2.0			V
V _{IL}	LOW Level Control Input Voltage		2.3-2.7			0.7	V
		Force V _I = 3.6V, I _{OUT} = 0.0A	2.3			10	
۱L	Input Leakage Current	Force V _I = 3.6V	0.0			10	μA
		$0 \leq V_{IN} \leq \ 3.6V$	3.6			1	
I _{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0A$	3.6			10	μA
ΔI_{CC}	Increase in I _{CC} per Input	One Input at 3V Other Inputs at V _{CC} or GND	3.6			300	μA
l _{oz}	Off-State Leakage	$0.0 \le A, B \le 3.6V$	3.6	-1		1	μA
		$I_{IN} = 64 \text{mA}, V_I = 0.0 \text{V}$	3.0		5	7	
		$I_{IN} = 30 \text{mA}, V_I = 0.0 \text{V}$	3.0		5	7	
		I_{IN} = 15mA, V_I = 2.4V	3.0		10	15	
Ron	Switch On Resistance	I _{IN} = 15mA, V _I = 3.0V	2.3			20	Ω
NON	Switch On Resistance	$I_{IN} = 64mA, V_I = 0.0V$	2.3		5	8	52
		I_{IN} = 30mA, V_I = 0.0V	2.3		5	8	
		I _{IN} = 15mA, V _I = 1.7V	2.3		10	15	
		I _{IN} = 15mA, V _I = 2.0V	2.3			20	

AC Electrical Characteristics

		T _A =-40°C to +85°C		T _A =40°C			
Cumhal	Devementer	C_L =30pF, R _L =500Ω V _{CC} = 2.5V ± 0.20V		C _L =50pF, R _L =500Ω V _{CC} =3.3V ± 0.30V			
Symbol	Parameter					- Unit	
		Min.	Max.	Min.	Max.		
t _{PHL} , t _{PLH}	Propagation Delay ⁽³⁾		0.15		0.25	ns	
t _{PHZ} , t _{PLZ}	Enable Time	0.5	4.7	1.0	7.0	ns	
t _{PZH} , t _{PZL}	Disable Time	0.5	5.1	1.0	5.5	ns	

Note:

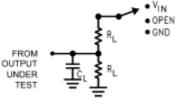
3. This parameter is guaranteed by design, but is not production tested. The bus switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the load capacitance when driven by an ideal voltage source (zero output impedance).

Capacitance

 T_A = +25°C, f = 1MHz, unless otherwise noted. Capacitance is characterized, but not production tested.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
CIN	Control Pin Input Capacitance	V _{CC} – 3.3V		4.5		pF
C _{I/O}	Input/Output Capacitance	V _{CC} , /OE= 3.3V		18		pF

AC Loading Waveforms



 TEST
 SWITCH

 tPD
 Open

 tPLZ/tPZL
 VIN

 tPHZ/tPZH
 GND

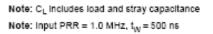
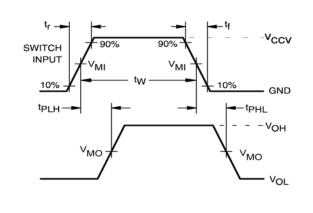
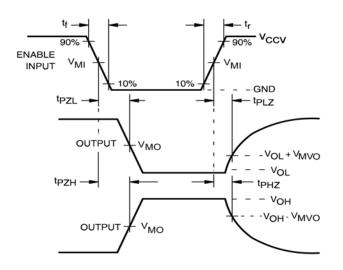


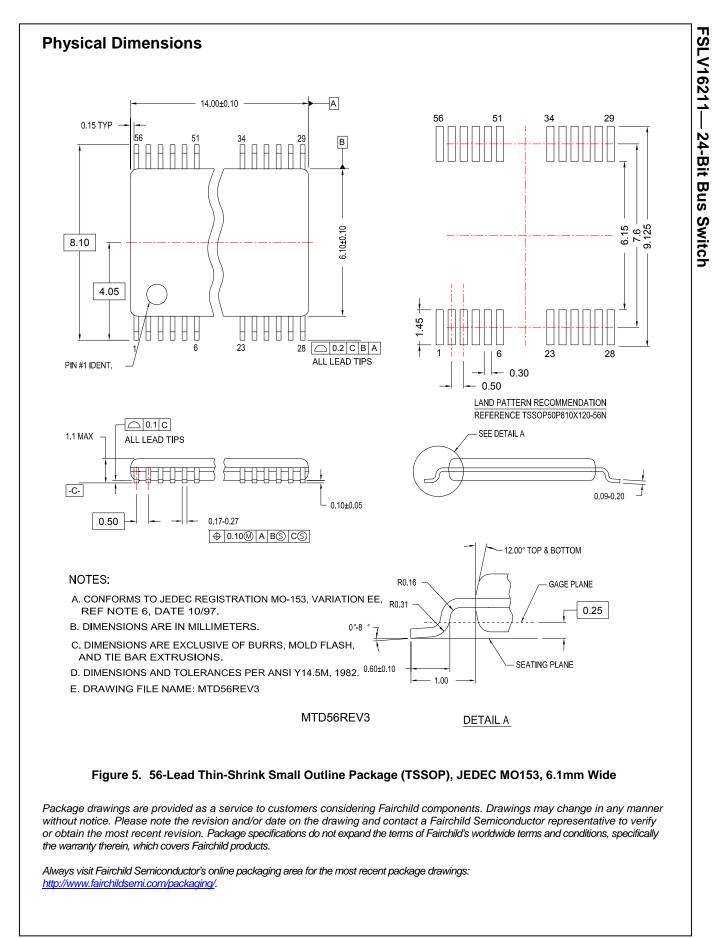
Figure 3. AC Test Circuit

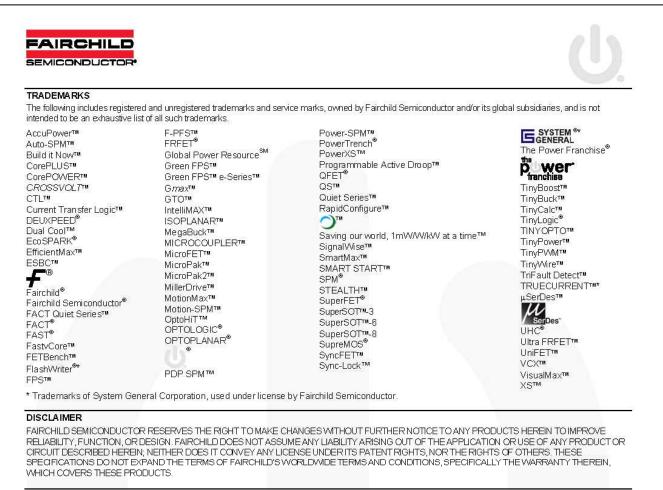






V _{cc}				
Symbol	3.3V ± 0.3V	2.5V ± 0.2V		
V _{MI}	1.5V	V _{CC} /2		
V _{MO}	1.5V	V _{CC} /2		
V _{MVO}	0.3V	0.15V		
V _{IN}	6.0V	2 x V _{CC}		
V _{CCV}	3.0V	V _{CC}		
t _r /t _f	2ns	2.5ns		





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SLV16211—24-Bit Bus Switch

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