IP4340CX15

6-channel filter for ESD protection of microSD memory card interfaces

Rev. 2 — 13 August 2012 Product data sheet

1. Product profile

1.1 General description

Array of 13 diodes and 11 resistors designed to protect downstream components against ElectroStatic Discharge (ESD) voltages as high as 15 kV. The device is encapsulated in a 1.56 mm × 1.56 mm Wafer-Level Chip-Scale Package (WLCSP) fabricated using monolithic silicon semiconductor technology.

These features make the device ideal for use in applications requiring a high degree of miniaturization, such as mobile phone handsets, cordless telephones and personal digital devices.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Integrated ESD protection, ElectroMagnetic Interference (EMI) and RF filtering for microSD memory card channels
- ESD protection up to 15 kV on 6 channels at output terminals
- Integrated EMI and RF filters with pull-up resistors (on 5 channels)
- Additional power supply protection
- WLCSP with 0.4 mm pitch

1.3 Applications

- MicroSD memory card interfaces in cellular phone and Personal Communication System (PCS) mobile handsets
- Cordless telephones
- Digital still and video cameras
- Media players
- Card readers

2. Pinning information

2.1 Pinning

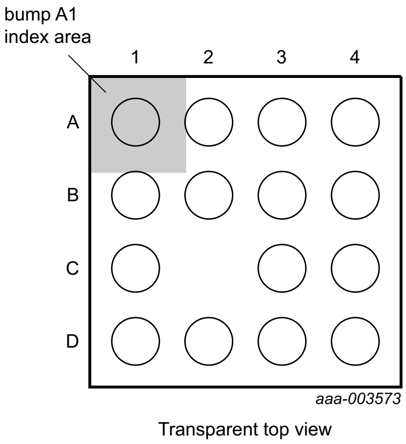


Fig 1. Pin configuration IP4340CX15

2.2 Pin description

Table 1. Pin description

Symbol	Pin	Type[1]	Description
DATA0	A1	I/O	data 0 input or output
DATA1	A2	I/O	data 1 input or output
SDDATA1	A3	I/O	data 1 input or output on microSD card side
SDDATA0	A4	I/O	data 0 input or output on microSD card side
CLK	B1	I/O	clock signal input or output
V_{CC}	B2	S	supply voltage
GND	B3	S	ground
SDCLK	B4	I/O	clock signal on microSD card side
CMD	C1	I/O	command signal
n.c.	C2	-	-
GND	C3	S	ground
SDCMD	C4	I/O	command signal on microSD card side
DATA3	D1	I/O	data 3 input or output
DATA2	D2	I/O	data 2 input or output
SDDATA2	D3	I/O	data 2 input or output on microSD card side
SDDATA3	D4	I/O	data 3 input or output on microSD card side

[1] I = input, O = output, I/O = input and output, S = power supply.

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4340CX15/P	WLCSP15	wafer-level chip-size package; 15 bumps; 1.56 × 1.56 × 0.47 mm	IP4340CX15/P

4. Functional diagram

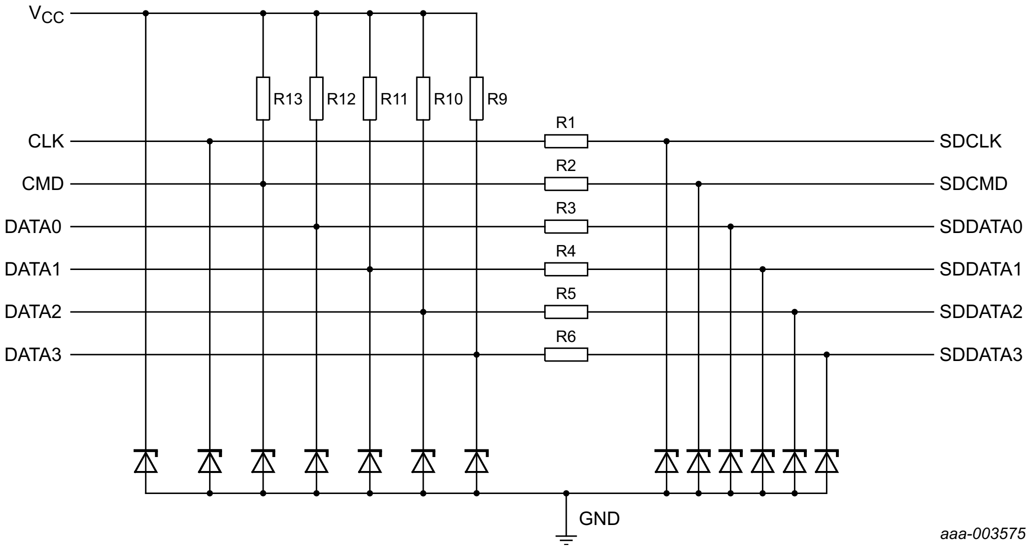


Fig 2. Schematic diagram IP4340CX15

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			–0.5	+5.0	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4, pins on microSD card side	[1]			
		contact discharge	[2]	–15	+15	kV
		air discharge		–15	+15	kV
		IEC 61000-4-2, level 1, all other pins				
		contact discharge		–2	+2	kV
		air discharge		–2	+2	kV
P_{ch}	channel power dissipation	continuous power; T_{amb} = 70 °C		-	25	mW
P_{tot}	total power dissipation	T_{amb} = 70 °C		-	100	mW

Table 3. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T_{stg}	storage temperature		–55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	$t_p \leq 10$ s	-	260	°C
T_{amb}	ambient temperature		–30	+85	°C

[1] Pins microSD card side: A3, A4, B4, C4, D3, D4 and B2

[2] Device is qualified with 1000 pulses of ±15 kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

6. Characteristics

Table 4. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance	R1 to R6	36	40	44	Ω
R_{pu}	pull-up resistance	R9 to R12	40	50	60	kΩ
		R13	12	15	18	kΩ
C_{line}	line capacitance	including diode capacitance; V_I = 0 V; f = 1 MHz; B2 = GND [1]	8	11	14	pF
V_{BR}	breakdown voltage	I_I = 1 mA	6	-	-	V
I_{RM}	reverse leakage current	V_I = 3 V	-	-	100	nA

[1] Guaranteed by design.

7. Frequency response

Table 5. Frequency response

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{il}	insertion loss	all channels; R_{source} = 50 Ω; R_L = 50 Ω				
		f < 400 MHz	-	-	7	dB
		400 MHz < f < 800 MHz	4	-	-	dB
		800 MHz < f < 2.5 GHz	8	-	-	dB
		2.5 GHz < f < 6.0 GHz	19	-	-	dB

8. Application information

8.1 Insertion loss

The insertion loss measurement configuration of a typical NetWork Analyzer (NWA) system is shown in Figure 3. The insertion loss is measured with a test Printed-Circuit Board (PCB) utilizing laser-drilled micro-via holes that connect the PCB ground plane to the IP4340CX15 ground pins.

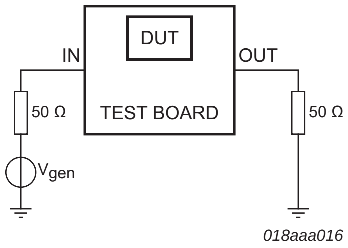
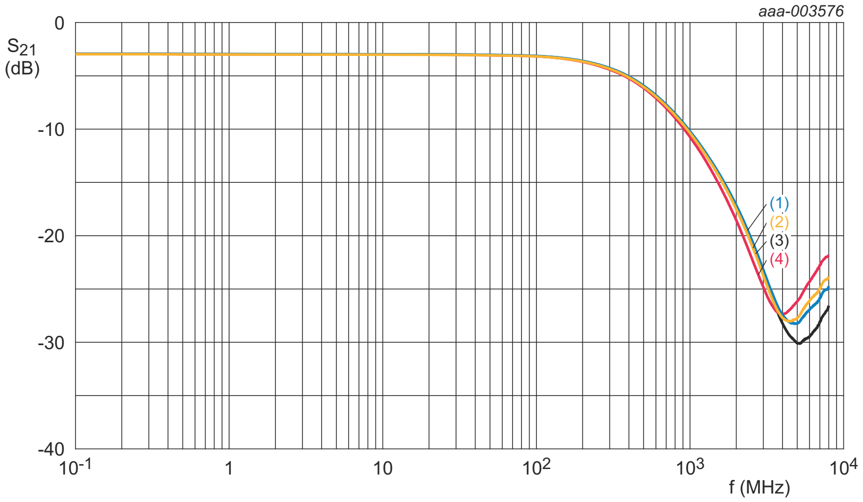


Fig 3. Frequency response setup

The frequency response curves for all channels at frequencies up to 6 GHz are shown in Figure 4.



(1) channel B1 to B4

(2) channel C1 to C4

(3) channel A1 to A4

(4) channel D2 to D4, A2 to A3, D1 to D4

Fig 4. Measured insertion loss magnitudes

8.2 Crosstalk

The setup for crosstalk measurements in a 50 Ω NWA system from one channel to another is shown in Figure 5. For the measurements, calibrated RF-probes are contacted to DUT bumps. Typical examples of crosstalk measurement results are depicted in Figure 6 and 7.

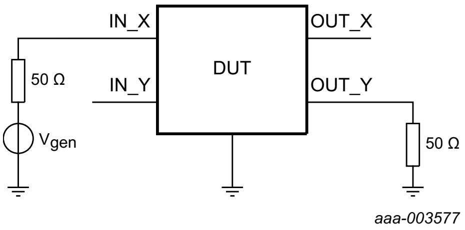
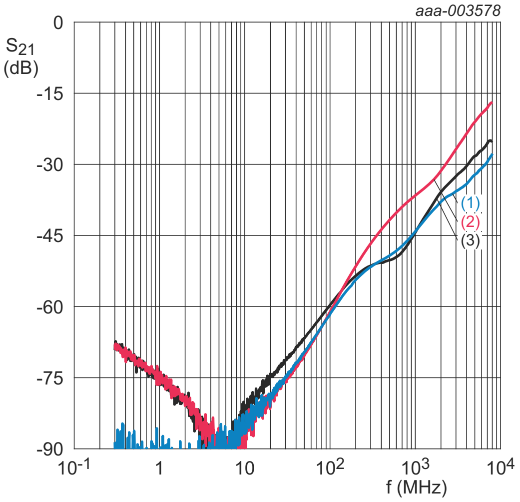


Fig 5. **Crosstalk measurement configuration**

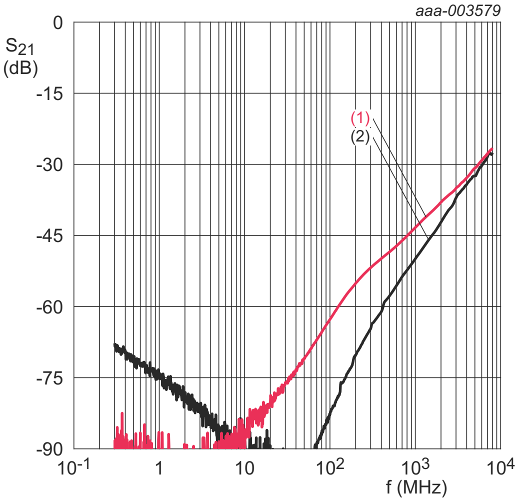


(1) Pin A1 to B4

(2) Pin A1 to A2, D1 to D2

(3) Pin A1 to A3, D1 to D3

Fig 6. **Crosstalk behavior between adjacent channels**



(1) Pin A2 to B4

(2) Pin A1 to C1

Fig 7. **Crosstalk behavior between adjacent channels**

9. Package outline

WLCSP15: wafer-level chip-size package; 15 bumps; (4 x 4 - C2)

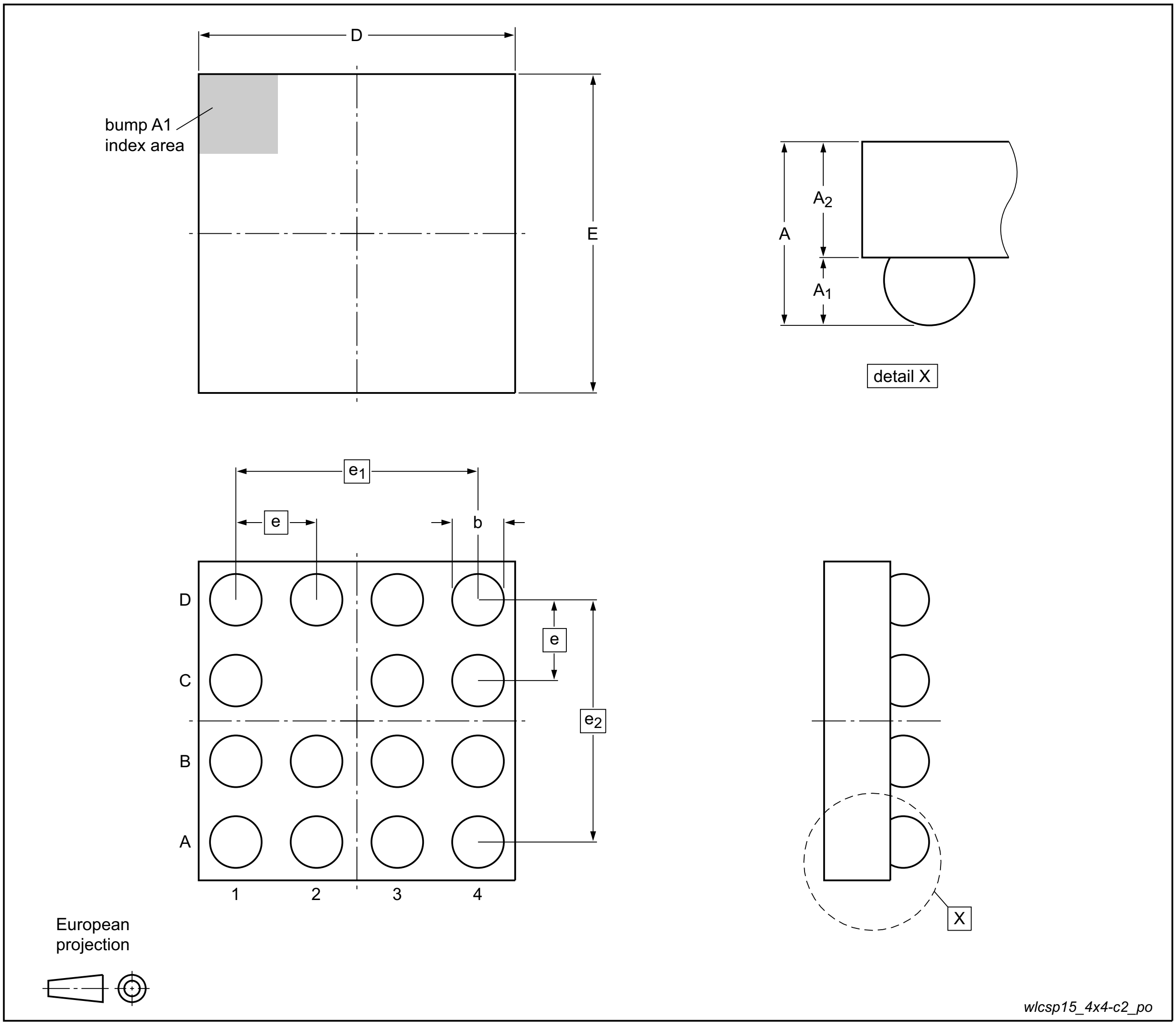


Fig 8. Package outline IP4340CX15 (WLCSP15)

Table 6. Package outline dimensions

Symbol	Min	Typ	Max	Unit
A	0.44	0.47	0.50	mm
A_1	0.18	0.20	0.22	mm
A_2	0.26	0.27	0.28	mm
b	0.21	0.26	0.31	mm
D	1.51	1.56	1.61	mm
E	1.51	1.56	1.61	mm

Table 6. Package outline dimensions *...continued*

Symbol	Min	Typ	Max	Unit
e	-	0.40	-	mm
e_1	-	1.2	-	mm
e_2	-	1.2	-	mm

10. Soldering of WLCSP packages

10.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 “Wafer Level Chip Scale Package”* and in application note *AN10365 “Surface mount reflow soldering description”*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

10.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

10.3 Reflow soldering

Key characteristics in reflow soldering are:

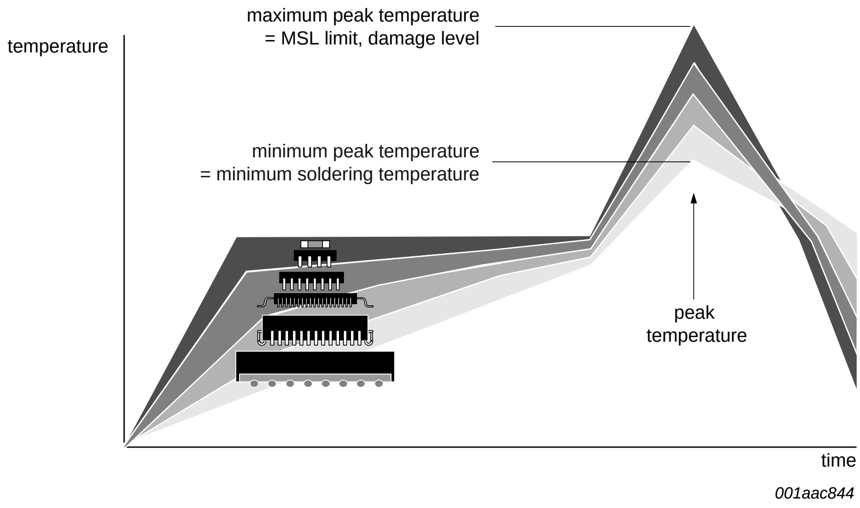
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 9) than a PbSn process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7.

Table 7. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 9.



MSL: Moisture Sensitivity Level

Fig 9. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 “Surface mount reflow soldering description”*.

10.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

10.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

10.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 “Surface mount reflow soldering description”*.

10.3.4 Cleaning

Cleaning can be done after reflow soldering.

11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4340CX15 v.2	20120813	Product data sheet	-	IP4340CX15 v.1
Modifications:	• Corrected package dimensions in Table 2 (height) and Table 6 (maximum values D and E)			
IP4340CX15 v.1	20120615	Product data sheet	-	-

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12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term ‘short data sheet’ is explained in section “Definitions”.

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