

# MAX20303

# Wearable Power Management Solution

## General Description

The MAX20303 is a highly integrated and programmable power management solution designed for ultra-low-power wearable applications. It is optimized for size and efficiency to enhance the value of the end product by extending battery life and shrinking the overall solution size. A flexible set of power-optimized voltage regulators, including multiple bucks, boost, buck-boost, and linear regulators, provides a high level of integration and the ability to create a fully optimized power architecture. The quiescent current of each regulator is specifically suited for 1 $\mu$ A (typ) to extend battery life in always-on applications.

The MAX20303 includes a complete battery management solution with battery seal, charger, power path, and fuel gauge. Both thermal management and input protection are built into the charger.

The device also includes a factory programmable button controller with multiple inputs that are customizable to fit specific product UX requirements.

Three integrated LED current sinks are included for indicator or backlighting functions, and an ERM/LRA driver with automatic resonance tracking is capable of providing sophisticated haptic feedback to the user.

The device is configurable through an I<sup>2</sup>C interface that allows for programming various functions and reading device status, including the ability to read temperature and supply voltages with the integrated ADC.

This device is available in a 56-bump, 0.5mm pitch 3.71mm x 4.21mm, wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

## Applications

- Wearable Devices
- IoT

**Ordering Information** appears at end of data sheet.

## Benefits and Features

- Extend Battery Use Time Between Battery Charging
  - 2 x Micro-I<sub>Q</sub> Buck Regulators (<1 $\mu$ A I<sub>Q</sub> (typ) Each)
    - 220mA Output
    - Buck1: 0.8V to 2.375V in 25mV Steps
    - Buck2: 0.8V to 3.95V in 50mV Steps
  - Micro-I<sub>Q</sub> LV LDO/Load Switch (1 $\mu$ A I<sub>Q</sub> (typ))
    - 1.16V to 2.0V Input Voltage
    - 50mA Output
    - 0.5V to 1.95V Output, 25mV Steps
  - Micro-I<sub>Q</sub> LDO/Load Switch (1 $\mu$ A I<sub>Q</sub> (typ))
    - 1.71V to 5.5V Input Voltage
    - 100mA Output
    - 0.9V to 4V, 100mV Steps
  - Micro-I<sub>Q</sub> Buck-Boost Regulator (1.3 $\mu$ A I<sub>Q</sub> (typ))
    - 250mW Output
    - 2.5V to 5V in 100mV Steps
- Easy-to-Implement Li+ Battery Charging
  - Wide Fast Charge Current Range: 5mA to 500mA
  - Smart Power Selector
    - 28V/-5.5V Tolerant Input
    - Programmable JEITA Current/Voltage Profiles
- Minimize Solution Footprint Through High Integration
  - Safe Output LDO
    - 15mA When CHGIN Present
    - 5V or 3.3V
  - Haptic Driver
    - ERM/LRA Driver with Quick Start And Breaking
    - Automatic Resonance Tracking (LRA only)
- Support Wide Variety of Display Options
  - Micro-I<sub>Q</sub> Boost Regulator (2.4 $\mu$ A I<sub>Q</sub> (typ))
    - 300mW Output
    - 5V to 20V in 250mV Step
  - 3 Channel Current Sinks
    - 20V Tolerant
    - Programmable from 0.6 to 30mA
- Optimize System Control
  - Power-On/Reset Controller
  - Programmable Push-Button Controller
  - Programmable Supply Sequencing
  - Factory Shelf Mode
  - On-Chip Voltage Monitor Multiplexer and Analog-to-Digital Converter (ADC)

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### Absolute Maximum Ratings

BAT, SYS, MON, PFN1, PFN2, THM, INT, RST,  
 SDA, SCL, CELL, ALRT, CTG, QSTRT, L2IN,  
 BBOUT .....-0.3V to +6V  
 VDIG, L1IN .....-0.3V to +2.2V  
 CHGIN .....-6V to +30V  
 CAP, SFOUT .....-0.3V to min(|CHGIN| + 0.3, +6)V  
 TPU .....-0.3V to VDIG + 0.3V  
 SET.....-0.3V to BAT + 0.3V  
 MPC0, MPC1, MPC2, MPC3, MPC4, DRP,  
 DRN, BK1LX, BK2LX, BK1OUT, BK2OUT,  
 CPP, BSTLVLX, BBLVLX.....-0.3V to SYS + 0.3V  
 L1OUT .....-0.3V to L1IN + 0.3V  
 L2OUT .....-0.3V to L2IN + 0.3V  
 CPP ..... CPN – 0.3V to CPN + 6V  
 CPOUT ..... CPP – 0.3V to min(CPP + 6, +12)V  
 BSTHVLX, BSTOUT, LED0, LED1, LED2.....-0.3V to +22V

BSTHVLX to BSTOUT .....-22V to +0.1V  
 BBHVLX .....-0.3V to min (BBOUT + 0.3, +6)V  
 AGND, DGND, BK1GND, BK2GND, BSTGND,  
 HDGND, BBGND to GSUB .....-0.3V to +0.3V  
 Continuous Current into BAT, SYS.....-1000mA to +1000mA  
 Continuous Current into CHGIN..... -1mA to +1000mA  
 Continuous Current into DRP, DRN ..... -600mA to +600mA  
 Continuous Current into Any Other Terminal -100mA to +100mA  
 Continuous Power Dissipation (multilayer board  
 at +70°C): 7 x 8 Array 56-Ball, 3.71mm x  
 4.21mm, 0.5mm pitch WLP (derate 29.98mW/°C)....2399mW  
 Operating Temperature Range ..... -40°C to +85°C  
 Junction Temperature ..... +150°C  
 Storage Temperature Range ..... -65°C to +150°C  
 Lead Temperature (soldering, 10s) ..... +300°C  
 Soldering Temperature (reflow) .....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### Package Information

<b>PACKAGE TYPE: 56 WLP</b>	
Package Code	W563A4+1
Outline Number	<a href="#">21-100104</a>
Land Pattern Number	Refer to <a href="#">Application Note 1891</a>
<b>THERMAL RESISTANCE, FOUR-LAYER BOARD</b>	
Junction to Ambient ( $\theta_{JA}$ )	33.35°C/W

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>GLOBAL SUPPLY CURRENT</b>						
Charger Input Current	$I_{CHGIN}$	$V_{CHGIN} = +5V$ , On state, charger disabled, Buck1 enabled, no LDO enabled		1.3		mA
BAT Input Current	$I_{BAT}$	$V_{CHGIN} = 0V$ , Off state, LDO2 disabled		0.4		$\mu A$
		$V_{CHGIN} = 0V$ , Off state, LDO2 enabled, L2IN connected to BAT		1.6		
		$V_{CHGIN} = 0V$ , On state, all blocks disabled, Fuel Gauge off		2.4		
		$V_{CHGIN} = 0V$ , On state, Buck1 enabled, Fuel Gauge off		3.4		
		$V_{CHGIN} = 0V$ , On state, Buck1 and Buck2 enabled, Fuel Gauge off		3.9		
<b>INTERNAL SUPPLIES, BIAS, AND UVLOS</b>						
$V_{CCINTUVLO}$ Rising Threshold	$V_{VCCINT\_UVLO\_R}$	(Note 2)	2.25	2.45	2.75	V
$V_{CCINTUVLO}$ Falling Threshold	$V_{VCCINT\_UVLO\_F}$	(Note 2)	2.2	2.4	2.7	V
$V_{CCINTUVLO}$ Threshold Hysteresis	$V_{VCCINT\_UVLO\_H}$	(Note 2)		50		mV
Internal CAP Regulator	$V_{CAP}$	$V_{CHGIN} = +4.3V$ to $+28V$	3.75	4.1	4.55	V
CAPOK Rising Threshold	$V_{CAP\_OK\_R}$	$V_{CHGIN} = V_{CAP}$	3.15	3.4	3.6	V
CAPOK Falling Threshold	$V_{CAP\_OK\_F}$	$V_{CHGIN} = V_{CAP}$	2.6	2.8	3	V
CAPOK Threshold Hysteresis	$V_{CAP\_OK\_H}$			600		mV
$V_{BDET}$ Rising Threshold	$V_{CHGIN\_DET\_R}$		4	4.15	4.3	V
$V_{BDET}$ Falling Threshold	$V_{CHGIN\_DET\_F}$		3.2	3.3	3.4	V
$V_{BDET}$ Threshold Hysteresis	$V_{CHGIN\_DET\_H}$			850		mV
CHGIN Detection Debounce Time	$t_{CHGIN\_DET\_R}$	CHGIN insertion		28		ms
	$t_{CHGIN\_DET\_F}$	CHGIN detachment		20		
$V_{SYSUVLO}$ Rising Threshold	$V_{SYS\_UVLO\_R}$		2.65	2.75	2.85	V
$V_{SYSUVLO}$ Falling Threshold	$V_{SYS\_UVLO\_F}$		2.6	2.7	2.8	V
$V_{SYSUVLO}$ Threshold Hysteresis	$V_{SYS\_UVLO\_H}$			50		mV

### Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BATOC Rising Threshold	$I_{BAT\_OC\_R}$	From 200mA to 1A in 200mA steps, Device specific (See Table 192)	-40		+40	%
BATOC Threshold Hysteresis	$I_{BAT\_OC\_H}$			6		%
BATOC Rising Debounce Time	$t_{BAT\_OC\_D}$		9	10	11	ms
Internal $V_{DIG}$ Regulator	$V_{VDIG}$		1.68	1.8	2.0	V
$V_{DIGUVLO}$ Rising Threshold	$V_{VDIG\_UVLO\_R}$		1.61		1.71	V
$V_{DIGUVLO}$ Falling Threshold	$V_{VDIG\_UVLO\_F}$		1.51		1.61	V
$V_{DIGUVLO}$ Threshold Hysteresis	$V_{VDIG\_UVLO\_H}$			100		mV
<b>SFOUT</b>						
SFOUT LDO Voltage	$V_{SFOUT}$	SFOUTVSet = 0 (+5V), $V_{CHGIN} = +6V$ , $I_{SFOUT} = 0mA$	4.85	5	5.15	V
		SFOUTVSet = 0 (+5V), $V_{CHGIN} = +5V$ , $I_{SFOUT} = 15mA$		4.9		
		SFOUTVSet = 1 (+3.3V), $V_{CHGIN} = +5V$ , $I_{SFOUT} = 0mA$	3.15	3.3	3.45	
		SFOUTVSet = 1 (+3.3V), $V_{CHGIN} = +5V$ , $I_{SFOUT} = 15mA$		3.29		
SFOUT OVP Voltage	$V_{SFOUT\_OVP}$	SFOUT LDO is turned off above $V_{CHGIN\_OV\_R}$ threshold		$V_{CHGIN\_OV\_R}$		V
SFOUT Thermal Limit	$T_{SFOUT\_LIM}$			150		$^{\circ}C$
<b>SAR ADC AND MON</b>						
ADC Quiescent Current	$I_{ADC\_Q}$	Conversion running		30		$\mu A$
ADC SYS Divider Resistance	$R_{ADC\_SYS\_DIV}$	SYS conversion running		2.2		$M\Omega$
ADC MON Divider Resistance	$R_{ADC\_MON\_DIV}$	MON conversion running		2.2		$M\Omega$
ADC CHGIN Divider Resistance	$R_{ADC\_CHGIN\_DIV}$	CHGIN conversion running		1.1		$M\Omega$
ADC CPOUT Divider Resistance	$R_{ADC\_CPOUT\_DIV}$	CPOUT conversion running		0.82		$M\Omega$
ADC BSTOUT Divider Resistance	$R_{ADC\_BSTOUT\_DIV}$	BSTOUT conversion running		0.89		$M\Omega$
ADC SYS Least Significant Bit	$V_{ADC\_SYS\_LSB}$			21.57		mV

### Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOUT\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOUT} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC MON Least Significant Bit	$V_{ADC\_MON\_LSB}$			21.57		mV
ADC THM Least Significant Bit	$V_{ADC\_THM\_LSB}$			0.39		% $V_{DIG}$
ADC CHGIN Least Significant Bit	$V_{ADC\_CHGIN\_LSB}$			32.35		mV
ADC CPOUT Least Significant Bit	$V_{ADC\_CPOUT\_LSB}$			32.35		mV
ADC BSTOUT Least Significant Bit	$V_{ADC\_BSTOUT\_LSB}$			82.35		mV
ADC SYS Absolute Sensing Worst-Case Accuracy	$V_{ADC\_SYS\_ACC}$	$V_{SYS} = +2.6V$	-75		+75	mV
		$V_{SYS} = +5.5V$	-133		+133	
ADC MON Absolute Sensing Worst-Case Accuracy	$V_{ADC\_MON\_ACC}$	$V_{MON} = +1.0V$	-46		+46	mV
		$V_{MON} = +5.5V$	-133		+133	
ADC THM Percentage Sensing Worst-Case Accuracy	$V_{ADC\_THM\_ACC}$	$V_{THM} = (5 \text{ to } 95)\%V_{DIG}$	-1.789		+1.789	% $V_{DIG}$
ADC CHGIN Absolute Sensing Worst-Case Accuracy	$V_{ADC\_CHGIN\_ACC}$	$V_{CHGIN} = +3.0V$	-94		+94	mV
		$V_{CHGIN} = +8.0V$	-193		+193	
ADC CPOUT Absolute Sensing Worst-Case Accuracy	$V_{ADC\_CPOUT\_ACC}$	$V_{CPOUT} = +5.0V$	-133		+133	mV
		$V_{CPOUT} = +6.6V$	-165		+165	
ADC BSTOUT Absolute Sensing Worst-Case Accuracy	$V_{ADC\_BSTOUT\_ACC}$	$V_{BSTOUT} = +3.0V$	-161		+161	mV
		$V_{BSTOUT} = +21.0V$	-503		+503	
ADC Conversion Time	$t_{ADC\_CONV}$	1.1ms (typ) additional delay prior to each 1 <sup>st</sup> conversion.		83		$\mu s$
THM Input Leakage	$I_{LK\_THM}$		-1		+1	$\mu A$
TPU Switch Resistance	$R_{TPU\_SW}$	1mA max load on TPU		4		$\Omega$
MON Multiplexer Output Ratio	$V_{MON\_DIV\_RT}$	No load on MON pin. Inputs: BAT, SYS, BK1OUT, BK2OUT, L1OUT, L2OUT, SFOUT, BBOUT	MonRatioCfg = 00		100	%
			MonRatioCfg = 01		50	
			MonRatioCfg = 10		33.33	
			MonRatioCfg = 11		25	

### Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOUT\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOUT} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MON Multiplexer Output Impedance	$R_{MON\_DIV}$	100 $\mu A$ load on MON pin. Inputs: BAT, SYS, BK2OUT, BK1OUT, L2OUT, L1OUT, SFOUT, BBOUT	MonRatioCfg = 00		5.5		k $\Omega$
		No load on MON pin. Inputs: BAT, SYS, BK2OUT, BK1OUT, L2OUT, L1OUT, SFOUT, BBOUT	MonRatioCfg = 01		31		
			MonRatioCfg = 10		28		
			MonRatioCfg = 11		24		
MON Multiplexer Off State Pulldown Resistance	$R_{MON\_OFF\_PD}$	MON disabled, pulldown resistance enabled			59		k $\Omega$
<b>OVP AND INPUT CURRENT LIMITER</b>							
Allowed CHGIN Input Voltage Range	$V_{CHGIN\_RNG}$			-5.5		+28	V
CHGIN Overvoltage Rising Threshold	$V_{CHGIN\_OV\_R}$	SFOUT LDO is turned off above this threshold		7.2	7.5	7.8	V
CHGIN Overvoltage Threshold Hysteresis	$V_{CHGIN\_OV\_H}$				200		mV
CHGIN Valid Trip Point	$V_{CHGN\_SYS\_TP}$	$V_{CHGIN} - V_{SYS}$		30	145	290	mV
CHGIN Valid Trip Point Hysteresis	$V_{CHGIN\_SYS\_TP\_HYS}$				275		mV
Input Overcurrent Max Limit ( $t < t_{ILIM\_BLANK}$ )	$I_{LIM\_MAX}$	ILimMax = 0/1, device specific (see Table 192)			450/1000		mA
Input Current Limit ( $t > t_{ILIM\_BLANK}$ )	$I_{LIM}$	ILimCnt = 000			50		mA
		ILimCnt = 001			90		
		ILimCnt = 010			150		
		ILimCnt = 011			200		
		ILimCnt = 100			300		
		ILimCnt = 101			400		
		ILimCnt = 110			450		
		ILimCnt = 111			1000		



### Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOUT\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOUT} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current Limit Blanking Time	$t_{LIM\_BLANK}$	ILimBlank = 00		0.003		ms
		ILimBlank = 01		0.5		
		ILimBlank = 10		1		
		ILimBlank = 11		10		
SYS Regulation Voltage	$V_{SYS\_REG}$		$V_{BAT\_REG} + 0.14$	$V_{BAT\_REG} + 0.2$	$V_{BAT\_REG} + 0.26$	V
SYS Regulation Voltage Dropout	$V_{CHGIN\_SYS}$			40		mV
CHGIN to SYS On-Resistance	$R_{CHGIN\_SYS}$			0.37	0.66	$\Omega$
Input Current Soft-Start Time	$I_{LIM\_SFT}$			1		ms
Thermal Shutdown Temperature	$T_{CHGIN\_SHDN}$	Future option		50		$^{\circ}C$
				60		
				70		
				80		
				90		
				100		
		MAX20303A,B,C,D	120			
Thermal Shutdown Timeout	$T_{CHGIN\_SHDN\_TO}$	TShdnTmo = 01		0.5		s
		TShdnTmo = 10		1		
		TShdnTmo = 11		5		
<b>BATTERY CHARGER</b>						
BAT to SYS On Resistance	$R_{BAT\_SYS}$	$V_{BAT} = 4.2V$ , $I_{BAT} = 300mA$		80	140	m $\Omega$
Thermal Regulation Temperature	$T_{CHG\_LIM}$			$T_{CHGIN\_SHDN} - 3$		$^{\circ}C$
BAT-to-SYS Switch On Threshold	$V_{BAT\_SYS\_ON}$	SYS falling	10	22	35	mV
BAT-to-SYS Switch Off Threshold	$V_{BAT\_SYS\_OFF}$	SYS rising	-3	-1.5	0	mV
SYS-BAT Charge Current Reduction Threshold	$V_{SYS\_BAT\_LIM}$	Measured as $V_{SYS} - V_{BAT}$ , SysMinVlt = 000, $V_{BAT} > 3.6V$		100		mV

### Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Minimum SYS Voltage	$V_{SYS\_LIM}$	$V_{BAT} < 3.4V$	SysMinVlt = 000		3.6		V
			SysMinVlt = 001		3.7		
			SysMinVlt = 010		3.8		
			SysMinVlt = 011		3.9		
			SysMinVlt = 100		4.0		
			SysMinVlt = 101		4.1		
			SysMinVlt = 110		4.2		
			SysMinVlt = 111		4.3		
Charger Current Soft-Start Time	$t_{CHG\_SOFT}$			1		ms	
Precharge Current	$I_{PCHG}$	IPChg = 00		5		%I <sub>FCHG</sub>	
		IPChg = 01	9	10	11		
		IPChg = 10		20			
		IPChg = 11		30			
Precharge Threshold	$V_{BAT\_PCHG}$	VPChg = 000		2.1		V	
		VPChg = 001		2.25			
		VPChg = 010		2.4			
		VPChg = 011		2.55			
		VPChg = 100		2.7			
		VPChg = 101		2.85			
		VPChg = 110		3			
		VPChg = 111		3.15			
Precharge Threshold Hysteresis	$V_{BAT\_PCHG\_HYS}$			90		mV	
SET Current Gain Factor	$K_{SET}$			2000		A/A	
SET Regulation Voltage	$V_{SET}$			1		V	
BAT Charge Current Set Range	$I_{FCHG}$	$R_{SET} = 400k\Omega$		5		mA	
		$R_{SET} = 40k\Omega$	45	50	55		
		$R_{SET} = 4k\Omega$		500			

### Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Battery Regulation Voltage	$V_{BAT\_REG}$	BatReg = 0000		4.05		V
		BatReg = 0001		4.10		
		BatReg = 0010		4.15		
		BatReg = 0011, $T_A = 25^{\circ}C$	4.179	4.20	4.221	
		BatReg = 0011	4.158	4.20	4.242	
		BatReg = 0100		4.25		
		BatReg = 0101		4.30		
		BatReg = 0110		4.35		
		BatReg = 0111		4.40		
		BatReg = 1000		4.45		
		BatReg = 1001		4.50		
		BatReg = 1010		4.55		
BatReg = 1011		4.60				
Battery Recharge Threshold	$V_{BAT\_RECHG}$	BatReChg = 00		70		mV
		BatReChg = 01		120		
		BatReChg = 10		170		
		BatReChg = 11		220		
Maximum Precharge Time	$t_{PCHG}$	PChgTmr = 00		30		min
		PChgTmr = 01		60		
		PChgTmr = 10		120		
		PChgTmr = 11		240		
Maximum Fast Charge Time	$t_{FCHG}$	FChgTmr = 00		75		min
		FChgTmr = 01		150		
		FChgTmr = 10		300		
		FChgTmr = 11		600		
Charge Done Qualification	$I_{CHG\_DONE}$	ChgDone = 00		5		%I <sub>FCHG</sub>
		ChgDone = 01	8.5	10	11.5	
		ChgDone = 10		20		
		ChgDone = 11		30		
Timer Accuracy	$t_{CHG\_ACC}$		-10		10	%
Timer Extend Threshold (1/2 Fast Charge Current Comparator)	$t_{CHG\_EXT}$	See Figure 5		50		%I <sub>FCHG</sub>

### Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOUT\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOUT} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Timer Suspend Threshold (1/5 Fast Charge Current Comparator)	$t_{CHG\_SUS}$	See Figure 5		20		% $I_{FCHG}$
THM Percentage Sensing Worst Case Accuracy	$V_{ADC\_THM\_ACC}$	$V_{THM} = (5 \text{ to } 95)\%V_{DIG}$		see ADC section		
Cool/Cold Threshold Hysteresis		Falling, $LSB = 0.39\%V_{DIG}$		0 to 31		LSB
Warm/Hot Threshold Hysteresis		Rising, $LSB = 0.39\%V_{DIG}$		0 to 31		LSB
Battery Regulation Voltage Reduction Due to Battery Pack Temperature	$V_{BAT\_REG\_RED}$	Cold/Cool/Room/Warm/ HotBatReg = 00		BatReg – 150mV		V
		Cold/Cool/Room/Warm/ HotBatReg = 01		BatReg – 100mV		
		Cold/Cool/Room/Warm/ HotBatReg = 10		BatReg – 50mV		
		Cold/Cool/Room/Warm/ HotBatReg = 11		BatReg		
Fast Charge Current Reduction Due to Battery Pack Temperature	$I_{FCHG\_FACT}$	Cold/Cool/Room/Warm/ HotFChg = 000		$I_{FCHG} \times 0.2$		mA
		Cold/Cool/Room/Warm/ HotFChg = 001		$I_{FCHG} \times 0.3$		
		Cold/Cool/Room/Warm/ HotFChg = 010		$I_{FCHG} \times 0.4$		
		Cold/Cool/Room/Warm/ HotFChg = 011		$I_{FCHG} \times 0.5$		
		Cold/Cool/Room/Warm/ HotFChg = 100		$I_{FCHG} \times 0.6$		
		Cold/Cool/Room/Warm/ HotFChg = 101		$I_{FCHG} \times 0.7$		
		Cold/Cool/Room/Warm/ HotFChg = 110		$I_{FCHG} \times 0.8$		
		Cold/Cool/Room/Warm/ HotFChg = 111		$I_{FCHG}$		
BAT UVLO Threshold	$V_{BAT\_UVLO}$		1.9	2.05	2.2	V
BAT UVLO Threshold Hysteresis	$V_{BAT\_UVLO\_HYS}$			50		mV

## Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>BUCK1</b>						
Input Voltage Range	$V_{BK1IN}$	Input voltage = $V_{SYS}$	2.7		5.5	V
Output Voltage Range	$V_{BK1OUT}$	25mV step resolution	0.8		2.375	V
Output Voltage UVLO	$V_{UVLO\_BK1}$				0.65	V
Quiescent Supply Current	$I_{Q\_BK1}$	$I_{BK1OUT} = 0$ , $V_{SYS} = +3.7V$ , $V_{BK1OUT} = +1.2V$		0.8	1.3	$\mu A$
Dropout Quiescent Supply Current	$I_{Q\_DO\_BK1}$	$I_{BK1OUT} = 0$ , $V_{SYS} - V_{BK1OUT} \leq +0.1V$		250		$\mu A$
Shutdown Supply Current with Active Discharge Enabled	$I_{SD\_BK1}$	Buck 1 disabled, Buck1ActDsc = 1		60		$\mu A$
Output Average Voltage Accuracy	$ACC\_BK1$	$I_{BK1OUT} = 1mA$	-3.2		+2.9	%
Peak-to-Peak Ripple	$V_{RPP\_BK1}$	Buck1ISet = 0100 (100mA), $C_{BK1OUT\_EFF} = 2.2\mu F$ , $I_{BK1OUT} = 1mA$		10		mV
Peak Current Set Range	$I_{PSET\_BK1}$	25mA step resolution. The accuracy of codes below 50mA is limited by $t_{ON\_MIN\_BK1}$	0		375	mA
Load Regulation Error	$V_{LOAD\_REG\_BK1}$	Buck1ISet = 0110 (150mA), Buck1IAdptEn = 1, $I_{BK1OUT} = 300mA$		-3		%
Line Regulation Error	$V_{LINE\_REG\_BK1}$	$V_{BK1OUT} = +1.2V$ , $V_{SYS}$ from +2.7V to +5.5V		2		mV
Maximum Operative Output Current	$I_{BK1\_MAX}$	$V_{SYS} = +3.7V$ , Buck1VSet = 0x10 (+1.2V), Buck1ISet = 1000 (200mA), Buck1IAdptEn = 1, load regulation error = -5%	220			mA
BK1OUT Pulldown Current	$I_{PD\_BK1\_E}$	Buck 1 Enabled		100	200	nA
BK1OUT Pulldown Resistance with Buck Disabled	$I_{PD\_BK1\_D}$	Buck 1 Disabled, $V_{SYS} = +3.6V$ , Buck1VSet = 0x10 (+1.2V)		12		M $\Omega$
PMOS On-Resistance	$R_{P\_ON\_BK1}$	Buck1FETScale = 0		0.35	0.49	$\Omega$
	$R_{P\_ON\_BK1\_FS}$	Buck1FETScale = 1		0.7	0.98	
NMOS On-Resistance	$R_{N\_ON\_BK1}$	Buck1FETScale = 0		0.25	0.4	$\Omega$
	$R_{N\_ON\_BK1\_FS}$	Buck1FETScale = 1		0.5	0.7	
Freewheeling On-Resistance	$R_{ON\_BK1\_FRWHL}$	$V_{SYS} = +3.7V$ , Buck1VSet = 0x10 (+1.2V)		7	12	$\Omega$

## Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum $t_{ON}$	$t_{ON\_MIN\_BK1}$			60	90	ns
Maximum Duty Cycle	$D\_MAX\_BK1$	Buck1IAdptEn = 1		95		%
Switching Frequency	$FREQ\_BK1$	Load regulation error = -5%		3		MHz
Average Current During Short-Circuit to GND	$I_{SHRT\_BK1}$	Buck1ISet = 0110 (150mA), Buck1IAdptEn = 1, $V_{BK1OUT} = 0V$		100		mA
BK1LX Leakage Current	$I_{LK\_BK1LX}$	Buck 1 disabled			1	$\mu A$
Active Discharge Current	$I_{ACTD\_BK1}$	$V_{BK1OUT} = +1.2V$	8	19	35	mA
Passive Discharge Resistance	$R_{PSV\_BK1}$			10		k $\Omega$
Full Turn-On Time	$t_{ON\_BK1}$	Time from enable to full current capability		58		ms
Efficiency	$EFFIC\_BK1$	Buck1VSet = 0x10 (+1.2V), $I_{BK1OUT} = 10mA$ , Buck1ISet = 0111 (175mA), Inductor: Murata DFE201610E-2R2M		88.5		%
BK1LX Rising/Falling Slew Rate	$SLW\_BK1$	Buck1LowEMI = 0		2		V/ns
	$SLW\_BK1\_L$	Buck1LowEMI = 1		0.5		
Thermal Shutdown Threshold	$T_{SHDN\_BK1}$			140		$^{\circ}C$
<b>BUCK2</b>						
Input Voltage Range	$V_{BK2IN}$	Input voltage = $V_{SYS}$	2.7		5.5	V
Output Voltage Range	$V_{BK2OUT}$	50mV step resolution	0.8		3.95	V
Output Voltage UVLO	$V_{UVLO\_BK2}$				0.65	V
Quiescent Supply Current	$I_{Q\_BK2}$	$I_{BK2OUT} = 0mA$ , $V_{SYS} = +3.7V$ , Buck2VSet = 0x08 (+1.2V)		0.9	1.4	$\mu A$
Dropout Quiescent Supply Current	$I_{Q\_DO\_BK2}$	$I_{BK2OUT} = 0mA$ , $V_{SYS} - V_{BK2OUT} \leq +0.1V$		250		$\mu A$
Shutdown Supply Current with Active Discharge Enabled	$ISD\_BK2$	Buck 2 disabled, Buck2ActDsc = 1		60		$\mu A$
Output Average Voltage Accuracy	$ACC\_BK2$	$I_{BK2OUT} = 1mA$ , Buck2VSet $\leq 0x34$ (+3.4V)	-3.2		+2.9	%
Peak-to-Peak Ripple	$V_{RPP\_BK2}$	Buck2ISet = 0100 (100mA), $C_{BK2OUT\_EFF} = 2.2\mu F$ , $I_{BK2OUT} = 1mA$		10		mV
Peak Current Set Range	$I_{PSET\_BK2}$	25mA step resolution. The accuracy of codes below 50mA is limited by $t_{ON\_MIN\_BK2}$	0		375	mA

## Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Load Regulation Error	$V_{LOAD\_REG\_BK2}$	Buck2ISet = 0110 (150mA), Buck2IAdptEn = 1, $I_{BK2OUT} = 300mA$		-3		%
Line Regulation Error	$V_{LINE\_REG\_BK2}$	$V_{BK2OUT} = +1.2V$ , $V_{SYS}$ from +2.7V to +5.5V		2		mV
Maximum Operative Output Current	$I_{BK2\_MAX}$	$V_{SYS} = +3.7V$ , Buck2VSet = 0x08 (+1.2V), Buck2ISet = 1000 (200mA), Buck2IAdptEn = 1, load regulation error = -5%	220			mA
BK2OUT Pulldown Current	$I_{PD\_BK2\_E}$	Buck 2 enabled		200	400	nA
BK2OUT Pulldown Resistance with Buck Disabled	$I_{PD\_BK2\_D}$	Buck 2 disabled, $V_{SYS} = +3.6V$ , Buck2VSet = 0x10 (+1.2V)		8		MΩ
PMOS On-Resistance	$R_{P\_ON\_BK2}$	Buck2FETScale = 0		0.35	0.49	Ω
	$R_{P\_ON\_BK2\_FS}$	Buck2FETScale = 1		0.7	0.98	
NMOS On-Resistance	$R_{N\_ON\_BK2}$	Buck2FETScale = 0		0.25	0.4	Ω
	$R_{N\_ON\_BK2\_FS}$	Buck2FETScale = 1		0.5	0.7	
Freewheeling On-Resistance	$R_{ON\_BK2\_FRWHL}$	$V_{SYS} = +3.7V$ , Buck2VSet = 0x08 (+1.2V)		7	12	Ω
Minimum $t_{ON}$	$t_{ON\_MIN\_BK2}$			60	90	ns
Maximum Duty Cycle	$D\_MAX\_BK2$	Buck2IAdptEn = 1		95		%
Switching Frequency	$FREQ\_BK2$	Load regulation error = -5%		3		MHz
Average Current During Short-Circuit to GND	$I_{SHRT\_BK2}$	Buck2ISet = 0110 (150mA), Buck2IAdptEn = 1, $V_{BK2OUT} = 0V$		100		mA
BK2LX Leakage Current	$I_{LK\_BK2LX}$	Buck 2 disabled			1	μA
Active Discharge Current	$I_{ACTD\_BK2}$	$V_{BK2OUT} = +1.2V$	8	19	35	mA
Passive Discharge Resistance	$R_{PSV\_BK2}$			10		kΩ
Full Turn-On Time	$t_{ON\_BUCK2}$	Time from enable to full current capability		58		ms
Efficiency	$EFFIC\_BK2$	Buck2VSet = 0x08 (+1.2V), $I_{BK2OUT} = 10mA$ , Buck2ISet = 0111 (175mA), Inductor: Murata DFE201610E-2R2M		88.5		%
BK2LX Rising/Falling Slew Rate	$SLW\_BK2$	Buck2LowEMI = 0		2		V/ns
	$SLW\_BK2\_L$	Buck2LowEMI = 1		0.5		
Thermal Shutdown Threshold	$T_{SHDN\_BK2}$			140		°C

## Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>HVBOOST</b>						
Input Voltage Range	$V_{BSTIN}$	Input voltage = $V_{SYS}$	2.7		5.5	V
Output Voltage Range	$V_{BSTOUT}$	250mV step resolution	5		20	V
Output Voltage UVLO	$V_{BSTOUT\_UVLO}$	$V_{BSTOUT} - V_{SYS}$	-2.7	-2.2	-1.6	V
Quiescent Supply Current	$I_{Q\_BST}$	$I_{BSTOUT} = 0mA$ , $V_{SYS} = +3.7V$ , $BstVSet = 0x00 (+5V)$ , $T_A = 25^{\circ}C$		2.4	9	$\mu A$
		$I_{BSTOUT} = 0mA$ , $V_{SYS} = +3.7V$ , $BstVSet = 0x00 (+5V)$			106	
Output Average Voltage Accuracy	$ACC\_BST$	$I_{BSTOUT} = 1mA$ , $HVOUT < 13V$	-4		+2	%
Peak-to-Peak Ripple	$V_{RPP\_BST}$	$BstISet = 0x0A (350mA)$ , $BstVSet = 0x1C (+12V)$ , $C_{BSTOUT\_EFF} = 10\mu F$ , $L = 4.7\mu H$ , $I_{BSTOUT} = 1mA$		5		mV
Peak Current Set Range	$I_{PSET\_BST}$	25mA step resolution	100		475	mA
DC Load Regulation Error	$V_{LOAD\_REG\_BST}$	$BstVSet = 0x1C (+12V)$ , $I_{BSTOUT} = 25mA$ , $BstISet = 0x08 (300mA)$ , $BstIAdptEn = 1$		0.3		%
DC Line Regulation Error	$V_{LINE\_REG\_BST}$	$BstVSet = 0x06 (+6.5V)$ , $V_{SYS}$ from $+2.7V$ to $+5.5V$		4		mV
Maximum Operative Output Power	$P_{MAX\_BST}$	$BstISet = 0x08 (300mA)$ , $BstIAdptEn = 1$	300	700		mW
BSTOUT Pulldown Resistance	$R_{BSTOUT}$	-3% Load Reg Error		10		$M\Omega$
True Shutdown PMOS On-Resistance	$R_{ON\_TS}$	$I_{BSTOUT} = 100mA$		0.15	0.22	$\Omega$
Boost Freewheeling NMOS On-Resistance	$R_{N\_ONFRW\_N}$	$I_{BSTOUT} = 100mA$		0.45	0.7	$\Omega$
Boost NMOS On-Resistance	$R_{ONBST\_N}$	$BstFETScale = 0$ , $I_{BSTOUT} = 100mA$		0.55	0.9	$\Omega$
	$R_{ONBST\_NFS}$	$BstFETScale = 1$ , $I_{BSTOUT} = 100mA$		1.1	1.8	
Schottky Diode Forward Voltage	$V_{BE\_SCHOTTKY}$	$I_{BSTOUT} = 100mA$ , $V_{BSTHV LX} - V_{BSTOUT}$	0.2	0.4	0.6	V
Freewheeling On-Resistance	$R_{ONBST\_FRWHL}$	$I_{BSTOUT} = 100mA$		50	80	$\Omega$
Minimum $t_{ON}$	$t_{ON\_BST\_MIN}$			65		ns



## Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOUT\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOUT} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Max Switching Frequency	FREQ_BST_MX	$V_{BSTOUT}$ regulation error = -150mV. BstISet = 100mA, BstIAdptEn = 0.	1.7	3.5	5.5	MHz
Max Peak Current Setting Extra Budget with BstIAdptEn = 1	$\Delta I_{P\_MAX}$	BstIAdptEn = 1, $V_{BSTOUT}$ regulation error = -200mV	150	250	450	mA
Short-Circuit Current Limit Difference vs. Peak Current Setting	$\Delta I_{BST\_SHRT}$	BstIAdptEn = 0	130	200	250	mA
BSTHVLX Leakage Current	$I_{LK\_BSTHVLX}$	Boost disabled			1	$\mu A$
BSTLVLX Leakage Current	$I_{LK\_BSTLVLX}$	Boost disabled			1	$\mu A$
Passive Discharge Resistance	$R_{BSTPSV}$			10		k $\Omega$
Linear BSTOUT Precharge Current	$I_{L\_BSTOUT\_PRCH}$	$V_{BSTOUT}$ from 0 to $V_{SYS} - 0.4V$	5	12.5	20	mA
Switching Precharge Inductor Current	$I_{SW\_BSTOUT\_PRCH}$	$V_{BSTOUT}$ from $V_{SYS} - 0.4V$ to final regulation voltage		13		mA
Full Turn-On Time	$t_{ON\_BST}$	Time from enable to full current capability		100		ms
Efficiency	EFFIC_12	BstVSet = 0x1C (+12V), $I_{BSTOUT} = 20mA$ , BstISet = 0x08 (300mA), Inductor: Murata DFE201610E-4R7M		85		%
	EFFIC_15	BstVSet = 0x28 (+15V), $I_{BSTOUT} = 2mA$ , BstISet = 0x08 (300mA), Inductor: Murata DFE201610E-4R7M		83		
	EFFIC_5	BstVSet = 0x00 (+5V), $I_{BSTOUT} = 10\mu A$ , BstISet = 0x02 (150mA), Inductor: Murata DFE201610E-4R7M		76		
	EFFIC_6P5	BstVSet = 0x06 (+6.5V), $I_{BSTOUT} = 10\mu A$ , BstISet = 0x02 (150mA), Inductor: Murata DFE201610E-4R7M		73		
BHVLX Rising/Falling Slew Rate	SLW_BST_HVLX			2		V/ns
Thermal Shutdown Threshold	$T_{SHDN\_BST}$			125		$^{\circ}C$

## Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>BUCK-BOOST</b>						
Input Voltage Range	$V_{BBIN}$	Input voltage = $V_{SYS}$	2.7		5.5	V
Quiescent Supply Current	$I_{Q\_BB}$	$I_{BBOU} = 0\mu A$ , $V_{BBOU} = +4V$		1.3	2.1	$\mu A$
Maximum Output Operative Power	$P_{MAX\_BBOU}$	$V_{SYS} > +3V$	250			mW
Output Voltage Set Range	$V_{BBOU}$	100mV step	2.5		5	V
Average Output Voltage Accuracy	$ACC\_BBOU$	$I_{BBOU} = 1mA$ , $C_{BBOU\_EFF} \geq 10\mu F$	-3		3	%
Line Regulation Error	$V_{LINE\_REG\_BB}$	$V_{SYS} = +2.7V$ to $+5.5V$ , $I_{BBOU} = 10\mu A$ , $BBstVSet = 0x0F (+4V)$ , $BBstISet = 0x02 (100mA)$	-1	+0.3	+1	%/V
Load Regulation Error	$V_{LOAD\_REG\_BB}$	$BBstVSet = 0x0F (+4V)$ , $I_{BBOU} = 10\mu A$ to $50mA$ , $BBstISet = 0x02 (100mA)$		100		mV/A
		$BBstVSet = 0x0F (+4V)$ , $I_{BBOU} = 10\mu A$ to $100mA$ , $BBstISet = 0x02 (100mA)$		310		
Line Transient	$V_{LINE\_TRAN\_BB}$	$BBstVSet = 0x0F (+4V)$ , $BBstISet = 0x02 (100mA)$ , $V_{SYS}$ from $+2.7V$ to $+5V$ , $0.2\mu s$ rise time		15		mV
Load Transient	$V_{LOAD\_TRAN\_BB}$	$I_{BBOU} = 0mA$ to $10mA$ , $200ns$ rise time, $BBstVSet = 0x0F (+4V)$ , $BBstISet = 0x02 (100mA)$		9		mV
		$I_{BBOU} = 0mA$ to $100mA$ , $200ns$ rise time, $V_{BBOU} = +4V$ , $BBstISet = 0x02 (100mA)$		31		
Oscillator Frequency	$f_{OSC\_BB}$		1.8	2	2.2	MHz
Output FETs $R_{ON}$	$R_{ON\_PBK\_BB}$	High-side PMOS Buck FET	0.15		0.22	$\Omega$
	$R_{ON\_NBK\_BB}$	Low-side NMOS Buck FET		0.22	0.36	
	$R_{ON\_PBST\_BB}$	High-side PMOS Boost FET ( $V_{BBOU} = +4V$ )		0.21	0.31	
	$R_{ON\_NBST\_BB}$	Low-side NMOS Boost FET		0.24	0.4	
	$R_{ON\_FRWH\_BB}$	EMI improve FET between $BBHVLX/$ $BBLVLX$		8	11	
Passive Discharge Pulldown Resistance	$R_{PDL\_BB}$	$BBstPasDsc = 1$		10		k $\Omega$
Active Discharge Current	$I_{ACTDL\_BB}$	$BBstActDsc = 1$ , $V_{BBOU} = +1.5V$	6	19	38	mA

## Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOUT\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOUT} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Time	$t_{ON\_BB}$	Time from enable to full current capability		100		ms
UVLO On BBOUT	$V_{BBOUT\_UVLO}$		1.65	1.75	1.9	V
Precharge Current	$I_{PC\_BB}$	Precharge current. $V_{SYS} = +2.7V$ , $V_{BBOUT} = +1.65V$	6	14	24	mA
Pulse Mode Input Current Limit	$I_{PLS\_IN}$	$BBstVSet = 0x0F (+4V)$ , $V_{SYS} < V_{BBOUT} - 0.5V$ , $f_{SW} = f_{OSC\_BBST}/10$ , $BBstSet = 0x02 (100mA)$		6.6		mA
Pulse Mode Switching Period Ratio	$T\_RATIO$	$f_{OSC\_BB}/f_{SW}$ 128 steps	10		138	
Average Current During Short-Circuit to GND	$I_{SHRT\_BB}$	$V_{BBOUT} = 0V$	0.4	0.75	1.1	A
Thermal Shutdown Threshold	$T_{SHDN\_BB}$	$T_J$ rising		150		$^{\circ}C$
Thermal Shutdown Hysteresis	$T_{SHDN\_HYST\_BB}$				10	$^{\circ}C$
<b>LDO1 (Typical values are at <math>V_{L1IN} = +1.2V</math>, <math>V_{L1OUT} = +1V</math>)</b>						
Input Voltage Range	$V_{L1IN}$	LDO mode	1.16		2	V
		Switch mode	0.7		2	
Quiescent Supply Current	$I_{Q\_L1}$	$I_{L1OUT} = 0\mu A$		1	2.1	$\mu A$
		$I_{L1OUT} = 0\mu A$ , Switch mode		0.35	0.7	
Output Leakage	$I_{LK\_L1OUT}$	$V_{L1OUT} = GND$ , LDO 1 disabled		0.015	2.5	$\mu A$
Quiescent Supply Current in Dropout	$I_{Q\_L1\_DRP}$	$I_{L1OUT} = 0\mu A$ , $V_{L1IN} = +1.2V$ , $LDO1VSet = 0x1D (+1.225V)$		2.4	4.2	$\mu A$
Maximum Output Current	$I_{L1OUT\_MAX}$		50			mA
Output Voltage	$V_{L1OUT}$	25mV step resolution	0.5		1.95	V
Output Accuracy	$ACC\_LDO1$	$(V_{L1OUT} + 0.2V) \leq V_{L1IN} \leq +2V$ , $I_{L1OUT} = 1mA$	-3.4		+3.9	%
Dropout Voltage	$V_{DRP\_L1}$	$V_{L1IN} = +1V$ , $LDO1VSet = 0x14 (+1V)$ , $I_{L1OUT} = 50mA$			63	mV
Line Regulation Error	$V_{LINE\_REG\_L1}$	$V_{L1IN} = (V_{L1OUT} + 0.2V)$ to $+2V$	-0.5		+0.5	%/V
Load Regulation Error	$V_{LOAD\_REG\_L1}$	$+1V \leq V_{L1IN} \leq +2V$ , $I_{L1OUT} = 100\mu A$ to $50mA$		0.003	0.013	%/mA
Line Transient	$V_{LINE\_TRAN\_L1}$	$V_{L1IN} = +1V$ to $+2V$ , 200ns rise time		$\pm 45$		mV
		$V_{L1IN} = +1V$ to $+2V$ , 1 $\mu s$ rise time		$\pm 25$		
Load Transient	$V_{LOAD\_TRAN\_L1}$	$I_{L1OUT} = 0$ to $10mA$ , 200ns rise time		80		mV
		$I_{L1OUT} = 0$ to $50mA$ , 200ns rise time		130		

## Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS		
Passive Discharge Resistance	$R_{PDL\_L1}$			5	10	15	k $\Omega$		
Active Discharge Current	$I_{ACTDL\_L1}$			7	25	55	mA		
Switch Mode On-Resistance	$R_{ON\_L1}$	Switch mode	$V_{L1IN} = +1V$ , $I_{L1OUT} = 50mA$			1.02	$\Omega$		
			$V_{L1IN} = +0.7V$ , $I_{L1OUT} = 1mA$			2.7			
Turn-On Time	$t_{ON\_L1}$	$I_{L1OUT} = 0mA$ , time from 10% to 90% of LDO1VSet				0.38	ms		
		$I_{L1OUT} = 0mA$ , time from 10% to 90% of $V_{L1IN}$ , Switch mode				0.065			
Short Circuit Current Limit	$I_{SHRT\_L1}$	$V_{L1IN} = +1.2V$ , $V_{L1OUT} = 0V$		165	310	405	mA		
		$V_{L1IN} = +1.2V$ , $V_{L1OUT} = 0V$ , Switch mode		160	305	400			
Thermal Shutdown Temperature	$T_{SHDN\_L1}$	$T_J$ rising				150	$^{\circ}C$		
Thermal Shutdown Temperature Hysteresis	$T_{SHDN\_HYS\_L1}$					20	$^{\circ}C$		
Output Noise		10Hz to 100kHz, $V_{L1IN} = +2V$	$V_{L1OUT} = +1.8V$			120	$\mu V_{RMS}$		
			$V_{L1OUT} = +1V$			95			
			$V_{L1OUT} = +0.5V$			70			
UVLO	$V_{L1IN\_UVLO\_F}$	$V_{L1IN}$ falling		0.53	0.77	V			
	$V_{L1IN\_UVLO\_R}$	$V_{L1IN}$ rising						0.78	1
<b>LDO2 (Typical values at <math>V_{L2IN} = +3.7V</math>, <math>V_{L2OUT} = +3V</math>)</b>									
Input Voltage Range	$V_{L2IN}$	LDO mode		1.71			5.5	V	
		Switch mode				1.2	5.5		
Quiescent Supply Current	$I_{Q\_L2}$	$I_{L2OUT} = 0\mu A$				1	1.7	$\mu A$	
		$I_{L2OUT} = 0\mu A$ , Switch mode.				0.35	0.7		
Quiescent Supply Current in Dropout	$I_{Q\_L2\_DRP}$	$I_{L2OUT} = 0\mu A$ , $V_{L2IN} = +2.9V$ , LDO2VSet = 0x15 (+3V)				2.2	3.7	$\mu A$	
Maximum Output Current	$I_{L2OUT\_MAX}$	$V_{L2IN} > +1.8V$				100	mA		
Output Voltage	$V_{L2OUT}$	100mV step resolution				0.9	4	V	
Output Accuracy	ACC_LDO2	$(V_{L2OUT} + 0.5V) \leq V_{L2IN} \leq +5.5V$ , $I_{L2OUT} = 1mA$				-2.9	+2.9	%	
Dropout Voltage	$V_{DRP\_L2}$	$V_{L2IN} = +3V$ , LDO2VSet = 0x16 (+3.1V), $I_{L2OUT} = 100mA$						100	mV
		$V_{L2IN} = +1.85V$ , LDO2VSet = 0x0A (+1.9V), $I_{L2OUT} = 100mA$						130	mV

### Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line Regulation Error	$V_{LINE\_REG\_L2}$	$V_{L2IN} = (V_{L2OUT} + 0.5V)$ to $+5.5V$		-0.38		+0.38	%/V
Load Regulation Error	$V_{LOAD\_REG\_L2}$	$+1.8V \leq V_{L2IN} \leq +5.5V$ $I_{L2OUT} = 100\mu A$ to $100mA$			0.002	0.005	%/mA
Line Transient	$V_{LINE\_TRAN\_L2}$	$V_{L2IN} = +4V$ to $+5V$ , 200ns rise time			$\pm 35$		mV
		$V_{L2IN} = +4V$ to $+5V$ , 1 $\mu s$ rise time			$\pm 25$		
Load Transient	$V_{LOAD\_TRAN\_L2}$	$I_{L2OUT} = 0mA$ to $10mA$ , 200ns rise time			100		mV
		$I_{L2OUT} = 0mA$ to $100mA$ , 200ns rise time			200		
Passive Discharge Resistance	$R_{PDL\_L2}$			5	10	15	k $\Omega$
Active Discharge Current	$I_{ACTDL\_L2}$			8	22	40	mA
Switch Mode On-Resistance	$R_{ON\_L2}$	Switch mode	$V_{L2IN} = +2.7V$ , $I_{L2OUT} = 100mA$			0.7	$\Omega$
			$V_{L2IN} = +1.8V$ , $I_{L2OUT} = 50mA$			1	
			$V_{L2IN} = +1.2V$ , $I_{L2OUT} = 5mA$			2.3	
Turn-On Time	$t_{ON\_L2}$	$I_{L2OUT} = 0mA$ , time from 10% to 90% of LDO2VSet			1.5		ms
		$I_{L2OUT} = 0mA$ , time from 10% to 90% of $V_{L2IN}$ . Switch mode			0.26		
Short Circuit Current Limit	$I_{SHRT\_L2}$	$V_{L2IN} = +2.7V$ , $V_{L2OUT} = 0V$		225	360	555	mA
		$V_{L2IN} = +2.7V$ , $V_{L2OUT} = 0V$ , Switch mode		210	350	540	
Thermal Shutdown Temperature	$T_{SHDN\_L2}$	$T_J$ rising			150		$^{\circ}C$
Thermal Shutdown Temperature Hysteresis	$T_{SHDN\_HYS\_L2}$				20		$^{\circ}C$
Output Noise		10Hz to 100kHz, $V_{L2IN} = +5V$	$V_{L2OUT} = +3.3V$		150		$\mu V_{RMS}$
			$V_{L2OUT} = +2.5V$		125		
			$V_{L2OUT} = +1.2V$		90		
			$V_{L2OUT} = +0.9V$		80		
UVLO	$V_{L2IN\_UVLO}$	$V_{L2IN}$ falling		1.05	1.35		V
		$V_{L2IN}$ rising			1.36	1.69	

## Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOUT\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOUT} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CHARGE PUMP</b>						
Input Voltage	$V_{CPIN}$	Input voltage = $V_{SYS}$	2.7		5.5	V
Quiescent Supply Current	$I_{Q\_CP\_5V}$	$I_{CPOUT} = 0\mu A$ , CPVSet = 1 (+5V)		2	3.5	$\mu A$
	$I_{Q\_CP\_6.6V}$	$I_{CPOUT} = 0\mu A$ , CPVSet = 0 (+6.6V)		2.2	4.3	
CPOUT Output Voltage	$V_{CPOUT}$	CPVSet = 0, $I_{CPOUT} = 10\mu A$ , $V_{SYS} > +3.3V$		6.6		V
		CPVSet = 1, $I_{CPOUT} = 10\mu A$		5		
Output Accuracy	ACC_CP	$I_{CPOUT} < 120\mu A$ , $V_{SYS} > +3.3V$	-3		+3	%
Maximum Operative Output Current	$I_{CPOUT\_MAX}$	$V_{SYS} > +3.3V$ , -5% load regulation error	250			$\mu A$
Efficiency	EFF_CP	CPVSet = 0 (+6.6V), $I_{OUT} = 10\mu A$ , $V_{SYS} = +3.7V$		79		%
Max Charge Pump Frequency	FREQ_CP		88	100	110	kHz
Passive Discharge Resistance	$R_{PSV\_CP}$			10		k $\Omega$
<b>HAPTIC DRIVER</b>						
Input Voltage	$V_{HD\_IN}$	Input voltage = $V_{SYS}$	2.6		5.5	V
Quiescent Current	$I_{HD\_Q}$	$V_{DRP}/V_{DRN} = 0$ to $V_{SYS}$		1300		$\mu A$
H-Bridge PWM Output Frequency	$f_{HD\_PWM\_OUT}$		22.5	25	27.5	kHz
H-Bridge PWM Output Duty Cycle Resolution	$D_{HD\_PWM\_OUT}$	7 bits		$V_{SYS}/128$		% $V_{SYS}$
H-Bridge Output Impedance in Off State	$R_{HD\_OFF}$	HptOffImp = 1		15		k $\Omega$
		HptOffImp = 0		$R_{HD\_ON\_LS}$		$\Omega$
H-Bridge Output Leakage in High-Z State	$I_{HD\_LK\_OUT}$	During back EMF detection, $V_{DRP}/V_{DRN} = 0$ to $V_{SYS}$	-1		+1	$\mu A$
H-Bridge On-Resistance	$R_{HD\_ON\_HS}$	High-side PMOS switch on, 300mA load	0.04	0.18	0.5	$\Omega$
	$R_{HD\_ON\_LS}$	Low-side NMOS switch on, 300mA load	0.04	0.18	0.5	
H-Bridge Overcurrent Protection Threshold	$I_{HD\_OC\_THR}$	Rising current through high-side or low-side	600	1000	1500	mA
H-Bridge Overcurrent Protection Hysteresis	$I_{HD\_OC\_HYS}$			130		mA

### Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOUT\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOUT} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
H-Bridge Thermal Shutdown Temperature Threshold	$T_{HD\_SHDN\_THR}$	Rising temperature		150		$^{\circ}C$
H-Bridge Thermal Shutdown Temperature Hysteresis	$T_{HD\_SHDN\_HYS}$			25		$^{\circ}C$
PWM Input Frequency	$f_{HD\_INPWM}$		10		250	kHz
LRA Resonance Frequency Tracking Range	$f_{HD\_LRA}$	See <i>Haptic Driver</i> section	120		305	Hz
Startup Latency	$t_{HD\_START}$	Time from command to vibration response. See <i>Haptic Driver</i> section		10	12	ms
<b>LED CURRENT SINKS</b>						
Maximum Input Voltage	$V_{IN\_LED\_MAX}$				20	V
Quiescent Current	$I_{Q\_LED}$	All LEDs on, $V_{SYS} = 3.7V$		245	370	$\mu A$
Current Sink Setting Range	$I_{LED\_RNG}$	LEDIStep = 00 (0.6mA steps)	0.6		15	mA
		LEDIStep = 01 (1mA steps)	1		25	
		LEDIStep = 10 (1.2mA steps)	1.2		30	
LED Current Accuracy	ACC_LED	$I_{LED\_} = 13mA$ , $T_A = +25^{\circ}C$ , $V_{LED\_} = +0.7V$ to $+20V$	-2		+2	%
		$I_{LED\_} = 13mA$ , $V_{LED\_} = +0.7V$ to $+20V$	-4		+4	%
		$I_{LED\_} = 0.6mA$ to $30mA$ , $V_{LED\_} = +0.7V$ to $+20V$ , $T_A = 25^{\circ}C$	-5		+5	%
		$I_{LED\_} = 0.6mA$ to $30mA$ , $V_{LED\_} = +0.7V$ to $+20V$	-6		+6	%
LED Dropout Voltage	$V_{LED\_DROP}$	$I_{LED\_SET} = 5mA$ , $I_{LED\_} = 0.9 \times 5mA$		110	160	mV
		$I_{LED\_SET} = 25mA$ , $I_{LED\_} = 0.9 \times 25mA$		145	215	
		$I_{LED\_SET} = 30mA$ , $I_{LED\_} = 0.9 \times 30mA$		175	270	
Leakage in Shutdown	$I_{LK\_LED}$	$V_{LED\_} = +20V$			0.1	$\mu A$
Open-LED Detection Threshold	$V_{LED\_DET}$	LED_ enabled, LEDIStep = 00, falling edge	61	92	140	mV

## Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOUT\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOUT} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>FUEL GAUGE</b>						
Supply Voltage	$V_{CELL}$	(Note 3)	2.5		4.5	V
Fuel-Gauge SOC Reset ( $V_{RESET}$ Register)	$V_{RST}$	Configuration range, in 40mV steps	2.28		3.48	V
		Trimmed at 3V	2.85	3.0	3.15	
Supply Current	$I_{DD0}$	Sleep mode		0.5	2	$\mu A$
		Hibernate mode, reset comparator disabled ( $V_{RESET.Dis} = 1$ )		3	5	
		Hibernate mode, reset comparator enabled ( $V_{RESET.Dis} = 0$ )		4	6	
	$I_{DD1}$	Active mode		23	40	
Time Base Accuracy	$t_{ERR}$	Active, hibernate modes (Note 4)	-3.5		+3.5	%
AD Sample Period		Active mode		250		ms
		Hibernate mode		45		s
Voltage Error	$V_{ERR}$	$V_{CELL} = 3.6V$ , $T_A = +25^{\circ}C$ (Note 5)	-9		+6	mV/cell
		$T_A = -20^{\circ}C$ to $+70^{\circ}C$	-23		+20	
Voltage-Measurement Resolution				1.25		mV/cell
BAT-to-Cell On-Resistance	$R_{ON\_ISO}$	$V_{BAT} = 3.7V$		15	30	$\Omega$
Bus Low-Detection Timeout	$t_{SLEEP}$	(Notes 6, 7)		2.125		s
<b>DIGITAL</b>						
SDA, SCL, MPC_, PFN_ Input Leakage Current	$I_{LK\_IO}$	Input pullup/pulldown resistances disabled, input voltage from 0 to +5.5V	-1		+1	$\mu A$
SDA, SCL, MPC_ Input Logic-High	$V_{IO\_IH}$		1.4			V
SDA, SCL, MPC_ Input Logic-Low	$V_{IO\_IL}$				0.5	V
PFN_ Input Logic-High	$V_{PFN\_IH}$	(Note 2)		$0.7 \times V_{CCINT}$		V
PFN_ Input Logic-Low	$V_{PFN\_IL}$	(Note 2)		$0.3 \times V_{CCINT}$		V
MPC_, PFN_ Input Pullup Resistance	$R_{IO\_UP}$	Pullup resistance to $V_{CCINT}$ (Note 2)		170		k $\Omega$
MPC_, PFN_ Input Pulldown Resistance	$R_{IO\_PD}$			170		k $\Omega$
MPC_ Output Logic-High	$V_{IO\_OH}$	$I_{OH} = 1mA$ , MPC_ configured as push-pull output, pullup voltage is $V_{BK2OUT}$	$V_{BK2OUT} - 0.4$			V



## Electrical Characteristics (continued)

( $V_{BAT} = +3.7V$ ,  $T_A = -20^{\circ}C$  to  $+70^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 10\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 1\mu F$ ,  $C_{L2IN} = 1\mu F$ ,  $C_{L1OUT} = 1\mu F$ ,  $C_{L2OUT} = 1\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOUT\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOUT} = 4.7\mu H$ ). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA, RST, INT, MPC_, PFN_ Output Logic-Low	$V_{IO\_OL}$	$I_{OL} = 4mA$			0.4	V
SDA, SCL Bus Low-Detection Current	$I_{PD}$	$V_{SDA} = V_{SCL} = +0.4V$		0.2	0.4	$\mu A$
SCL Clock Frequency	$f_{SCL}$		0		400	kHz
Bus Free Time Between a STOP and START Condition	$t_{BUF}$		1.3			$\mu s$
START Condition (repeated) Hold Time	$t_{HD\_STA}$		0.6			$\mu s$
Low Period of SCL Clock	$t_{LOW}$		1.3			$\mu s$
High Period of SCL Clock	$t_{HIGH}$		0.6			$\mu s$
Setup Time for a Repeated START Condition	$t_{SU\_STA}$		0.6			$\mu s$
Data Hold Time	$t_{HD\_DAT}$		0		0.9	$\mu s$
Data Setup Time	$t_{SU\_DAT}$		100			$\mu s$
Setup Time for a STOP Condition	$t_{SU\_STO}$		0.6			$\mu s$
Spike Pulse Widths Suppressed by Input Filter	$t_{SP}$		50			ns

**Note 1:** All devices are 100% production tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range are guaranteed by design.

**Note 2:**  $V_{CCINT}$  is an internal voltage supply generated from either  $V_{BAT}$  or  $V_{CAP}$ . The source is determined by the following:

IF  $[(V_{CHGIN} > V_{CHGIN\_DET} \text{ AND } V_{CAP} > V_{CAP\_OK}) \text{ OR } V_{CAP} > (V_{BAT} + V_{THSWOVER})]$

THEN  $V_{CCINT} = V_{CAP}$

ELSE

$V_{CCINT} = V_{BAT}$

Where  $V_{THSWOVER} = [0-300]mV$

**Note 3:** All voltages are referenced to GND.

**Note 4:** Test performed on unmounted/unsoldered parts.

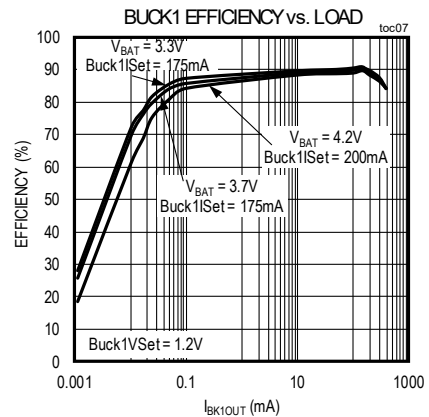
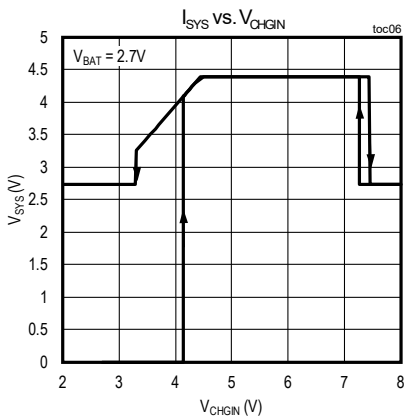
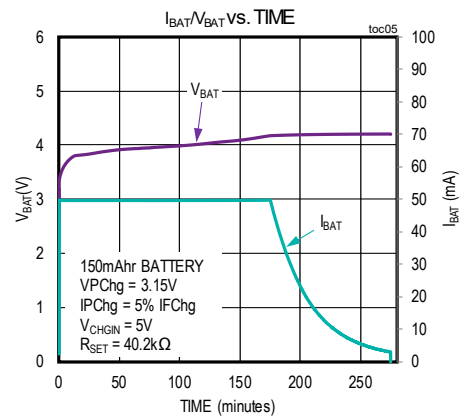
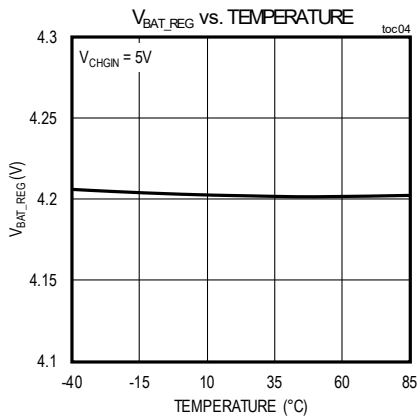
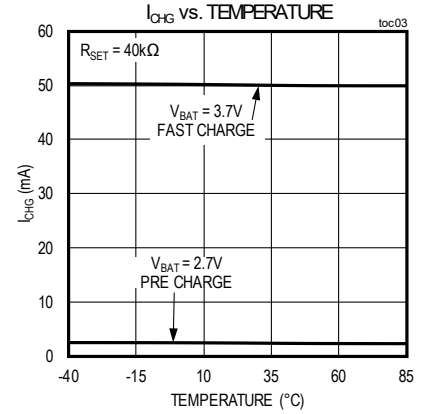
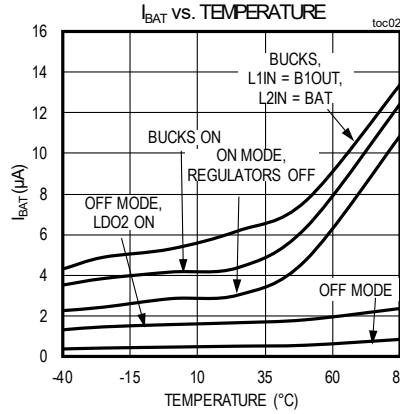
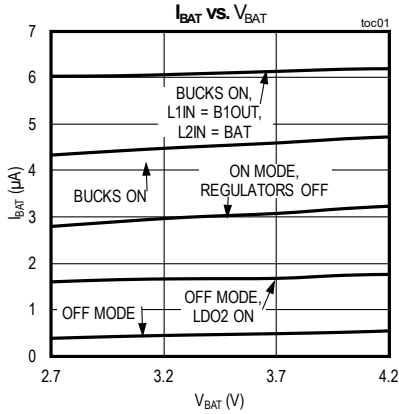
**Note 5:** The voltage is trimmed and verified with 16x averaging.

**Note 6:** Fuel Gauge enters shutdown mode after  $SCL < V_{IL}$  and  $SDA < V_{IL}$  for longer than  $t_{SLEEP}$ .

**Note 7:** Guaranteed by design.

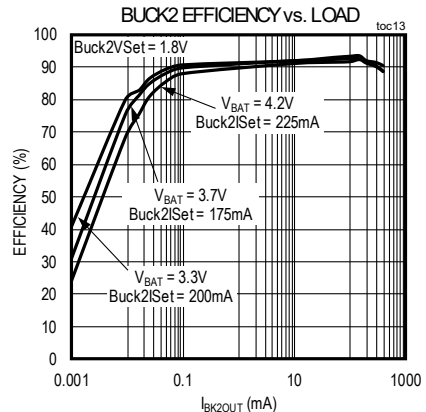
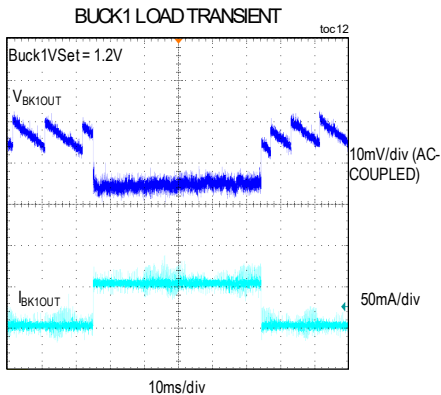
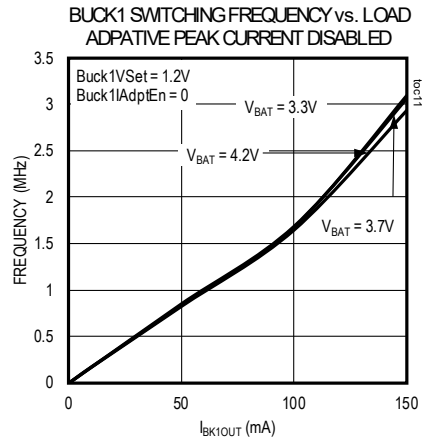
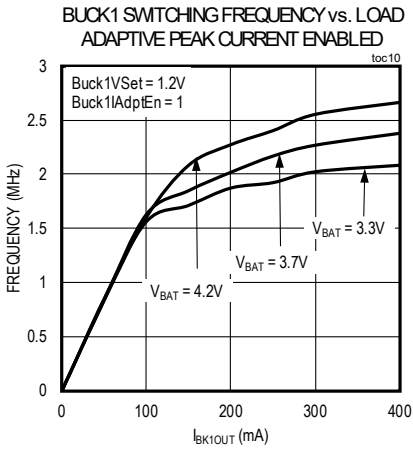
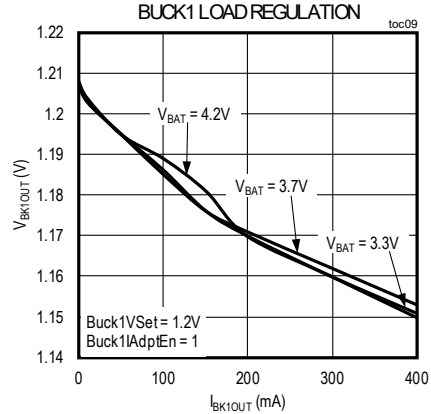
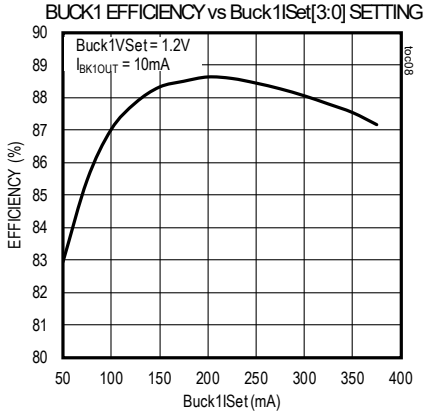
### Typical Operating Characteristics

$V_{BAT} = +3.7V$ ,  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 15\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 22\mu F$ ,  $C_{L2IN} = 22\mu F$ ,  $C_{L1OUT\_EFF} = 15\mu F$ ,  $C_{L2OUT\_EFF} = 10\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



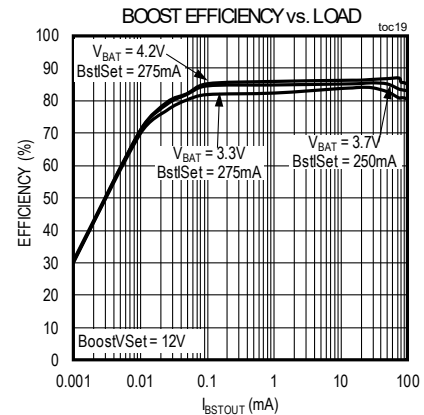
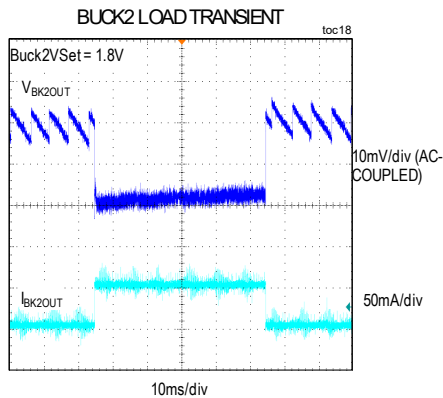
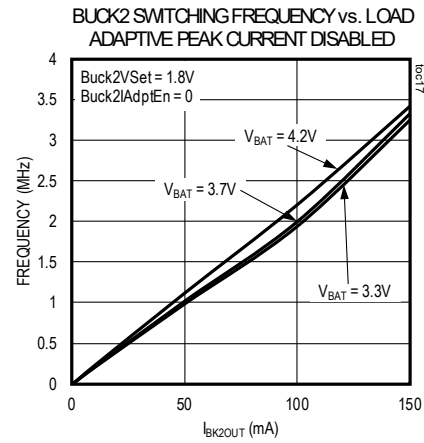
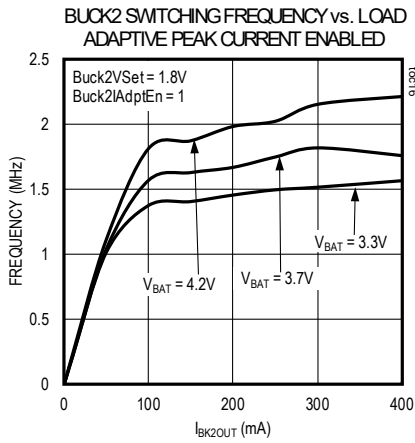
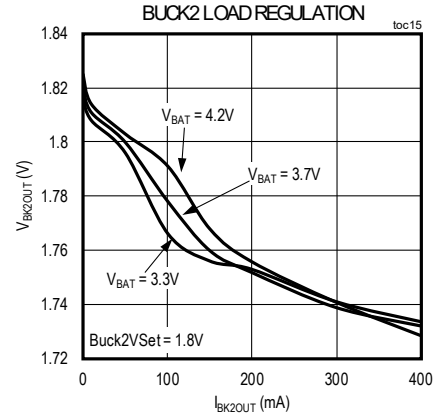
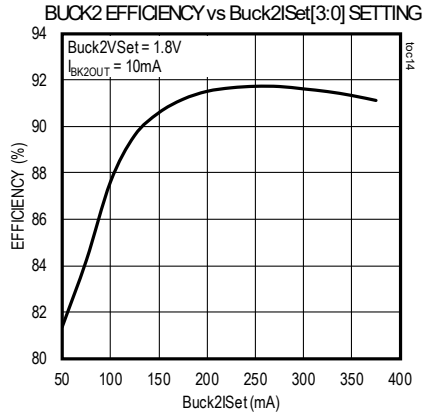
Typical Operating Characteristics (continued)

$V_{BAT} = +3.7V$ ,  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 15\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 22\mu F$ ,  $C_{L2IN} = 22\mu F$ ,  $C_{L1OUT\_EFF} = 15\mu F$ ,  $C_{L2OUT\_EFF} = 10\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



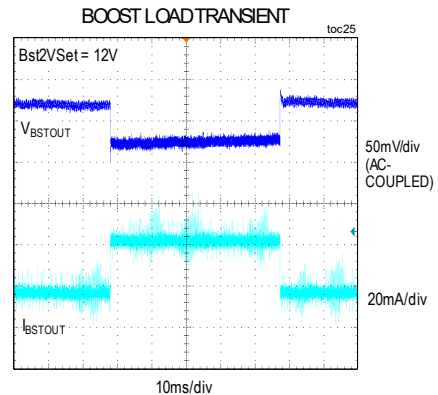
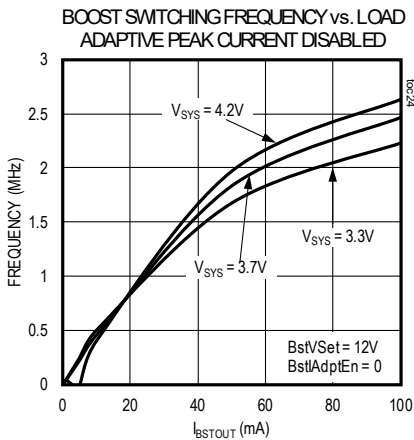
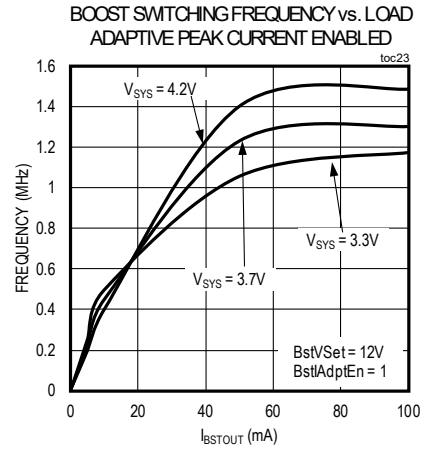
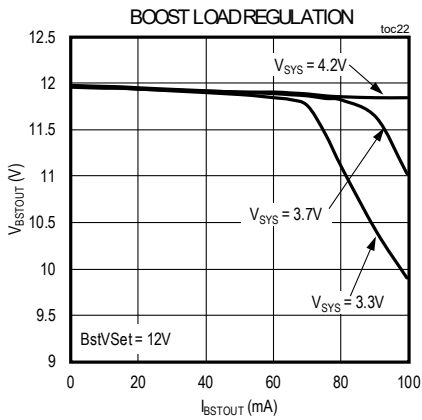
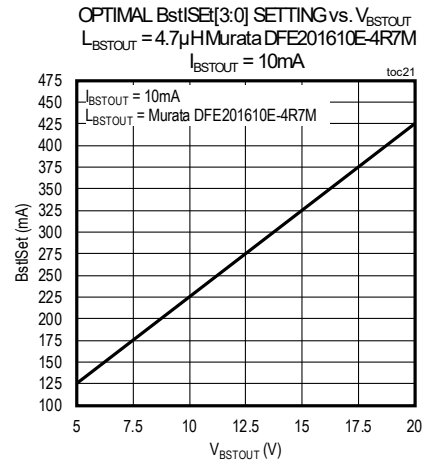
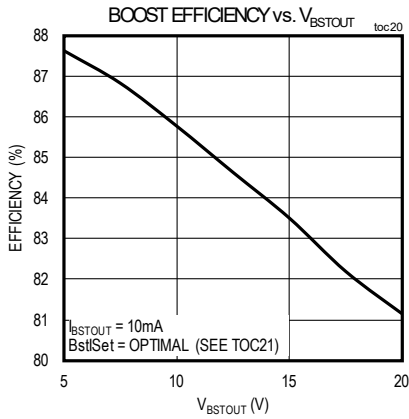
Typical Operating Characteristics (continued)

$V_{BAT} = +3.7V$ ,  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 15\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 22\mu F$ ,  $C_{L2IN} = 22\mu F$ ,  $C_{L1OUT\_EFF} = 15\mu F$ ,  $C_{L2OUT\_EFF} = 10\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



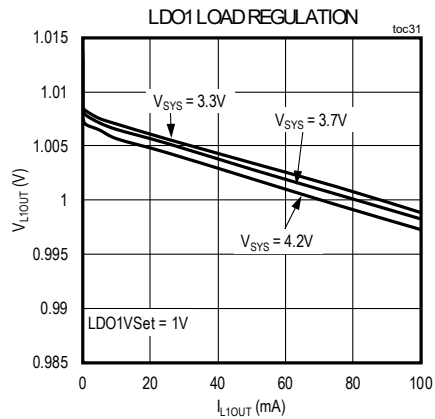
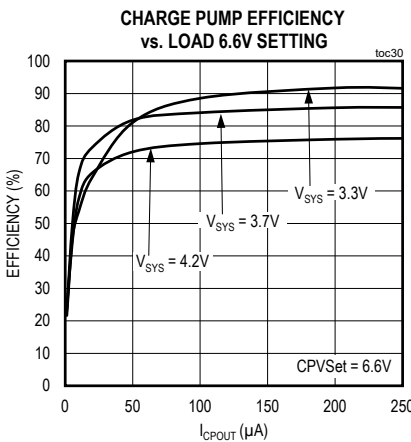
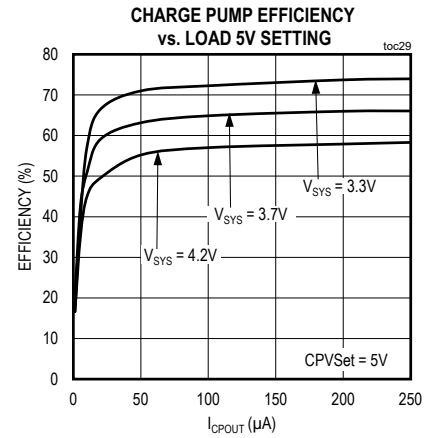
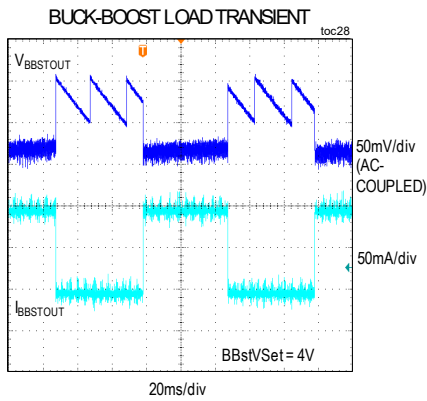
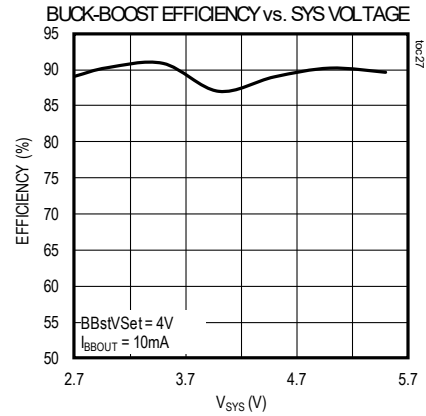
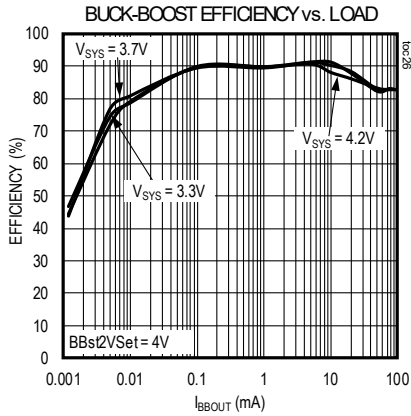
Typical Operating Characteristics (continued)

$V_{BAT} = +3.7V$ ,  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 15\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 22\mu F$ ,  $C_{L2IN} = 22\mu F$ ,  $C_{L1OUT\_EFF} = 15\mu F$ ,  $C_{L2OUT\_EFF} = 10\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



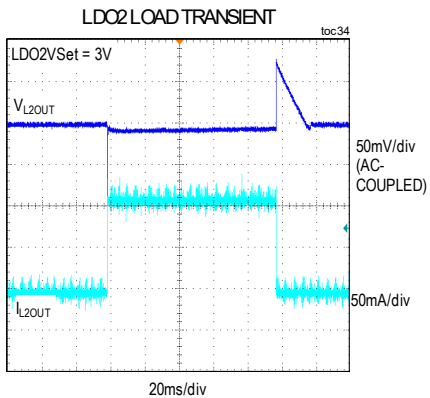
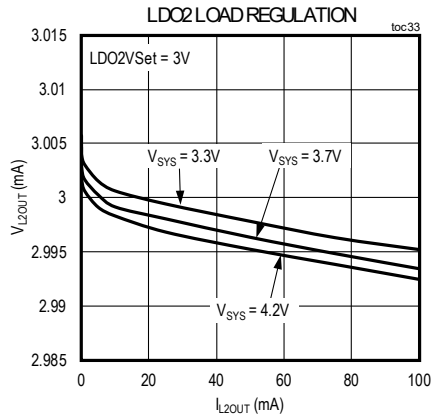
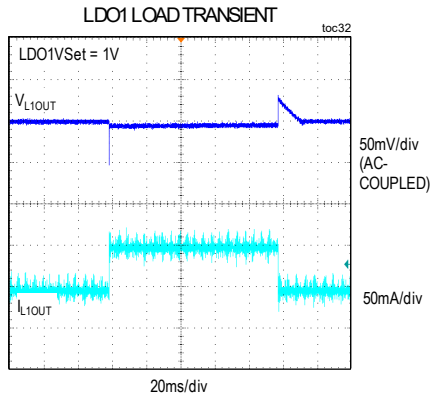
Typical Operating Characteristics (continued)

$V_{BAT} = +3.7V$ ,  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 15\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 22\mu F$ ,  $C_{L2IN} = 22\mu F$ ,  $C_{L1OUT\_EFF} = 15\mu F$ ,  $C_{L2OUT\_EFF} = 10\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

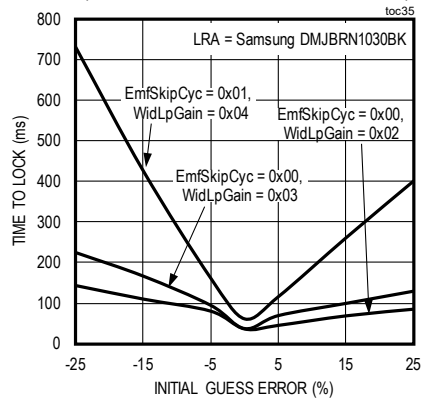


Typical Operating Characteristics (continued)

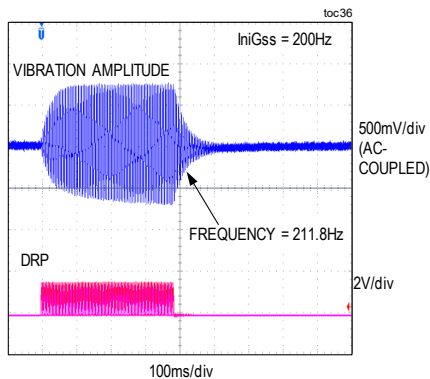
$V_{BAT} = +3.7V$ ,  $C_{SFOUT} = 1\mu F$ ,  $C_{VDIG} = 1\mu F$ ,  $C_{CAP} = 1\mu F$ ,  $C_{SYS} = 10\mu F$ ,  $C_{BK1OUT\_EFF} = 15\mu F$ ,  $C_{BK2OUT\_EFF} = 10\mu F$ ,  $C_{L1IN} = 22\mu F$ ,  $C_{L2IN} = 22\mu F$ ,  $C_{L1OUT\_EFF} = 15\mu F$ ,  $C_{L2OUT\_EFF} = 10\mu F$ ,  $C_{CPP} = 27nF$ ,  $C_{BSTOUT\_EFF} = 10\mu F$ ,  $C_{BBOU\_EFF} = 10\mu F$ ,  $L_{BK1} = 2.2\mu H$ ,  $L_{BK2} = 2.2\mu H$ ,  $L_{BSTOUT} = 4.7\mu H$ ,  $L_{BBOU} = 4.7\mu H$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



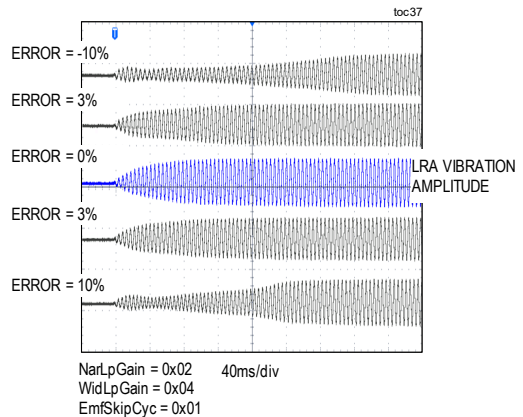
TIME TO RESONANCE LOCK vs. INITIAL GUESS ERROR (ESTIMATED BY VIBRATION AMPLITUDE)



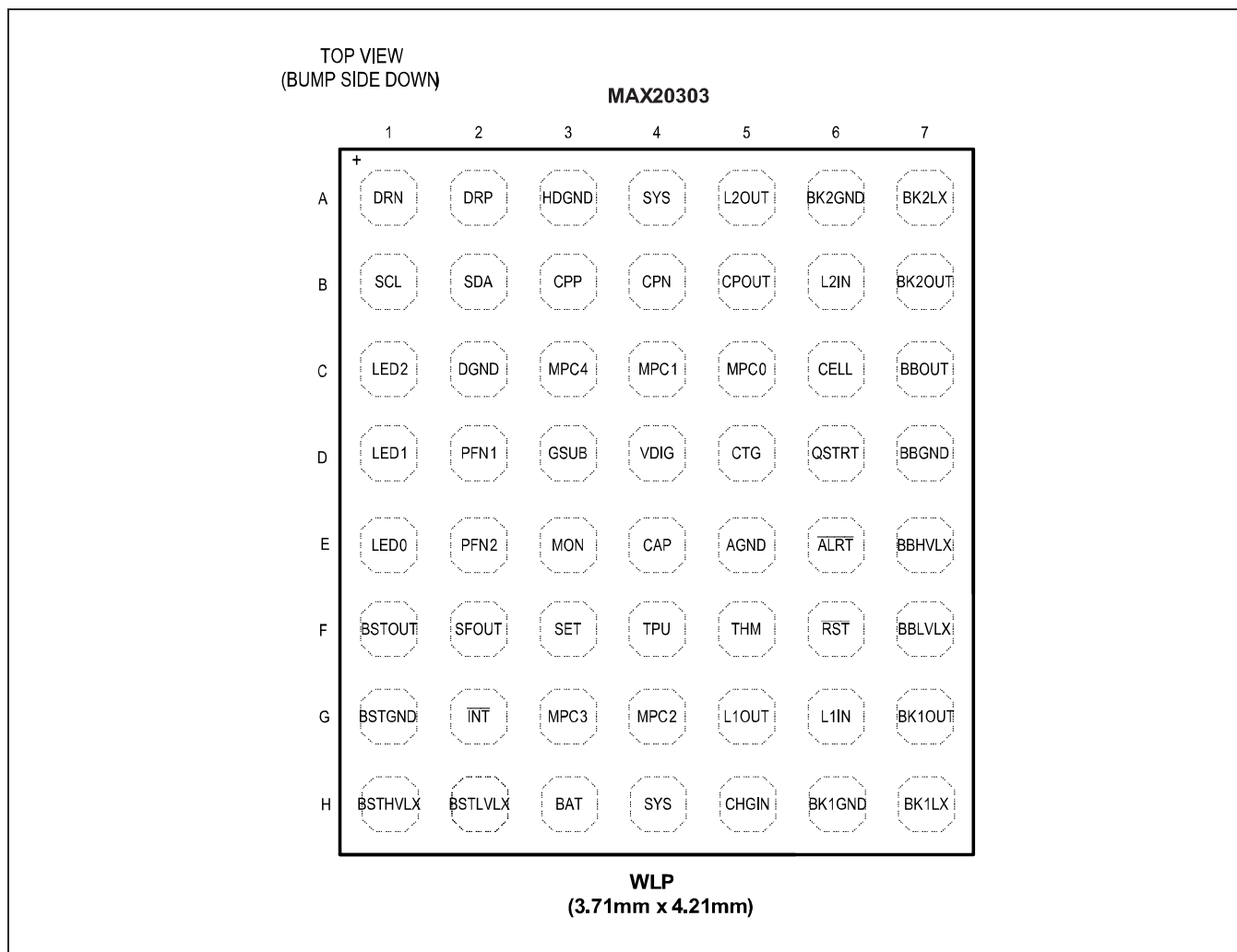
HAPTIC DRIVER LRA SELF TUNING  
IniGss CLOSE TO RESONANT FREQUENCY



HAPTIC DRIVER LRA SELF TUNING  
ERROR IN IniGss RESONANCE SETTING



### Bump Configuration





## Bump Description

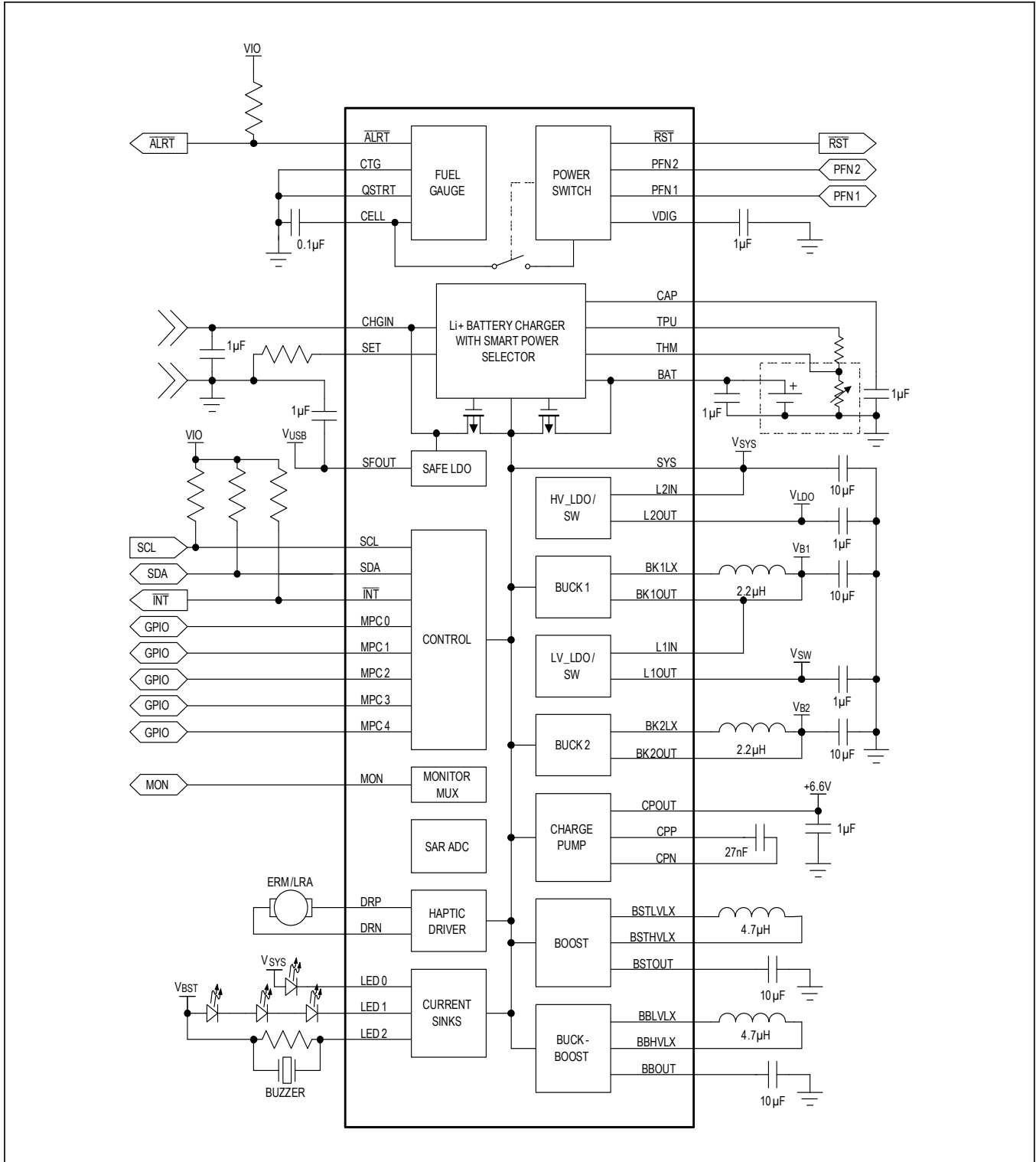
BUMP	NAME	FUNCTION
A1	DRN	ERM/LRA Haptic Driver Negative Output.
A2	DRP	ERM/LRA Haptic Driver Positive Output.
A3	HDGND	Haptic Driver Ground.
A4, H4	SYS	System Load Connection. Connect to the system load. Both SYS bumps should be connected on PCB through a low-impedance trace. Bypass common node with a minimum 10 $\mu$ F capacitor to GND.
A5	L2OUT	LDO Output. Bypass with 1 $\mu$ F capacitor to GND.
A6	BK2GND	Buck 2 Ground.
A7	BK2LX	Buck2 Regulator Switch. Connect through 2.2 $\mu$ H inductor to BK2OUT.
B1	SCL	I <sup>2</sup> C Serial Clock Input.
B2	SDA	I <sup>2</sup> C Serial Data Input/Open-Drain Output.
B3	CPP	Charge Pump Capacitor Positive Terminal. Connect 22nF (min), 33nF (max) capacitor to CPN.
B4	CPN	Charge Pump Capacitor Negative Terminal. Connect to 22nF (min), 33nF (max) capacitor to CPP.
B5	CPOUT	Charge Pump Output. Bypass with 1 $\mu$ F capacitor to GND.
B6	L2IN	LDO2 Input. Bypass with 1 $\mu$ F capacitor to GND.
B7	BK2OUT	Buck2 Regulator Output. Bypass with 10 $\mu$ F capacitor to GND.
C1	LED2	Current Sink Output 2.
C2	DGND	Digital Ground.
C3	MPC4	Multipurpose Control I/O 4.
C4	MPC1	Multipurpose Control I/O 1.
C5	MPC0	Multipurpose Control I/O 0.
C6	CELL	Fuel Gauge Voltage. Bypass with 0.1 $\mu$ F capacitor to GND.
C7	BBOUT	Buck-Boost Regulator Output. Bypass with 10 $\mu$ F capacitor to GND.
D1	LED1	Current Sink Output 1.
D2	PFN1	Configurable Power Mode Control Pin (e.g., $\overline{\text{KIN}}$ ).
D3	GSUB	Substrate Connection. Connect to Ground.
D4	VDIG	Internal Reference Supply. Bypass with 1 $\mu$ F capacitor to GND.
D5	CTG	Fuel Gauge. Connect to GND.
D6	QSTRT	Fuel Gauge Quick Start Input.
D7	BBGND	Buck-Boost Ground.
E1	LED0	Current Sink Output 0.
E2	PFN2	Configurable Power Mode Control Pin (e.g., $\overline{\text{KOUT}}$ ).
E3	MON	Monitor Multiplexer Output.
E4	CAP	Internal Reference Supply. Bypass with 1 $\mu$ F capacitor to GND.
E5	AGND	Analog Ground.

## Bump Description (continued)

BUMP	NAME	FUNCTION
E6	$\overline{\text{ALRT}}$	Fuel Gauge Alert Output.
E7	BBHVLX	Buck-Boost Regulator Switch HV side. Connect through a 3.3 $\mu\text{H}$ or 4.7 $\mu\text{H}$ inductor to BBLVLX.
F1	BSTOUT	Boost Regulator Output. Bypass with 10 $\mu\text{F}$ capacitor to GND.
F2	SFOUT	Safe Out LDO. Bypass with 1 $\mu\text{F}$ capacitor to GND.
F3	SET	External Resistor For Battery Charge Current Level Setting. Do not connect any capacitance on this pin; maximum allowed capacitance ( $C_{\text{SET}} < 5\mu\text{s}/R_{\text{SET}}$ )pF.
F4	TPU	Battery Temperature Thermistor Measurement Pullup (Internally Connected To $V_{\text{DIG}}$ During Battery Temperature Thermistor Measurement). Do not exceed 1mA load on TPU.
F5	THM	Battery Temperature Thermistor Measurement Connection.
F6	$\overline{\text{RST}}$	Reset Output. Active-Low, Open-Drain Output.
F7	BBLVLX	Buck-Boost Regulator Switch LV Side. Connect through a 3.3 $\mu\text{H}$ or 4.7 $\mu\text{H}$ inductor to BBHVLX.
G1	BSTGND	High-Voltage Boost Ground.
G2	$\overline{\text{INT}}$	Interrupt Open-Drain Output.
G3	MPC3	Multipurpose Control I/O 3.
G4	MPC2	Multipurpose Control I/O 2.
G5	L1OUT	LDO1 Output. Bypass with 1 $\mu\text{F}$ capacitor to GND.
G6	L1IN	LDO1 Input. Bypass with 1 $\mu\text{F}$ capacitor to GND.
G7	BK1OUT	Buck1 Regulator Output. Bypass with 10 $\mu\text{F}$ capacitor to GND.
H1	BSTHVLX	Boost Regulator Switch. Connect through a 4.7 $\mu\text{H}$ inductor to BSTLVLX.
H2	BSTLVLX	Boost Regulator Switch. Connect through a 4.7 $\mu\text{H}$ inductor to BSTHVLX.
H3	BAT	Battery Connection. Connect to positive battery terminal. Bypass with a minimum 1 $\mu\text{F}$ capacitor to GND.
H5	CHGIN	+28V/-5.5V Protected Charger Input. Bypass with 1 $\mu\text{F}$ capacitor to GND.
H6	BK1GND	Buck 1 Ground.
H7	BK1LX	Buck1 Regulator Switch. Connect through a 2.2 $\mu\text{H}$ inductor to BK1OUT.

**Note:** All capacitance values listed in this document refer to effective capacitance. Be sure to specify capacitors that will meet these requirements under typical operating conditions taking into consideration the effects of voltage and temperature.

Typical Application Diagram



## Detailed Description

### Power Regulation

The MAX20303 features two high-efficiency, low quiescent current buck regulators, a buck-boost regulator, a high-voltage boost regulator, a charge pump, and two low quiescent current, low-dropout (LDO) linear regulators that are configurable as load switches. Additionally, a safe-output LDO is available when there is a valid voltage present at CHGIN. This SFOUT regulator's output is configurable to 3.3V or 5V. Excellent light-load efficiency allows the switching regulators to run continuously without significant energy cost. The buck and boost regulators can operate in a fixed peak current mode for low-current applications, as well as an adaptive peak current mode to improve load regulation, extend the high-efficiency range, and minimize capacitor size when more current is required.

### Power Switch and Reset Control

The MAX20303 features a power switch that provides the ability to execute a reset sequence or to turn off the main system power and enter Off mode to extend battery life.

Shutdown and reset events are triggered by an external control through the power function (PFN) control inputs, I<sup>2</sup>C commands, or if other conditions are met. The behavior of the PFN pins is preconfigured to support one of the multiple types of wearable application cases. [Table 1](#) describes the behavior of the PFN1 and PFN2 pins based on the PwrRstCfg[3:0] bits, while [Figure 1a](#) thru [Figure 1d](#) shows basic flow diagrams associated with each mode.

A soft reset sends a 10ms pulse on  $\overline{\text{RST}}$  and will either leave register settings unchanged or reset them to their default values depending on the device version (see [Table 192](#) for device settings). A hard reset on any device initiates a complete Power-On Reset sequence.

The device enters Off mode on cold boot (initial battery attach,  $V_{\text{CHGIN}} = 0\text{V}$ ) in response to a power-off I<sup>2</sup>C command, a valid PFN signal based on the PwrRstCfg[3:0] setting, or in the case of a UVLO condition on SYS. When the device is in Off mode, the BAT-SYS connection is opened and all functions are disabled except for the power function controller and LDO2 (if configured as always-on).

The MAX20303 will exit Off mode and turn the main power back on when there is a qualified PFN1 signal (PwrRstCfg[3:0] = 0000, 0001, 0110, 0111, 1000) or when a valid voltage is applied to CHGIN. In the powered-on state, the SYS node is enabled and other functions can be controlled through the I<sup>2</sup>C registers. When the power-on event occurs, the BAT-to-CELL switch is immediately closed and, 30ms later, the power path to SYS is enabled. This delay allows the fuel gauge to take an open cell measurement before the battery is loaded. Note that there is a relearning period to determine the state of the battery whenever the fuel gauge is disconnected. If the typical use case frequently switches the fuel gauge off and on, the user may consider permanently connecting CELL-to-BAT to avoid the relearning period. [Figure 2](#) illustrates a complete boot sequence coming out of the Off state.

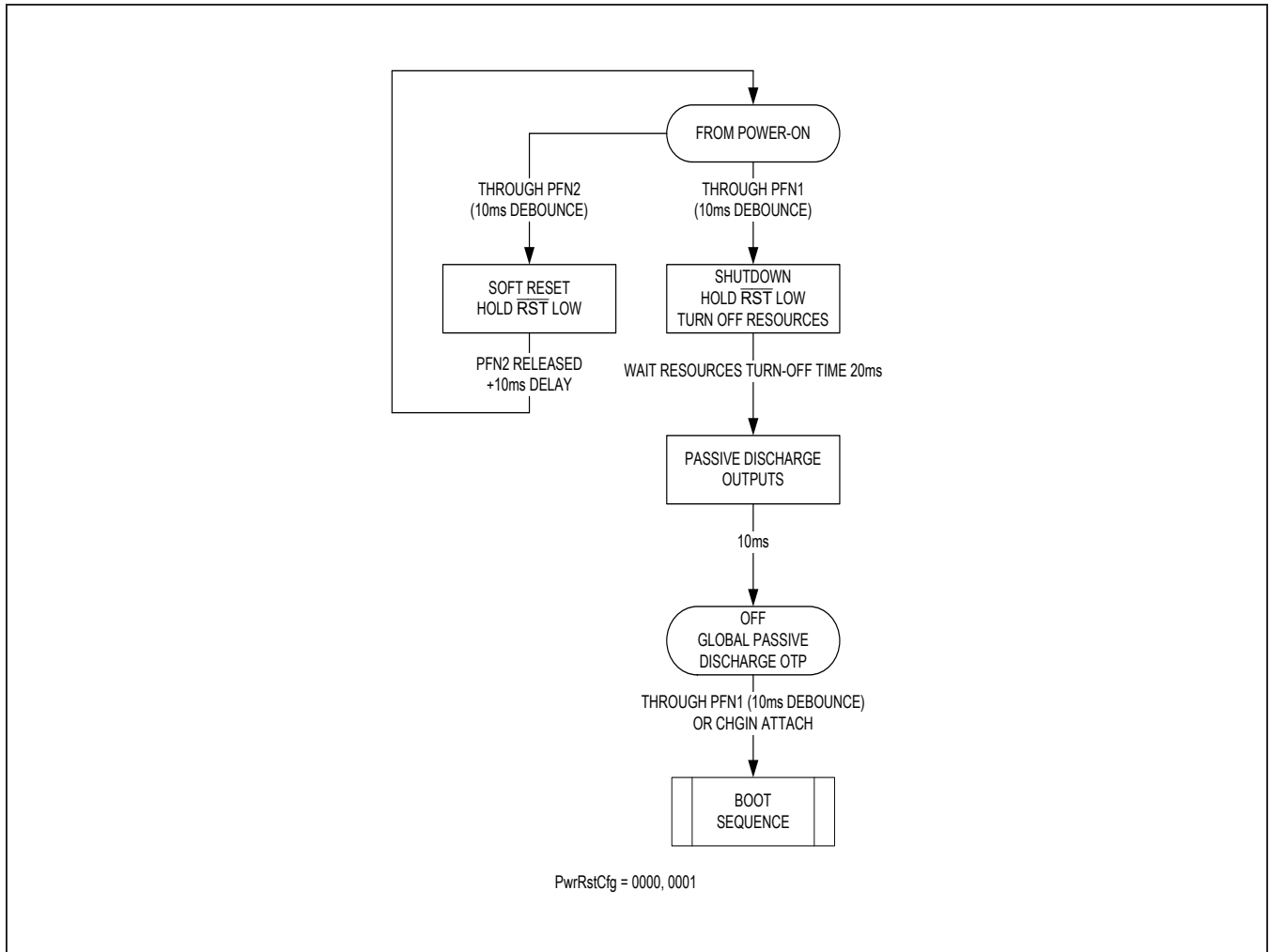


Figure 1a. PwrRstCfg = 0000 or 0001

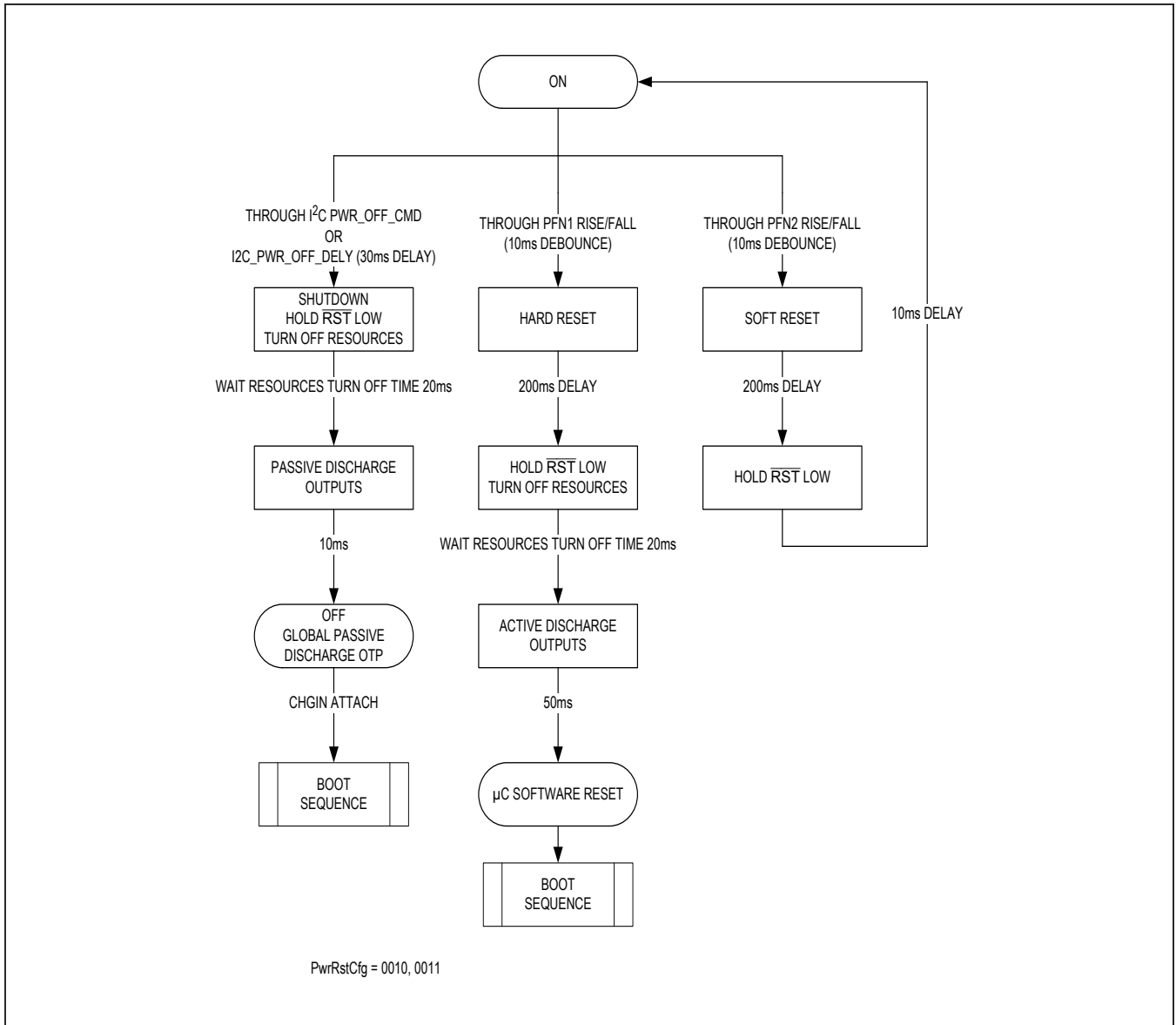


Figure 1b. PwrRstCfg = 0010 or 0011

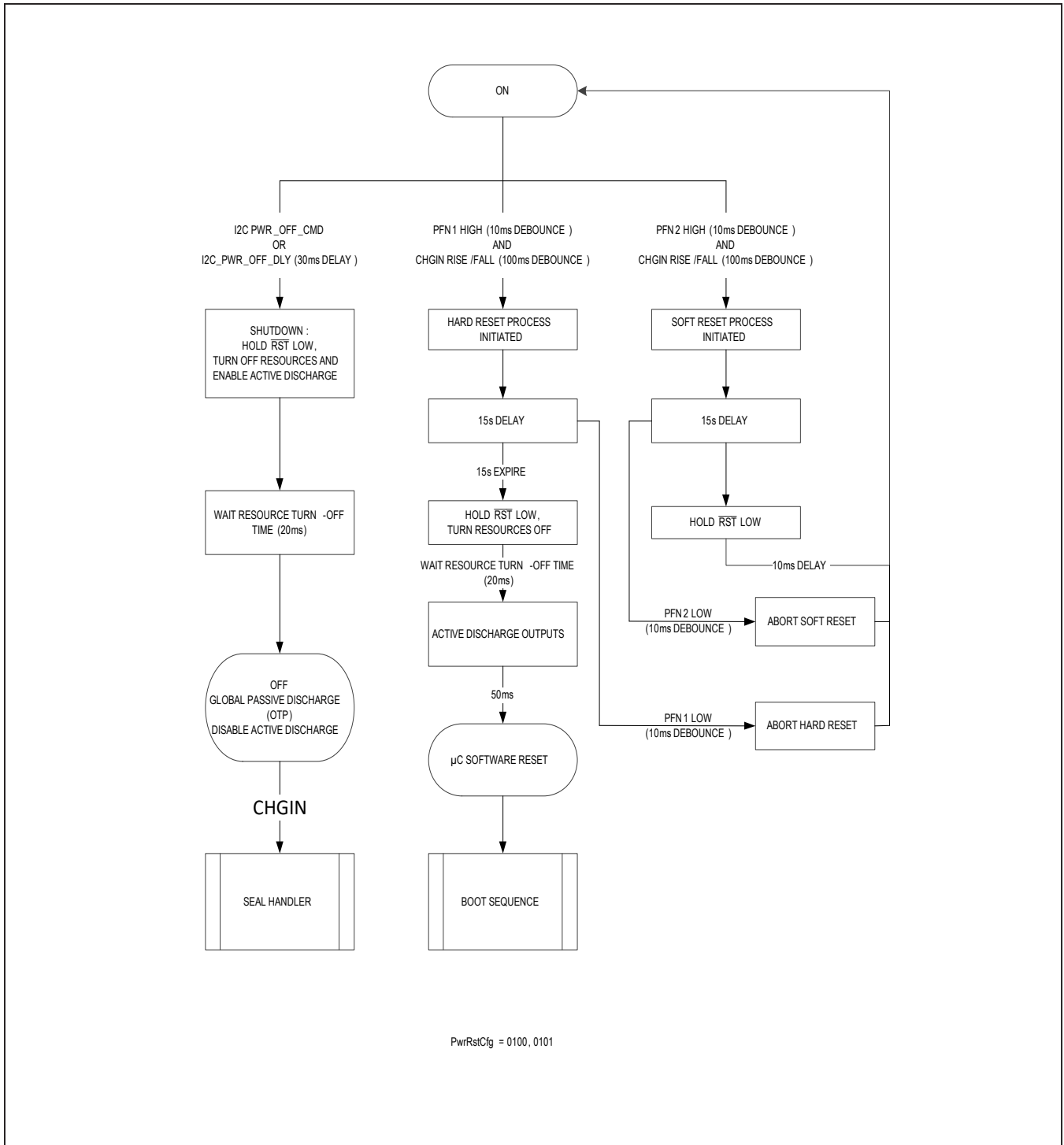


Figure 1c. PwrRstCfg = 0100 or 0101

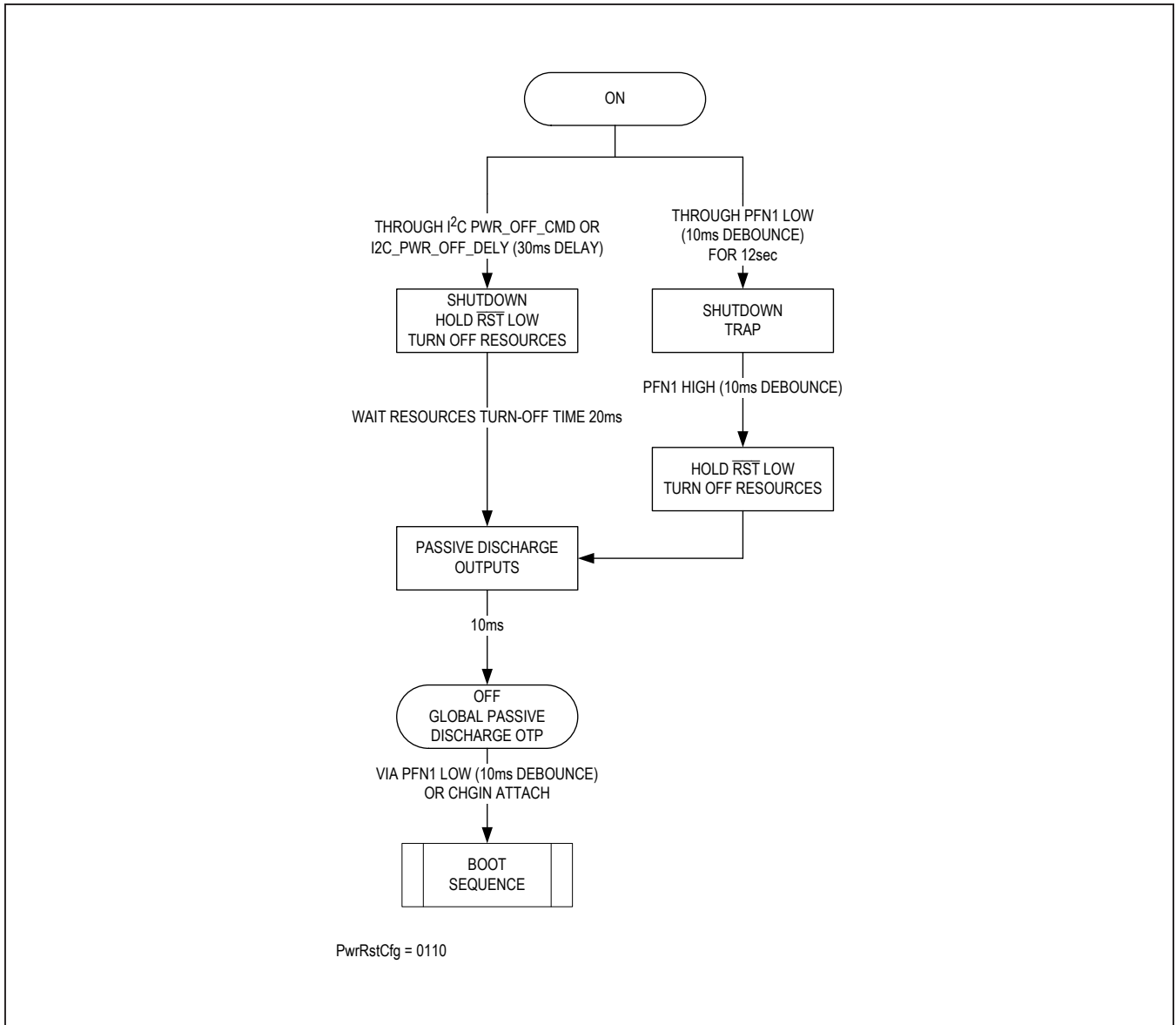


Figure 1d. PwrRstCfg = 0110



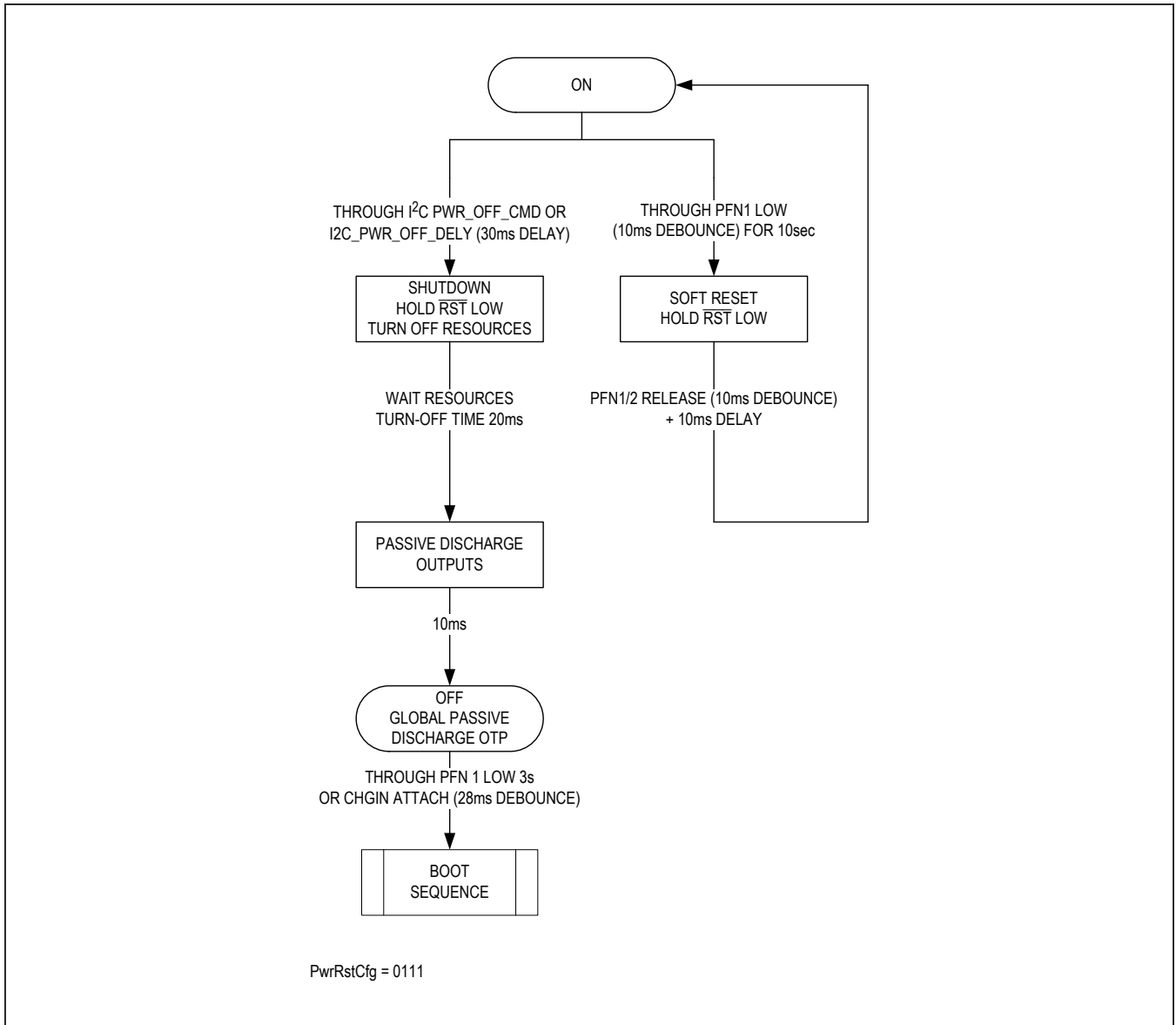


Figure 1e. PwrRstCfg = 0111

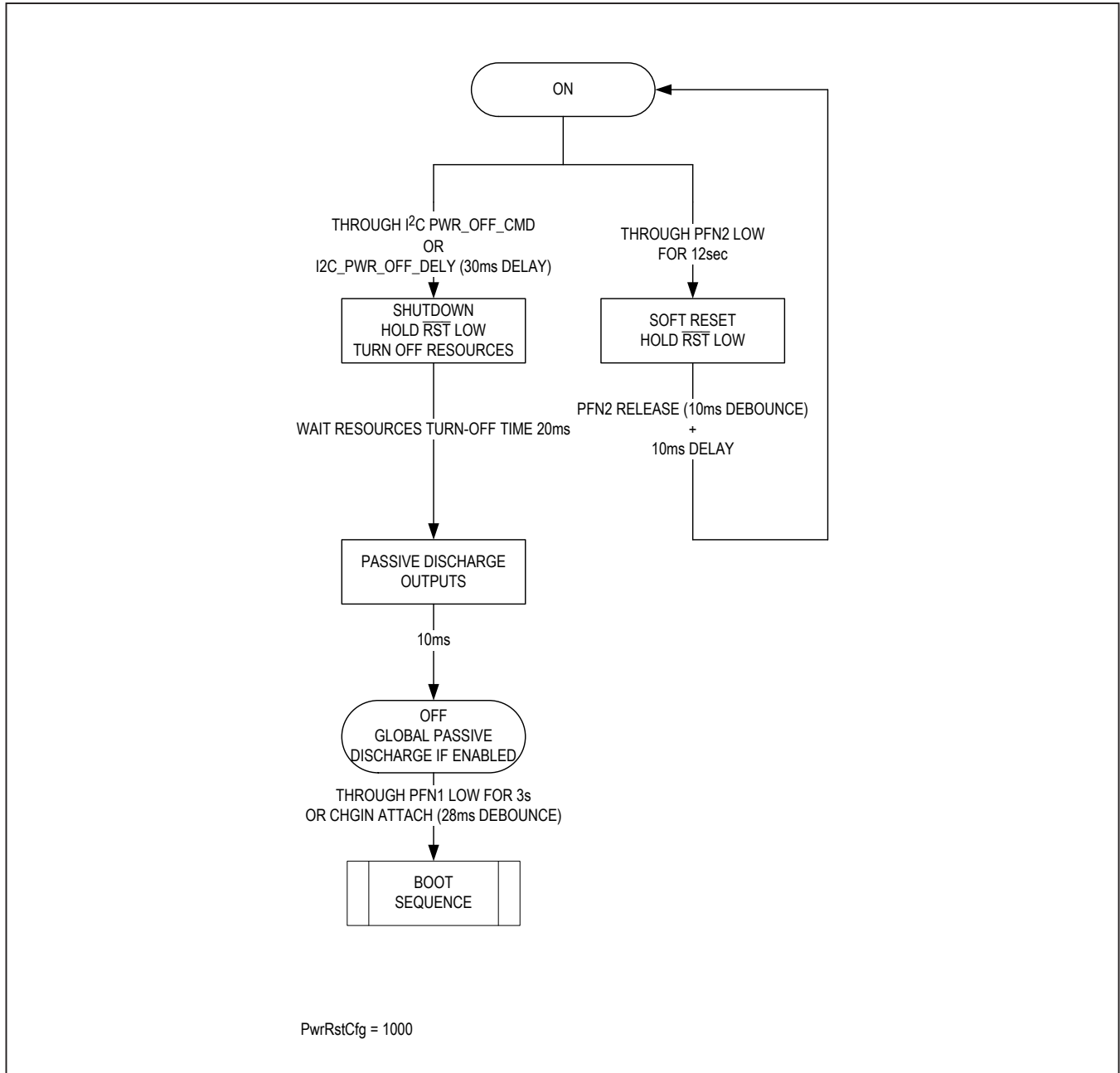


Figure 1f. PwrRstCfg = 1000

Table 1. PwrRstCfg Settings

PwrRstCfg	PFN1	PFN1 PU/PD	PFN2	PFN2 PU/PD	Notes
0000	Enable	Pulldown	Soft-Reset Active-Low	Pullup	On/Off mode with 10ms debounce. Active-high On/Off control on PFN1. Logic-low on PFN2 generates 10ms pulse on $\overline{RST}$ . <b>Note:</b> In this mode, if PFN1 is high, PWR_OFF_CMD will cause the part to turn off, then immediately return to the ON state.
0001	Disable	Pullup	Soft-Reset Active-Low	Pullup	On/Off mode with 10ms debounce. Active-low On/Off control on PFN1. Logic-low on PFN2 generates 10ms pulse on $\overline{RST}$ . <b>Note:</b> In this mode, if PFN1 is high, PWR_OFF_CMD will cause the part to turn off, then immediately return to the ON state.
0010	Hard-Reset Active-High	Pulldown	Soft-Reset Active-High	Pulldown	Always-On mode (i.e., device can only be put in Off state through PWR_OFF_CMD). 10ms hard reset off time. 10ms soft reset pulse time. 200ms delay prior to both reset behaviors.
0011	Hard-Reset Active-Low	Pullup	Soft-Reset Active-Low	Pullup	Always-On mode (i.e., device can only be put in Off state through PWR_OFF_CMD). 50ms Hard-Reset off time. 10ms Soft-Reset pulse time. 200ms delay prior to both reset behaviors.
0100	Hard-Reset Active-High Triggered on CHGIN Insertion	Pulldown	Soft-Reset Active-High Triggered on CHGIN Insertion	Pulldown	Always-On mode (i.e., device can only be put in Off state through PWR_OFF_CMD). 50ms Hard-Reset off time. 10ms Soft-Reset pulse time. 15s delay prior to both reset behaviors. Either reset may be aborted
0101	Hard-Reset Active-Low Triggered by CHGIN Insertion	Pullup	Soft-Reset Active-Low Triggered on CHGIN Insertion	Pullup	Always-On mode (i.e., device can only be put in Off state through PWR_OFF_CMD). 70ms Hard-Reset off time. 10ms Soft-Reset pulse time. 15s delay prior to both reset behaviors. Either reset may be aborted.
0110	$\overline{KIN}$	Pullup	KOUT	None	On/Off mode through specific long-press button timing or PWR_OFF_CMD.
0111	$\overline{KIN}$	Pullup	KOUT	None	Off mode through PWR_OFF_CMD. On mode through specific long-press (3s) or CHGIN insertion soft reset through specific long press (10s).
1000	$\overline{KIN}$	Pullup	Soft-Reset Active-Low 12s Long Press	Pullup	Custom Two Button. Off mode through PWR_OFF_CMD. On mode through $\overline{KIN}$ long-press (3s) or CHGIN insertion. Soft reset through PFN2 long press (12s).
1001-1111	RFU				

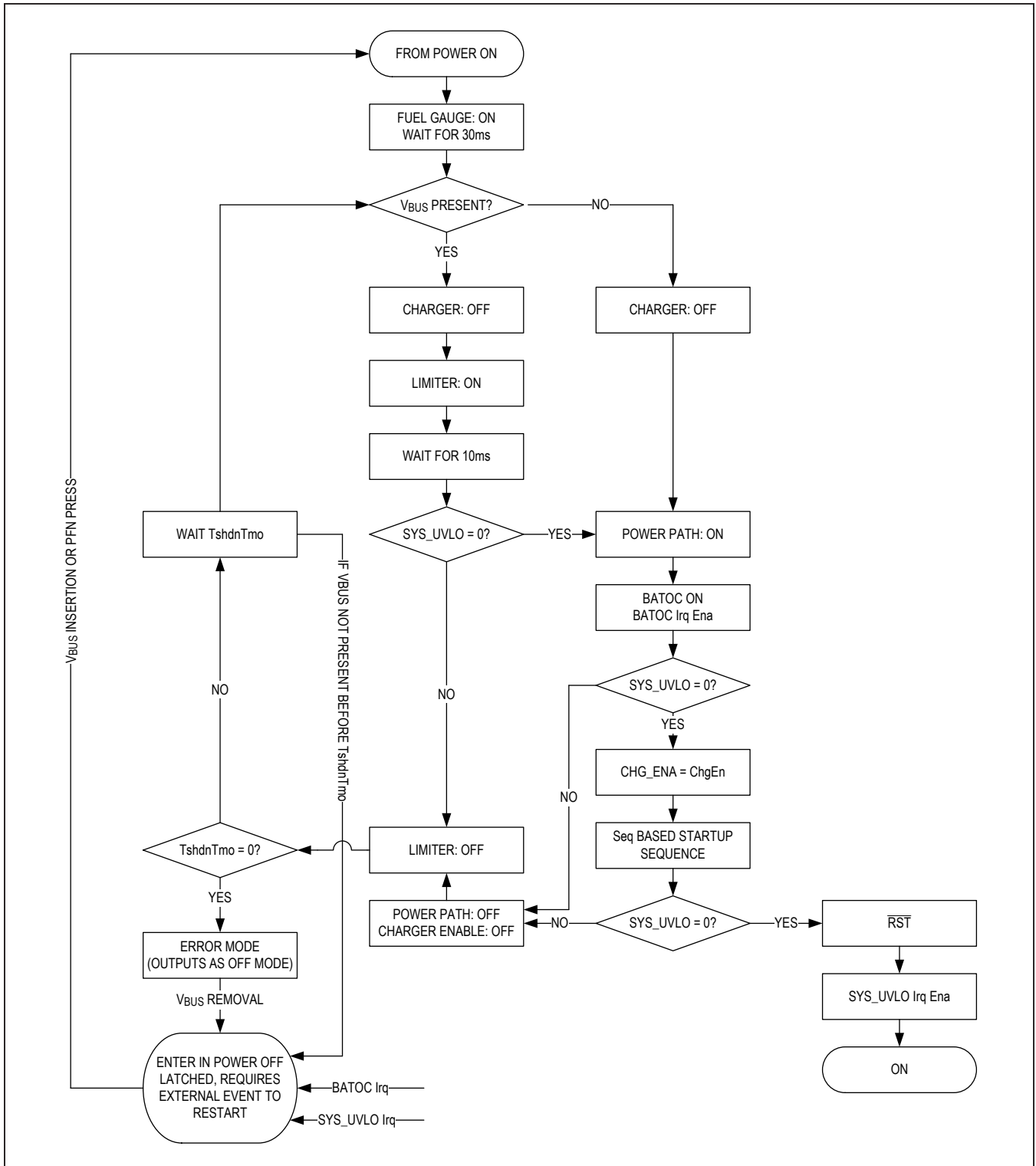


Figure 2. The full MAX20303 Boot Sequence

### Power Sequencing

The sequencing of the switching regulators, LDOs, and charge pump during power-on is configurable. See each regulator’s sequencing bits for details. Regulators can turn on at one of three points during the power-on process: 75ms after the power-on event, at the time the  $\overline{RST}$  signal is released, or at two points in between. The two points between SYS and  $\overline{RST}$  are fixed proportionally to the duration of the Power-On Reset (POR) process ( $t_{RST}$ ). The timing relationship is presented graphically in [Figure 3](#).

Alternatively, the regulators can remain off by default and turn on with an I<sup>2</sup>C command after  $\overline{RST}$  is released.

LDO2 can be configured to be always-on as long as SYS or BAT is present.

The SYS voltage is monitored during the power-on sequence. If  $V_{SYS}$  falls below  $V_{SYS\_UVLO\_F}$  during the sequencing process with a valid voltage at CHGIN, the process repeats from the point where SYS was enabled to allow more time for the voltage to stabilize. If there is not a valid voltage at CHGIN, the device returns to the OFF state to avoid draining the battery. Power is also turned off if BAT experiences a current greater than  $I_{BAT\_OC\_R}$  for more than  $t_{BAT\_OC\_D}$ .

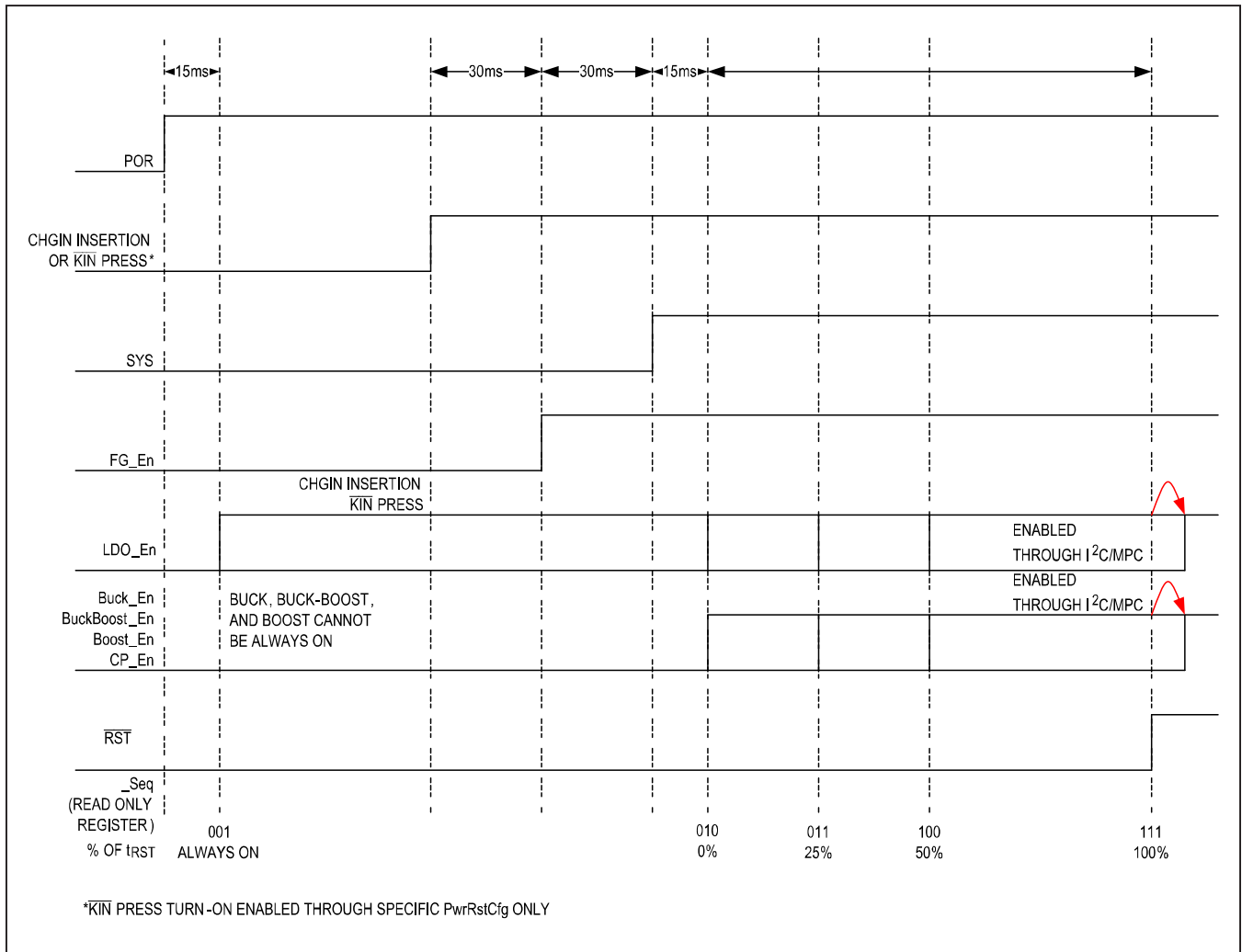


Figure 3. Reset Sequence Programming

### Current Sink

In addition to several voltage regulators, the MAX20303 also includes three low-dropout linear current regulators from LED\_ to GND. The sink current of each current regulator is independently programmable through its respective LED\_ISet[4:0] bits in direct registers LED\_Direct (0x2D–0x2F). The current regulators can be programmed to sink 0.6mA to 30mA with configurable step sizes and are ideal for sinking current from external LEDs. The LEDIStep[1:0] bits in direct register LEDStepDirect (0x2C) control the size of the current steps for all current sinks. This step size also sets an effective limit on the sinking current as the number of steps remains constant while the step size varies. Current sinks are enabled through an I<sup>2</sup>C command, by an internal charger status signal, or by an external MPC pin allowing for LED status indicators. Note that the current sinks always draw quiescent current when tied to an MPC\_ control or status signal regardless of the MPC\_ or status state.

### System Load Switch

An internal 80mΩ (typ) MOSFET connects BAT to SYS when no voltage source is available on CHGIN. When an external source is detected at CHGIN, this switch opens and SYS is powered from the input source through the input current limiter. The SYS-to-BAT switch also prevents V<sub>SYS</sub> from falling below V<sub>BAT</sub> when the system load exceeds the input current limit. If V<sub>SYS</sub> drops to V<sub>BAT</sub> due to the current limit, the BAT-SYS switch turns on so the load is supported by the battery. If the system load continuously exceeds the input current limit, the battery is not charged. This is useful for handling loads that are nominally below the input current limit but have high current peaks exceeding the input current limit. During these peaks, battery energy is used, but at all other times the battery charges.

### Smart Power Selector

The smart power selector seamlessly distributes power from the external CHGIN input to the BAT and SYS nodes. With both an external adapter and battery connected, the smart power selector basic functions are:

- When the system load requirements are less than the input current limit, the battery is charged with residual power from the input.
- When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load.
- When the battery is connected and there is no external power input, the system is powered from the battery.

### Input Limiter

The input limiter distributes power from the external adapter to the system load and battery charger. In addition to the input limiter's primary function of passing power to the system load and charger, it performs several additional functions to optimize use of available power.

**Invalid CHGIN Voltage Protection:** If CHGIN is above the overvoltage threshold, the device enters overvoltage lockout (OVL). OVL protects the MAX20303 and downstream circuitry from high-voltage stress up to +28V and down to -5.5V. During positive OVL, the internal circuit remains powered and an interrupt is sent to the host. The negative voltage protection disconnects CHGIN and the device is powered only by BAT. The charger turns off and the system load switch closes, allowing the battery to power SYS. CHGIN is also invalid if it is less than V<sub>BAT</sub>, or less than the USB undervoltage threshold. With an invalid input voltage, the BAT-SYS load switch closes and allows the battery to power SYS.

**CHGIN Input Current Limit:** The CHGIN input current is limited to prevent input overload. The input current limit is controlled by I<sup>2</sup>C. To accommodate systems with a high in-rush current, the limiter includes a programmable blanking time during which the input current limit increases to I<sub>LIM\_MAX</sub>.

**Thermal Limiting:** In case the die temperature exceeds the normal limit (T<sub>CHG\_LIM</sub>), the MAX20303 attempts to limit temperature increase by reducing the input current from CHGIN. In this condition, the system load has priority over the charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit (T<sub>CHGIN\_SHDN</sub>), no input current is drawn from CHGIN and the battery powers the entire system load.

**Adaptive Battery Charging:** While the system is powered from CHGIN, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, an adaptive charger control loop reduces charge current to prevent V<sub>SYS</sub> from collapsing. When the charge current is reduced below 50% due to I<sub>LIM</sub> or T<sub>CHG\_LIM</sub> limits, the timer clock operates at half speed. When the charge current is reduced below 20% due to I<sub>LIM</sub> or T<sub>CHG\_LIM</sub> limits, the timer clock is paused.

**Fast-Charge Current Setting:** The MAX20303 uses an external resistor connected from SET to GND to set the fast-charge current. The precharge and charge-termination currents are programmed as a percentage of this value by opcode 0x14. The fast-charge current resistor can be calculated as:

$$R_{SET} = K_{SET} \times V_{SET} / I_{FChg}$$

where  $K_{SET}$  has a typical value of 2000A/A and  $V_{SET}$  has a typical value of +1V. The range of acceptable resistors for  $R_{SET}$  is 4kΩ to 400kΩ.

A capacitive load on SET can cause instability of the charger if the condition  $(C_{SET} < 5\mu s/R_{SET})$  pF is violated.

**SAR ADC/Monitor MUX**

In order to simplify system monitoring, the MAX20303 includes a voltage monitor multiplexer (MUX). The I<sup>2</sup>C controlled MUX connects the MON pin to the scaled value of one of six voltage regulators, BAT, or SYS. A resistive divider scales the voltage to one of four ratios determined by MONRatioCfg[1:0] (opcode 0x50, Table 117). Because the MUX can only tolerate voltages up to +5.5V,  $V_{CHGIN}$ ,  $V_{CPOUT}$ , and  $V_{BSTOUT}$  are not available to MON.

An internal ADC reads the remaining voltage rails and performs system tasks such as JEITA temperature monitoring and SYS tracking during haptic driver operations. Manual ADC measurements are initiated by writing the desired channel to ADC\_Measure\_Launch (opcode 0x53, Table 121) and reading the response from APDataIn0-3. The ADC can also measure the MON voltage when the MUX is enabled with a 1:1 ratio. The full-scale range of the ADC for different voltage rails is detailed in Table 2.

**JEITA Monitoring with Charger Control**

To enhance safety when charging Li+ batteries, the MAX20303 includes JEITA-compliant temperature monitoring. A resistive divider is formed on THM by attaching a pullup resistor to TPU and connecting the thermistor of a battery-pack (do not exceed 1mA load on TPU). The divider output is read by the internal ADC when JEITA monitoring is enabled and the resulting temperature measurement places the battery into one of

**Table 2. SAR ADC Full-Scale Voltages and Conversions**

VOLTAGE RAIL	AVAILABLE RANGE	CONVERSION (V)
SYS	+2.6V to +5.5V	(Result[7:0] * 5.5)/255
MON	0V to +5.5V	(Result[7:0] * 5.5)/255
THM	0% to 100% $V_{DIG}$	(Result[7:0] * 100)/255
CHGIN	+3V to +8V	(Result[7:0] * 8.25)/255
CPOUT	+3V to +8V	(Result[7:0] * 8.25)/255
BSTOUT	+3V to +21V	(Result[7:0] * 21.0)/255

five temperature zones: cold, cool, room, warm, and hot. Zone-specific temperature limits and charging behavior are fully configurable through the ChargerThermalLimits\_Config\_Write (opcode 0x16, Table 69) and ChargerThermalReg\_Config\_Write (opcode 0x18, Table 73) commands detailed in Table 69 and Table 73. Some example profiles are included in Figure 4. It is important to note that, because battery temperature is measured by the internal ADC, JEITA monitoring is unavailable when automatic level compensation is enabled in the haptic driver.

**Haptic Driver**

The MAX20303 features a versatile, integrated haptic driver. The driver allows for real time control of haptic devices through PWM or I<sup>2</sup>C as well as the ability to run haptic patterns from internal RAM. For added flexibility, the driver is capable of driving both Linear Resonant Actuator (LRA) and Eccentric Rotating Mass (ERM) actuators.

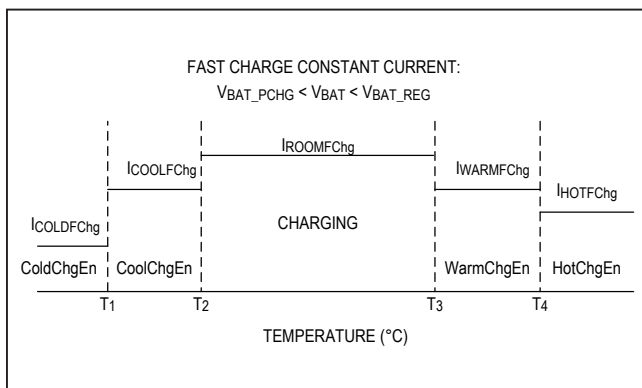


Figure 4a. Sample JEITA Pre Charge Profile

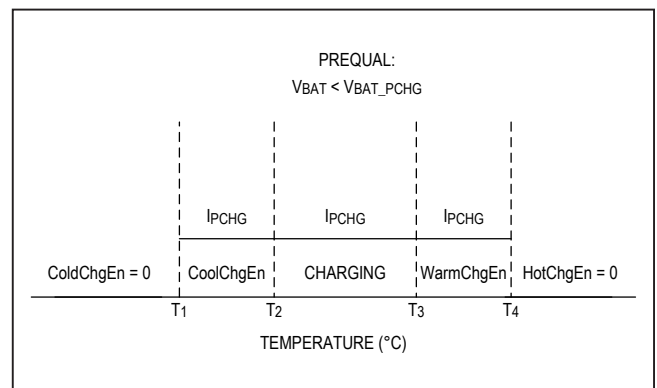


Figure 4b. Sample JEITA Fast Charge Profile

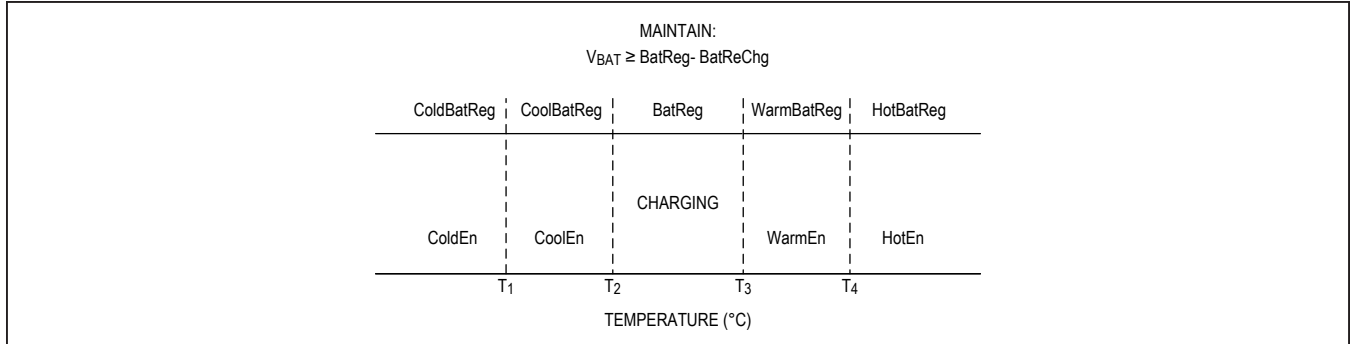


Figure 4c. Sample JEITA Maintain Charge Profile

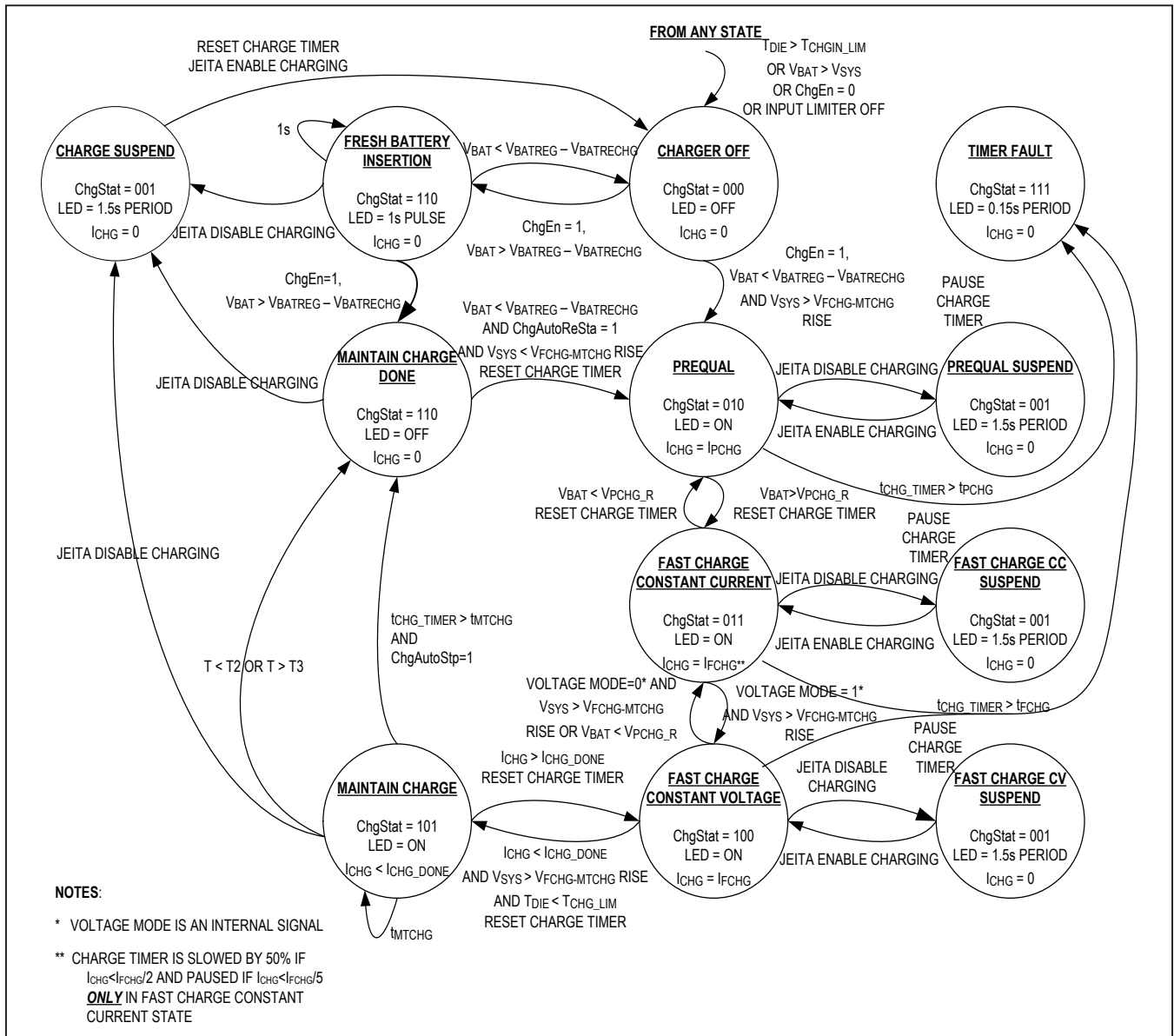


Figure 5. Charger State Diagram



**ERM**

An ERM is the simplest haptic actuator to drive. The driving signal is taken directly as the output of an integrated H-bridge, allowing for bidirectional operation of the actuator. To configure the MAX20303 to drive an ERM, the HptSel bit must be set to 0 using the opcode 0xA0 or 0xAD ([Table 127](#) and [Table 153](#)).

**LRA**

Unlike the on-off control of an ERM, LRAs require a sinusoidal driving signal. The MAX20303 realizes this with a Class-D amplifier that converts the driver input to a sinusoidal output. Note that any changes made to the output amplitude take effect in the next period of the sinusoid.

An LRA's vibration magnitude is maximized when the driving signal matches the LRA's resonant frequency. To ensure the haptic driver closely tracks this frequency, the MAX20303 includes an auto-resonance tracking feature. Resonance tracking is enabled by setting the EmfEn bit to 1 with opcode 0xA0 or 0xAD. The range of resonant frequencies that can be reliably driven is 120Hz to 305Hz. Enabling resonance tracking is strongly recommended when driving an LRA to ensure maximum driving efficiency and amplitude.

To select LRA mode, set the HptSel bit to 1 using opcode 0xA0 or 0xAD.

**Driver Amplitude**

The haptic driver features a configurable voltage basis for the amplitude of the driving signal. Setting this basis, referred to as the full-scale voltage ( $V_{FS}$ ), configures the maximum amplitude of the driver output. It is set using HptVfs[7:0] with opcode 0xA2 or 0xB2 ([Table 131](#) and [Table 163](#)) and has a range of 0V to 5.5V (LSB = 21.57mV). Since the H-bridge is supplied by  $V_{SYS}$ , the actual full-scale voltage of the driver at any given moment is the minimum of the value stored in HptVfs[7:0] and  $V_{SYS}$ .

Once  $V_{FS}$  has been set, all driver amplitudes are scaled as a percentage of the full-scale voltage. The resolution of the amplitude is always  $V_{SYS}/128$ . Therefore, the effective resolution of the amplitude scales with the  $V_{FS}/V_{SYS}$  ratio. For example, if  $V_{FS} = V_{SYS}/2$ , the effective resolution is 6 bits.

**Automatic Level Compensation**

Because  $V_{SYS}$  can vary over time, the driver must adjust its output duty cycle to maintain a constant reference to the full-scale voltage. An Automatic Level Compensation (ALC) function measures  $V_{SYS}$  and handles this adjustment. ALC can be enabled by setting the AlcMod bit to 1 using opcode

0xA0 or 0xAD and uses the MAX20303's internal ADC to monitor  $V_{SYS}$ . The ALC function then scales the haptic driver's duty cycle as needed to maintain the programmed driver amplitude. If ALC is not enabled,  $V_{SYS}$  is assumed to be  $V_{FS}$ .

**Haptic UVLO**

Additionally,  $V_{SYS}$  is measured after the driver is enabled but prior to starting a vibration. At any moment, if  $V_{SYS}$  goes below the programmed UVLO value, which is set through HptSysUVLO[7:0] with opcode 0xA6 ([Table 139](#)), the vibration event is aborted and the haptic driver is locked. See the [Haptic Driver Lock](#) section for details regarding restarting vibration if a haptic UVLO condition is reached.

The time required to perform the  $V_{SYS}$  measurement, as well as other startup delays, results in an initial latency of the haptic driver. To avoid partial pattern skipping in real-time modes, vibration patterns should be provided at least t<sub>HD\_START</sub> after enabling the desired real-time vibration mode (PPWM or RTI<sup>2</sup>C).

**Vibration Timeout**

A vibration timeout parameter is programmable through I<sup>2</sup>C. If a vibration lasts longer than the programmed timeout period, the vibration is aborted. The timeout period is stored in HptDrvTmo[5:0] (LSB = 1s), which can be written using opcode 0xB7 ([Table 173](#)). Writing code "000000" disables the timeout function. See the [Haptic Driver Lock](#) section for details regarding restarting vibration if a timeout is reached.

**Overcurrent/Thermal Protection**

The haptic driver also includes overcurrent and thermal shutdown protection. While the haptic driver is active, the MAX20303 monitors the current from DRP and DRN. If overcurrent protection is enabled (HptOCProtDis = 0) and the DRP or DRN current exceeds I<sub>HD\_OC\_THR</sub>, the haptic driver issues a fault, aborts vibration, and enters the locked state.

Thermal protection allows the MAX20303 to immediately shut down the haptic driver should the die temperature exceed T<sub>HD\_OC\_THR</sub>. This feature is enabled by setting HptThmProtDis = 0.

See the [Haptic Driver Lock](#) section for details regarding restarting vibration if an overcurrent or overtemperature condition is reached.

### Haptic Driver Lock

If the MAX20303 detects a fault in the haptic driver, vibrations in progress are aborted and the haptic driver is locked by the HptLock bit. The user must manually clear the HptLock bit using opcode 0xA8 (Table 143) in order to run a new vibration attempt. A fault occurs under any of the following conditions:  $V_{SYS}$  drops below the threshold programmed in HptSysUVLO[7:0] (SystemError 0x25), an overcurrent is detected on DRN or DRP (SystemError = 0x20, 0x21, 0x22, or 0x23), the die temperature exceeds the thermal protection threshold (SystemError = 0x24), or a vibration duration exceeds the timeout period stored in HptDrvTmo[5:0] (SystemError 0x04). Writing any value other than 0x00 with opcode 0xA8 will set HptLock high and disable the driver output.

### Interface Modes

There are a total of four interface modes for controlling the haptic driver. These include two real-time modes and two stored memory modes. The haptic driver mode is set through HptDrvMode[4:0] with the direct-access I<sup>2</sup>C register 0x31. Selecting an operation mode also enables the driver. In addition, HptDrvEn must be set and kept to 1 before setting HptDrvMode[4:0] and for the whole duration of vibration. Once vibration finishes, HptDrvMode[4:0] must be set to “00000” before the haptic driver may be disabled via HptDrvEn = 0 for power savings.

### Pure-PWM (PPWM)

PPWM mode offers real-time control of the haptic driver. Patterns are generated by applying a PWM signal to the MPC\_ pin selected by HptDrvMode[4:0]. The duty cycle of the applied signal determines the amplitude of the driving signal, scaled by  $V_{FS}$ . The driving direction is centered about a 50% duty cycle. A duty cycle of 0% to 47.5% produces a (100 to 0)% $V_{FS}$  amplitude in the negative direction and a duty cycle of 52.5% to 100% produces a (0 to 100)% $V_{FS}$  amplitude in the positive direction. The region between 47.5% and 52.5% duty cycle is a dead zone and inputs within this range correspond to a null output.

A timeout feature prevents idle PWM inputs from causing unwanted vibrations of the haptic motor. If the input signal remains at 0% duty cycle or 100% duty cycle for more than 2.56ms, the output is null and vibration stops. As such, the MPC\_ input must remain dynamic to produce a continuous output.

### Real-Time I<sup>2</sup>C (RTI<sup>2</sup>C)

Similar to PPWM mode, RTI<sup>2</sup>C mode offers real-time control of the haptic driver. The direct register HptRTI2CAmp (0x32) determines the amplitude of the output signal. The lower seven bits of the register (HptRTI2CAmp[6:0]) set the amplitude as a percentage of  $V_{FS}$  and the MSB (HptRTI2CSign) sets the direction of rotation. 100% amplitude, reverse drive, for example, is produced by setting HptRTI2CAmp to 0x7F (0b01111111).

Once RTI<sup>2</sup>C mode is enabled through HptDrvMode[4:0], the haptic driver continuously outputs the amplitude and direction defined by the latest data in HptRTI2CAmp. In order to generate haptic patterns, the HptRTI2CAmp register must receive new data.

### External Triggered Stored Pattern (ETRG)

In ETRG mode, a rising edge on an MPC\_ pin or a 0-to-1 transition of the HptExtTrig bit in direct I<sup>2</sup>C register 0x31 initiates a vibration sequence. The sequence is contained in six registers and comprises an overdrive (startup) amplitude, active drive amplitude, braking amplitude, and the duration of each driving behavior.

Amplitudes contained in ETRGOdAmp[7:0], ETRGActAmp[7:0], and ETRGBrkAmp[7:0], which are set through opcode 0xA2–0xA4 or 0xB3 (Table 131 thru Table 136 and Table 165), follow the same format as HptRTI2CSign + HptRTI2CAmp[6:0] in direct I<sup>2</sup>C register 0x32 (i.e., the lower-seven bits store the amplitude as a percentage of  $V_{FS}$  and the MSB determines the direction).

The trigger input is selected when the driver enters ETRG mode via HptDrvMode[4:0] in direct I<sup>2</sup>C register 0x31. In order to properly register the rising edge, the trigger signal must remain high for a few clock cycles of the driver. Once the sequence begins, the haptic driver follows the duration values stored in ETRGOdDur[7:0], ETRGActDur[7:0], and ETRGBrkDur[7:0]. It is possible, however, to extend the active drive time by leaving the trigger high longer than the time specified in ETRGActDur[7:0]. Doing so will cause the driver to output the amplitude stored in ETRGActAmp[7:0] until a falling edge is detected. Once the trigger signal falls low, the brake sequence executes.

### RAM Stored Haptic Pattern (RAMHP)

The final method of controlling the haptic driver is RAMHP mode. The MAX20303 contains an internal 256 x 24 bit RAM in which haptic patterns are stored. By storing haptic sequences in RAM at startup, the driver can perform sophisticated haptic sequences upon receipt of a trigger signal as in ETRG mode. The direct I<sup>2</sup>C register HptPatRAMAddr (0x33) specifies the RAM address where the sequence begins.

RAM should be loaded when the MAX20303 comes out of Off mode. To write data to the RAM, the HptRAMEn bit in direct register HptDirect1 (0x31) must first be set high. Next, writing a value to the direct register HptRAMAddr (0x28) specifies the RAM address in which data written to HptDataH, HptDataM, and HptDataL (0x29, 0x2A, and 0x2B, respectively) is stored. It is possible to read back data from RAM. Writing an address to HptRAMAddr, then initiating an I<sup>2</sup>C read transaction of register 0x29, will allow readback of the three bytes stored in the RAM address. RAM read and write procedures are depicted graphically in [Figure 6](#).

A haptic pattern is composed of multiple pattern samples. Pattern samples define the amplitude, duration, wait time, transition, and repetition of a segment of a haptic pattern.

These samples are defined in three bytes and written to RAM through HptDataH, HptDataM, and HptDataL. HptDataH contains the sign of the sample’s amplitude (AxSign), the upper-five bits of the amplitude (Ax[6:2]), and instructions to the haptic driver on handling the pattern sample (nLSx). HptDataM contains the lower two bits of the sample’s amplitude (Ax[1:0]), the duration of the sample (Dx), and the upper bit of the wait time before the next sample in the pattern (Wx[4]). HptDataL contains the lower four bits of the wait time (Wx[3:0]) and the repetition behavior (RPTx). [Table 3](#) describes the definition of a pattern sample and [Figure 7](#) provides a sample haptic pattern with corresponding waveform.

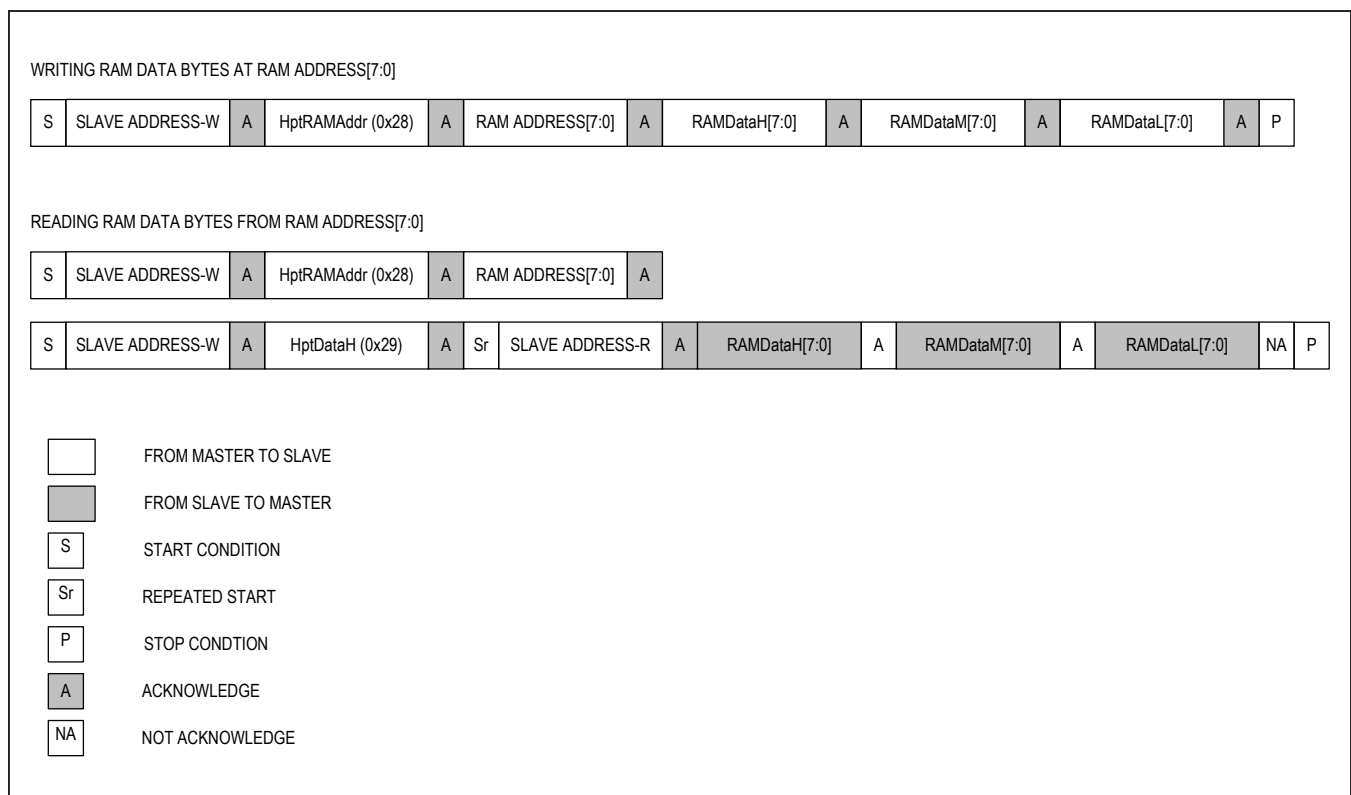


Figure 6. Read and Write Processes for RAM

**Table 3. RAMHP Pattern Storage Format**

ADDRESS	0x28-0x2B							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
HptRAMAddr	HptRAMAddr[7:0]							
HptDataH	nLSx[1:0]		AmpSign	Amp[6:2]				
HptDataM	Amp[1:0]		Dur[4:0]				Wait[4]	
HptDataL	Wait[3:0]				RPTx[3:0]			
HptRAMAddr [7:0]	The RAM address in which the pattern sample is stored							
nLSx[1:0]	Sets the behavior of a sample in the pattern. 00 = Current sample is the last sample in the pattern 01 = Current sample is not the last sample in the pattern 10 = Interpolate current sample with next sample 11 = Current sample is the last sample in the pattern. Repeat the entire pattern RPTx[3:0] times							
AmpSign[1:0]	Sign of haptic amplitude in current sample 0 = Positive 1 = Negative							
Amp[6:2]	Sets the amplitude of pattern sample x as a 7-bit percentage of $V_{FS}$ and a 1-bit direction. See HptVfs[7:0] in Table 131.							
Dur[4:0]	Sets the duration of time the driver outputs the amplitude of the current sample in increments of 5ms 00000 = 0ms 00001 = 5ms ... 11110 = 150ms 11111 = 155ms							
Wait[4:0]	Sets the duration of time the driver waits at zero amplitude before the next sample in increments of 5ms 00000 = 0ms 00001 = 5ms ... 11110 = 150ms 11111 = 155ms							
RPTx[3:0]	Sets the number of times to repeat the sample before moving to the next sample in the pattern. If nLSx[1:0] = 11, this sets the number of times to repeat the whole pattern. 0000 = Repeat 0 times 0001 = Repeat 1 time ... 1110 = Repeat 14 times 1111 = Repeat 15 times							

nLS0[1:0]	Amp[7:0]	Dur[4:0]	Wait[4:0]	Rpt[3:0]
nLS <sub>PREV</sub>	Amp <sub>PREV</sub>	Dur <sub>PREV</sub>	Wait <sub>PREV</sub>	Rpt <sub>PREV</sub>
01	A0	00010	00001	0001
01	A1	00011	00000	0010
10	A2	00011	00000	X
10	A3	00011	00000	X
11	A4	DC	00010	0010

← END OF PREVIOUS PATTERN

Figure 7a. Sample Pattern Stored in RAM

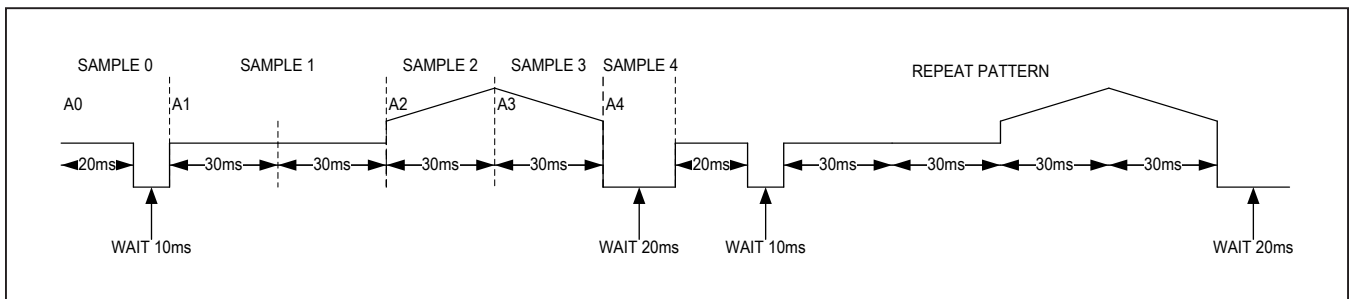


Figure 7b. Haptic Driver Output of Stored Pattern

## Fuel Gauge

### ModelGauge Theory of Operation

The MAX20303 fuel gauge is based on the MAX17048 stand-alone fuel gauge and simulates the internal, non-linear dynamics of a Li+ battery to determine its State of Charge (SOC). The sophisticated battery model considers impedance and the slow rate of chemical reactions in the battery. ModelGauge performs best with a custom model, obtained by characterizing the battery at multiple discharge currents and temperatures to precisely model it. At power-on reset (POR), the ICs have a preloaded ROM model that performs well for some batteries. For more details on the fuel gauge, refer to the MAX17048 data sheet.

### Fuel-Gauge Performance

In coulomb counter-based fuel gauges, SOC drifts because offset error in the current-sense ADC measurement accumulates over time. Instantaneous error can be very

small, but never precisely zero. Error accumulates over time in such systems (typically, 0.5%–2% per day) and requires periodic corrections. Some algorithms correct drift using occasional events and, until such an event occurs, the algorithm’s error is boundless:

- Reaching predefined SOC levels near full or empty
- Measuring the relaxed battery voltage after a long period of inactivity
- Completing a full charge/discharge cycle

ModelGauge requires no correction events because it uses only voltage, which is stable over time. The ModelGauge remains accurate despite the absence of any of the above events; it neither drifts nor accumulates error over time.

To correctly measure performance of a fuel gauge as experienced by end-users, exercise the battery dynamically. Accuracy cannot be fully determined from only simple cycles.

### Battery Voltage and State of Charge

Open-circuit voltage (OCV) of a Li+ battery uniquely determines its SOC; one SOC can have only one value of OCV. In contrast, a given  $V_{CELL}$  can occur at many different values of OCV because  $V_{CELL}$  is a function of time, OCV, load, temperature, age, impedance, etc.; one value of OCV can have many values of  $V_{CELL}$ . Therefore, one SOC can have many values of  $V_{CELL}$ , so  $V_{CELL}$  cannot uniquely determine SOC.

Even the use of sophisticated tables to consider both voltage and load results in significant error due to the load transients typically experienced in a system. During charging or discharging, and for approximately 30 min after,  $V_{CELL}$  and OCV differ substantially, and  $V_{CELL}$  has been affected by the preceding hours of battery activity. ModelGauge uses voltage comprehensively.

### Temperature Compensation

For best performance, the host microcontroller must measure battery temperature periodically, and compensate the RCOMP ModelGauge parameter accordingly, at least once per minute. Each custom model defines constants RCOMP0 (0x97, default), TempCoUp (-0.5, default), and TempCoDown (-5.0, default). To calculate the new value of CONFIG.RCOMP:

```
// T is battery temperature (degrees Celsius)
if (T > 20) {
    RCOMP = RCOMP0 + (T - 20) x TempCoUp;
}
else {
    RCOMP = RCOMP0 + (T - 20) x TempCoDown;
}
```

### Impact of Empty-Voltage Selection

Most applications have a minimum operating voltage below which the system immediately powers off (empty voltage). When characterizing the battery to create a custom model, choose empty voltage carefully. Capacity unavailable to the system increases at an accelerating rate as empty voltage increases.

To ensure a controlled shutdown, consider including operating margin into the fuel gauge based on some low threshold of SOC, for example shutting down at 3% or 5%. This utilizes the battery more effectively than adding error margin to empty voltage.

### Battery Insertion

When the battery is first inserted into the system, the fuel-gauge IC has no previous knowledge about the battery's SOC. Assuming that the battery is relaxed, the IC translates its first  $V_{CELL}$  measurement into the best initial estimate

of SOC. Initial error caused by the battery not being in a relaxed state diminishes over time, regardless of loading following this initial conversion. While SOC estimated by a coulomb counter diverges, ModelGauge SOC converges, correcting error automatically. Initial error has no long-lasting impact.

### Battery Insertion Debounce

Any time the IC powers on or resets (see the [VRESET/ID Register \(0x18\)](#) section), it estimates that OCV is the maximum of 16  $V_{CELL}$  samples (1ms each, full 12-bit resolution). OCV is ready 17ms after battery insertion, and SOC is ready 175ms after that.

### Battery Swap Detection

If  $V_{CELL}$  falls below  $V_{RST}$ , the IC quick-starts once  $V_{CELL}$  returns above  $V_{RST}$ . This handles battery swap; the SOC of the previous battery does not affect that of the new one. See the [Quick-Start and VRESET/ID Register \(0x18\)](#) sections.

### Quick-Start

If the IC generates an erroneous initial SOC, the battery insertion and system power-up voltage waveforms must be examined to determine if a quick-start is necessary, as well as the best time to execute the command. The IC samples the maximum  $V_{CELL}$  during the first 17ms. See the [Battery Insertion Debounce](#) section. Unless  $V_{CELL}$  is fully relaxed, even the best sampled voltage can appear greater or less than OCV. Therefore, quick-start must be used cautiously.

Most systems should not use quick-start because the ICs handle most startup problems transparently, such as intermittent battery-terminal connection during insertion. If battery voltage stabilizes faster than 17ms, do not use quick-start.

The quick-start command restarts fuel-gauge calculations in the same manner as initial power-up of the IC. If the system power-up sequence is so noisy that the initial estimate of SOC has unacceptable error, the system microcontroller may be able to reduce the error by using quick-start. A quick-start is initiated by a rising edge on the QSTRT pin, or by writing 1 to the quick-start bit in the MODE register.

### Power-On Reset (POR)

POR includes a quick-start, so only use it when the battery is fully relaxed. See the [Quick-Start](#) section. This command restores all registers to their default values. After this command, reload the custom model. See the [CMD Register \(0xFE\)](#) section.

### Hibernate Mode

The ICs have a low-power hibernate mode that can accurately fuel gauge the battery when the charge/discharge rate is low. By default, the device automatically enters and exits hibernate mode according to the charge/discharge rate, which minimizes quiescent current (below 5 $\mu$ A) without compromising fuel-gauge accuracy. The ICs can be forced into hibernate or active modes. Force the IC into hibernate mode to reduce power consumption in applications with less than C/4-rate maximum loading. For applications with higher loading, Maxim recommends the default configuration of automatic control of hibernate mode.

In hibernate mode, the device reduces its ADC conversion period and SOC update to once per 45s. See the [HIBRT Register \(0x0A\)](#) section for details on how the IC automatically enters and exits hibernate mode.

### Alert Interrupt

The ICs can interrupt a system microcontroller with five configurable alerts. All alerts can be disabled or enabled with software. When the interrupt occurs, the system microcontroller can determine the cause from the STATUS register.

When an alert is triggered, the IC drives the  $\overline{\text{ALRT}}$  pin logic-low and sets CONFIG.ALRT = 1. The  $\overline{\text{ALRT}}$  pin remains logic-low until the system software writes CONFIG.ALRT = 0 to clear the alert. The alert function is enabled by default, so any alert can occur immediately upon power-up. Entering sleep mode clears no alerts.

### Sleep Mode

In sleep mode, the IC halts all operations, reducing current consumption to below 1 $\mu$ A. After exiting sleep mode, the IC continues normal operation. In sleep mode, the IC does not detect self-discharge. If the battery changes state while the IC sleeps, the IC cannot detect it, causing SOC error. Wake up the IC before charging or discharging. To enter sleep mode, write MODE.EnSleep = 1 and either:

Hold SDA and SCL logic-low for a period for  $t_{\text{SLEEP}}$ . A rising edge on SDA or SCL wakes up the IC.

Write CONFIG.SLEEP = 1. To wake up the IC, write CONFIG.SLEEP = 0. Other communication does not wake up the IC. POR does wake up the IC.

Therefore, applications that can tolerate 4 $\mu$ A should use hibernate mode rather than Sleep mode.

### I<sup>2</sup>C Interface

The MAX20303 uses the two-wire I<sup>2</sup>C interface to communicate with a host microcontroller. The configuration settings and status information provided through this interface are detailed in the register descriptions. To simplify the use of existing code and drivers designed for interfacing with the ModelGauge fuel gauge, the MAX20303 appears as two devices on an I<sup>2</sup>C bus. The main device controlling the regulators, charger, and other system functions has the seven-bit slave address 0b0101000 (0x50 for writes, 0x51 for reads). Accessing the fuel gauge is done using the seven-bit slave address 0b0110110 (0x6C for writes, 0x6D for reads).

## Applications Information

### I<sup>2</sup>C Interface

The MAX20303 contains an I<sup>2</sup>C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

### Start, Stop, And Repeated Start Conditions

When writing to the MAX20303 using I<sup>2</sup>C, the master sends a START condition (S) followed by the MAX20303 I<sup>2</sup>C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I<sup>2</sup>C slave. See [Figure 8](#).

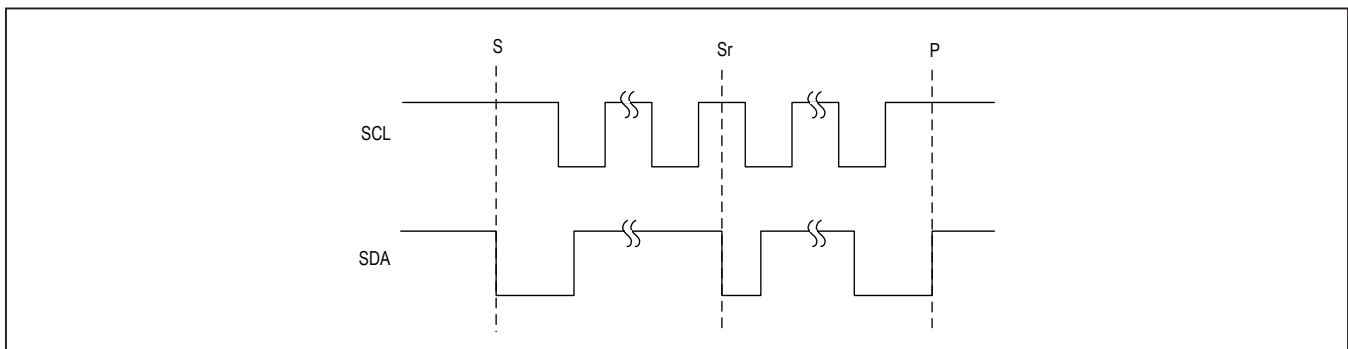


Figure 8. I<sup>2</sup>C START, STOP and REPEATED START Conditions

**Slave Address**

Set the Read/Write bit high to configure the MAX20303 to read mode. Set the Read/Write bit low to configure the MAX20303 to write mode. The address is the first byte of information sent to the MAX20303 after the START condition.

**Bit Transfer**

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the [Start, Stop, And Repeated Start Conditions](#) section). Both SDA and SCL remain high when the bus is not active.

**Single-Byte Write**

In this operation, the master sends an address and two data bytes to the slave device (Figure 9). The following procedure describes the single byte write operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address
- The slave asserts an ACK on the data line only if the address is valid (NAK if not)

- The master sends 8 data bits
- The slave asserts an ACK on the data line
- The master generates a STOP condition

**Burst Write**

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 10). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address
- The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- The master sends 8 data bits
- The slave asserts an ACK on the data line
- Repeat 6 and 7 N-1 times
- The master generates a STOP condition

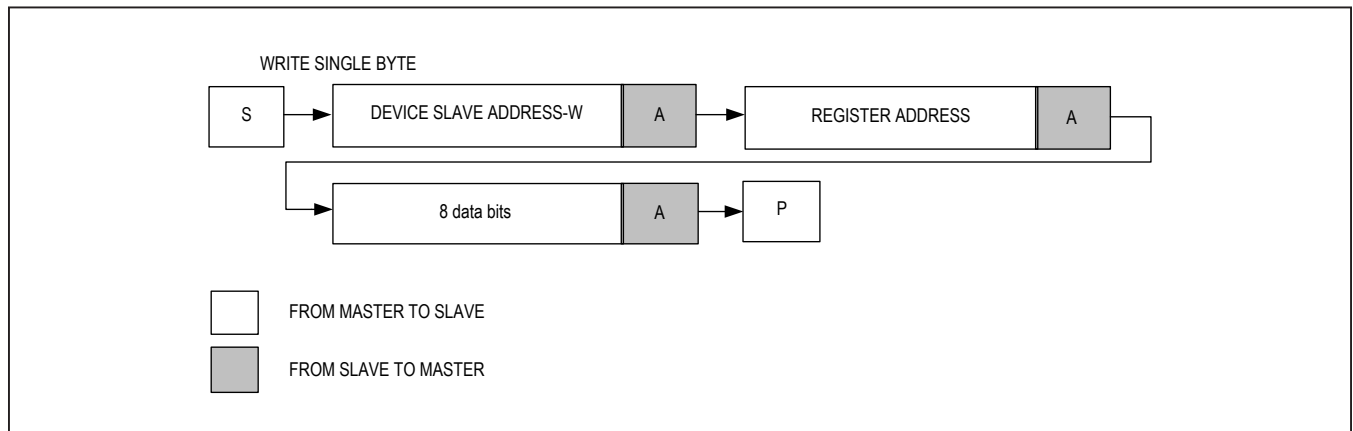


Figure 9. Write Byte Sequence



**Single Byte Read**

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 11). The following procedure describes the single byte read operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address

- The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- The master sends a REPEATED START condition
- The master sends the 7-bit slave address plus a read bit (high)
- The addressed slave asserts an ACK on the data line
- The slave sends 8 data bits
- The master asserts a NACK on the data line
- The master generates a STOP condition

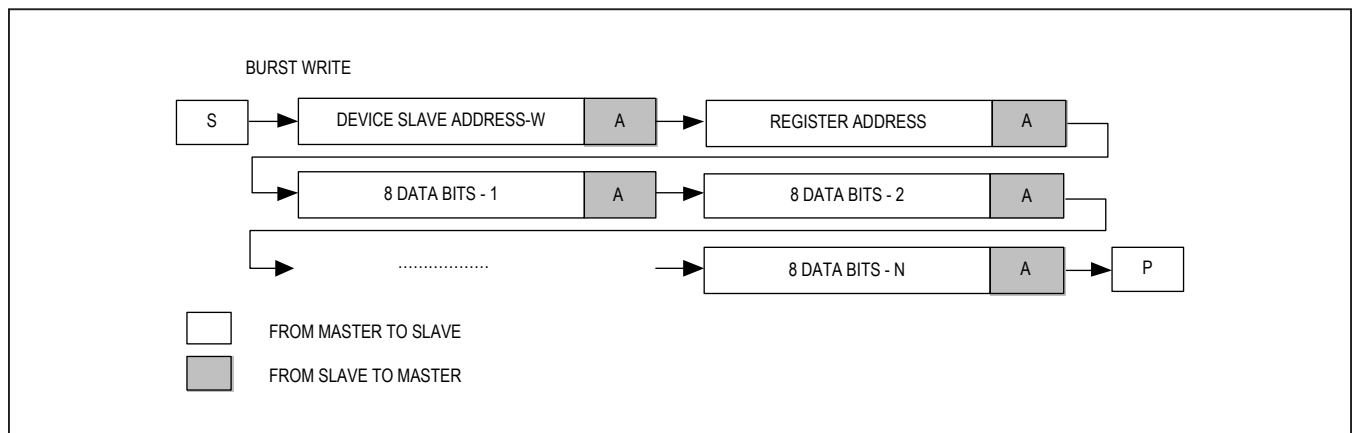


Figure 10. Burst Write Sequence

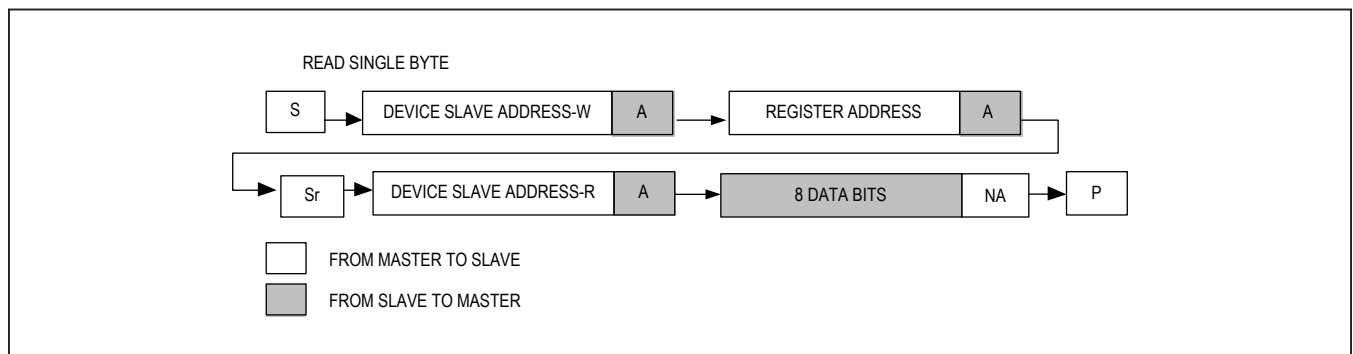


Figure 11. Read Byte Sequence

**Burst Read**

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 12). The following procedure describes the burst byte read operation:

- The master sends a START condition
- The master sends the 7-bit slave address plus a write bit (low)
- The addressed slave asserts an ACK on the data line
- The master sends the 8-bit register address
- The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- The master sends a REPEATED START condition
- The master sends the 7-bit slave address plus a read bit (high)
- The slave asserts an ACK on the data line

- The slave sends 8 data bits
- The master asserts an ACK on the data line
- Repeat 9 and 10 N-2 times
- The slave sends the last 8 data bits
- The master asserts a NACK on the data line
- The master generates a STOP condition

**Acknowledge Bits**

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX20303 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see Figure 13). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

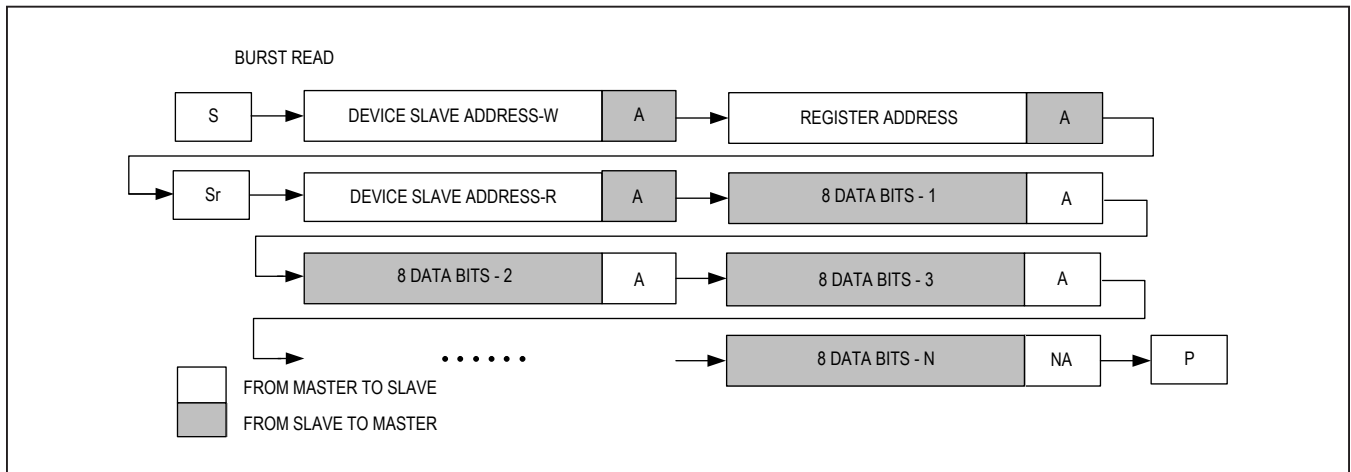


Figure 12. Burst Read Sequence

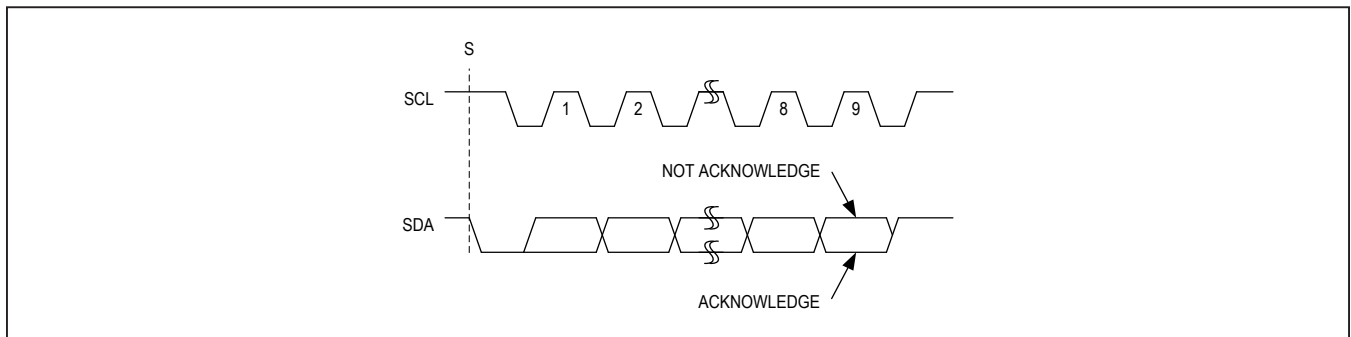


Figure 13. Acknowledge

**Application Processor Interface**

Several of the MAX20303’s functions are controlled by an Application Processor (AP). AP commands read and write configuration settings to the internal registers. Data transfer is handled by the AP controller and is triggered by writes to APCmdOut. There is a 5ms (typ), 9ms (max) latency associated with setting commands. This delay increases if the command requires additional processes such as ADC measurements, haptic autotune, etc. When the transfer is complete, INT goes low, APCmdResponseInt (bit seven of direct register Int2 (0x05)) is set, and the controller writes the value of the received opcode to APResponse. Reading the data in APResponse provides verification of the successful execution of an opcode.

**AP Write**

To set configuration registers, data must first be written to the APDataOut0-5 registers. Tables 47 to 190 detail the functions of each APDataOut\_ register for a given opcode. Once APDataOut0-5 contain the configuration bytes, writing an opcode to APCmdOut signals the controller to transfer data to the internal registers. Note that a write opcode only transfers the number of bytes defined by the command. The controller ignores the contents of all extra APDataOut\_ registers. See Figure 14 for the structure of an AP write procedure with an APResponse opcode check.

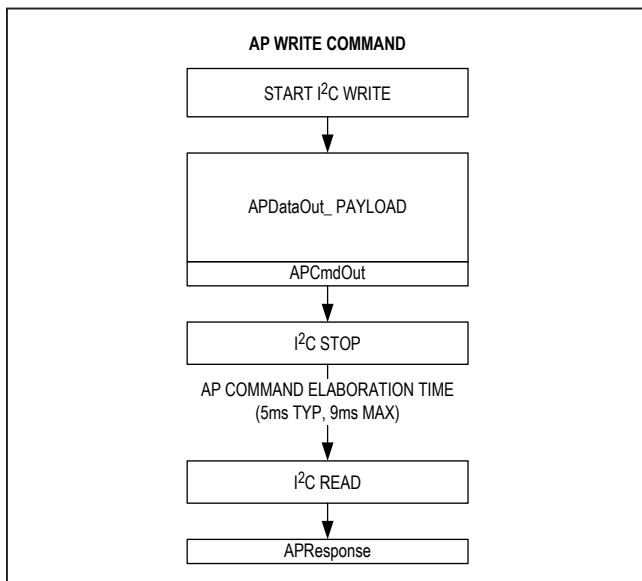


Figure 14. Executing a Write Opcode and Reading the MAX20303 Response

**AP Read**

To read a configuration register, APCmdOut is set to a read opcode. Read opcodes signal the controller to transfer the internal register contents to the APDataIn0-5 registers. When the transfer is complete, APDataIn0-5 contain the stored configuration settings or operation results and can be read over I2C. Because read opcodes expect no inputs, any data stored in APDataOut0-5 is ignored. Figure 15 illustrates the AP read processes.

**AP Launch**

Certain commands trigger additional functions in the MAX20303. These commands, such as ADC\_Measure\_Launch (opcode 0x53) and HPT\_Autotune (opcode 0xAC), may require additional elaboration time for taking measurements and computing the result. When the process is complete, results may be read from APDataIn0-5 as in normal AP Read commands.

**Write-Protected Commands and Fields**

If the factory configured bit WriteProtect is enabled, the AP commands InputCurrent\_Config\_Write (0x10), Charger\_Config\_Write (0x14), and Charger\_ControlWrite (0x1A) are not accessible. If the application processor issues a request to one of these commands, the device will respond with the SysError code MA\_SYSEERROR\_APCMD\_WRITEPROTECT.

A settings are also write protected, but it is possible to write these settings using an additional field in the command that contains a password.

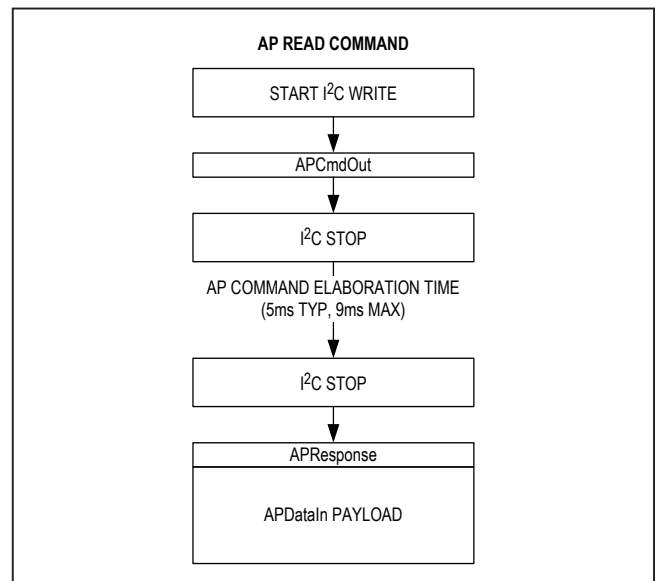


Figure 15. Executing a Read Opcode and Reading the MAX20303 Response

Direct Access I2C Register Map

REGISTER ADDRESS	REGISTER NAME	RW	B7	B6	B5	B4	B3	B2	B1	B0
0x00	HardwareID	R	HardwareID[7:0]							
0x01	FirmwareID	R	FirmwareID[7:0]							
0x03	Int0	COR	ThmStatInt	ChgStatInt	ILimInt	UsbOVPInt	UsbOkInt	ChgThmSdInt	ThmRegInt	ChgTmoInt
0x04	Int1	COR	ThmSDInt	BstFltInt	ThmBuck2Int	ThmBuck1Int	UVLOLDO2Int	UVLOLDO1Int	ThmLDO2Int	ThmLDO1Int
0x05	Int2	COR	APCmdResplnt	SysErrInt	—	LRAALockInt	LRAAActInt	BBstThmInt	SysBatLimInt	ChgSysLimInt
0x06	Status0	R	—	—	—	ThmStat[2:0]		ChgStat[2:0]		
0x07	Status1	R	—	—	ILim	UsbOVP	UsbOk	ChgJEITASD	ChgJEITAReg	ChgTmo
0x08	Status2	R	ThmSD	BstFlt	ThmBuck2	ThmBuck1	UVLOLDO2	UVLOLDO1	ThmLDO2	ThmLDO1
0x09	Status3	R	ApCmdResp	SysErr	—	LRAALock	LRAAAct	BBstThm	SysBatLim	ChgSysLim
0x0B	SystemError	R	SystemError[7:0]							
0x0C	IntMask0	RW	ThmStatIntM	ChgStatIntM	ILimIntM	UsbOVPIntM	UsbOkIntM	ChgJEITASDIntM	ChgJEITARegIntM	ChgTmoIntM
0x0D	IntMask1	RW	ThmSdIntM	BstFltIntM	ThmBuck2IntM	ThmBuck1IntM	UVLOLDO2IntM	UVLOLDO1IntM	ThmLDO2IntM	ThmLDO1IntM
0x0E	IntMask2	RW	APCmdResplntM	SysErrIntM	—	LRAALockIntM	LRAAActIntM	BBstThmIntM	SysBatLimIntM	ChgSysLimIntM
0x0F	APDataOut0	RW	APDataOut0[7:0]							
0x10	APDataOut1	RW	APDataOut1[7:0]							
0x11	APDataOut2	RW	APDataOut2[7:0]							
0x12	APDataOut3	RW	APDataOut3[7:0]							
0x13	APDataOut4	RW	APDataOut4[7:0]							
0x14	APDataOut5	RW	APDataOut5[7:0]							
0x15	APDataOut6	RW	APDataOut6[7:0]							
0x17	APCmdOut	RW	APCmdOut[7:0]							
0x18	APResponse	R	APResponse[7:0]							
0x19	APDataIn0	R	APDataIn0[7:0]							
0x1A	APDataIn1	R	APDataIn1[7:0]							
0x1B	APDataIn2	R	APDataIn2[7:0]							
0x1C	APDataIn3	R	APDataIn3[7:0]							
0x1D	APDataIn4	R	APDataIn4[7:0]							
0x1E	APDataIn5	R	APDataIn5[7:0]							
0x20	LDODirect	RW	—	—	—	—	—	—	LDO2DirEn	LDO1DirEn
0x21	MPCDirectWrite	RW	—	—	—	MPC4Write	MPC3Write	MPC2Write	MPC1Write	MPC0Write

Direct Access I2C Register Map (continued)

REGISTER ADDRESS	REGISTER NAME	RW	B7	B6	B5	B4	B3	B2	B1	B0
0x22	MPCDirectRead	R	—	—	—	MPC4Read	MPC3Read	MPC2Read	MPC1Read	MPC0Read
0x28	HptRAMAddr	RW	HptRAMAddr[7:0]							
0x29	HptRAMDataH	RW	nLSx[1:0]	AmpSign		Amp[6:2]				
0x2A	HptRAMDataM	RW	Amp[1:0]		Dur[4:0]		Wait[4]			
0x2B	HptRAMDataL	RW	Wait[3:0]							
0x2C	LEDStepDirect	RW	LED2Open	LED1Open	LED0Open	—	—	—	—	LEDIStep[1:0]
0x2D	LED0Direct	RW	LED0En[2:0]							
0x2E	LED1Direct	RW	LED1En[2:0]							
0x2F	LED2Direct	RW	LED2En[2:0]							
0x30	HptDirect0	RW	—	—	—	—	—	HptOffImp	HptThmProtDis	HptOCProtDis
0x31	HptDirect1	RW	HptExtTrig	HptRamEn	HptDrvEn	HptDrvMode[4:0]				
0x32	HptRTI2CAmp	RW	HptRTI2CAmp [6:0]							
0x33	HptPatRAMAddr	RW	HptPatRAMAddr[7:0]							

## Direct Access I<sup>2</sup>C Register Descriptions

### Table 4. HardwareID Register (0x00)

ADDRESS:	0x00							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	HardwareID[7:0]							
HardwareID [7:0]	HardwareID[7:0] bits show information about the hardware revision of the MAX20303							

### Table 5. FirmwareID Register (0x01)

ADDRESS:	0x01							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	FirmwareID[7:0]							
FirmwareID [7:0]	FirmwareID[7:0] bits show information about the firmware revision of the MAX20303							

## Interrupt Registers

### Table 6. Int0 Register (0x03)

ADDRESS:	0x03							
MODE:	Clear On Read							
BIT	7	6	5	4	3	2	1	0
NAME	ThmStatInt	ChgStatInt	ILimInt	UsbOVPInt	UsbOkInt	ChgThmSDInt	ThmRegInt	ChgTmolnt
ThmStatInt	Change in ThmStat caused interrupt.							
ChgStatInt	Change in ChgStat caused interrupt, or first detection complete after POR.							
ILimInt	Input current limit caused interrupt.							
UsbOVPInt	Change in USBOVP caused interrupt.							
UsbOkInt	Change in USBOK caused interrupt. Note: Registers written using opcodes 0x10, 0x14, 0x16, 0x18, 0x1A, and 0x1C are reset on charger insertion. After receiving a UsbOk interrupt, wait 10ms before writing any data using these opcodes. Failure to wait 10ms may result in the data being overwritten to the default.							
ChgThmSDInt	Change in ChgThmSD caused interrupt.							
ThmRegInt	Change in ChgThmReg caused interrupt.							
ChgTmolnt	Change in ChgTmolnt caused interrupt.							

### Table 7. Int1 Register (0x04)

ADDRESS:	0x04							
MODE:	Clear On Read							
BIT	7	6	5	4	3	2	1	0
NAME	ThmSDInt	BstFltInt	ThmBuck2Int	ThmBuck1Int	UVLLODO2Int	UVLLODO1Int	ThmLDO2Int	ThmLDO1Int
ThmSDInt	Change in ThmSD caused interrupt.							
BstFltInt	Change in BstFlt caused interrupt.							
ThmBuck2Int	Change in ThmBuck2 caused interrupt.							
ThmBuck1Int	Change in ThmBuck1 caused interrupt.							
UVLLODO2Int	Change in UVLLODO2 caused interrupt.							
UVLLODO1Int	Change in UVLLODO1 caused interrupt.							
ThmLDO2Int	Change in ThmLDO2 caused interrupt.							
ThmLDO1Int	Change in ThmLDO1 caused interrupt.							

**Table 8. Int2 Register (0x05)**

ADDRESS:	0x05							
MODE:	Clear On Read							
BIT	7	6	5	4	3	2	1	0
NAME	APCmdResplnt	SysErrInt	—	LRALockInt	LRAActInt	BBstThmInt	SysBatLimInt	ChgSysLimInt
APCmdResplnt	AP Command Response Interrupt 0 = No new data available in APDataIn registers. 1 = New data available in APDataIn registers.							
SysErrInt	System Error Interrupt 0 = No new error 1 = New Asynchronous System Error							
LRALockInt	LRA Lock Interrupt Change in LRALock caused interrupt.							
LRAActInt	Change in LRAAct caused interrupt.							
BBstThmInt	Change in BBstThm caused interrupt.							
SysBatLimInt	Change in SysBatLim caused interrupt.							
ChgSysLimInt	Change in ChgSysLim caused interrupt.							

**Status Registers****Table 9. Status0 Register (0x06)**

ADDRESS:	0x06							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	ThmStat[2:0]			ChgStat[2:0]		
ThmStat[2:0]	Status of Thermistor Monitoring 000 = T < T1 001 = T1 < T < T2 010 = T2 < T < T3 011 = T3 < T < T4 100 = T > T4 101 = No thermistor detected/THM high due to external pull-up 110 = NTC input disabled via ThmEn 111 = Automatic monitoring disabled because CHGIN is not present. THM can still be measured by ADC_Measure_Launch							
ChgStat[2:0]	Status of Charger Mode 000 = Charger off 001 = Charging suspended due to temperature (see battery charger state diagram) 010 = Pre-charge in progress 011 = Fast-charge constant current mode in progress 100 = Fast-charge constant voltage mode in progress 101 = Maintain charge in progress 110 = Maintain charger timer done 111 = Charger fault condition (see battery charger state diagram)							

**Table 10. Status1 Register (0x07)**

ADDRESS:	0x07							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	ILim	UsbOVP	UsbOk	ChgJEITA SD	ChgJEITA Reg	ChgTmo
ILim	CHGIN Input Current Limit 0 = CHGIN input current below limit 1 = CHGIN input current limit active							
UsbOVP	Status of CHGIN OVP 0 = CHGIN overvoltage not detected 1 = CHGIN overvoltage detected							
UsbOk	Status of CHGIN Input 0 = CHGIN Input not present or outside of valid range 1 = CHGIN Input present and valid							
ChgJEITASD	Status of Thermal Shutdown 0 = Charger in normal operating mode 1 = Charger is in thermal shutdown							
ChgJEITAREg	Status of Thermal Regulation 0 = Charger is functioning normally, or disabled 1 = Charger is running in thermal regulation mode and charging current is being actively reduced according to JEITA settings							
ChgTmo	Status of Time-Out Condition 0 = Charger is running normally, or disabled 1 = Charger has reached a time-out condition							



**Table 11. Status2 Register (0x08)**

ADDRESS:	0x08							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	ThmSD	BstFit	ThmBuck2	ThmBuck1	UVLOLD O2	UVLOLDO1	ThmLDO2	ThmLDO1
ThmSD	0 = Device operating normally 1 = Device in thermal shutdown							
BstFit	0 = HV Boost operating normally 1 = HV Boost in fault mode due to overcurrent or thermal shutdown							
ThmBuck2	0 = Buck2 operating normally 1 = Buck2 in thermal shutdown							
ThmBuck1	0 = Buck1 operating normally 1 = Buck1 in thermal shutdown							
UVLOLDO2	0 = LDO2 operating normally 1 = LDO2 UVLO active							
UVLOLDO1	0 = LDO1 operating normally 1 = LDO1 UVLO active							
ThmLDO2	0 = LDO2 operating normally 1 = LDO2 in thermal shutdown							
ThmLDO1	0 = LDO1 operating normally 1 = LDO1 in thermal shutdown							

**Table 12. Status3 Register (0x09)**

ADDRESS:	0x09							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	APCmdResp	SysErr	—	LRALock	LRAAct	BBstThm	SysBatLim	ChgSysLim
APCmdResp	AP Command Response Ready 0 = APResponse register is empty 1 = APResponse register contains an opcode							
SysErr	System Error Detect 0 = No system error 1 = System error detected. See SystemError (register 0x0B)							
LRALock	0 = Haptic driver is not active or has not yet locked onto LRA resonant frequency 1 = Haptic driver has locked onto LRA resonant frequency							
LRAAct	0 = LRA driver not active 1 = LRA driver active							
BBstThm	0 = Buck-boost converter operating normally 1 = Buck-boost converter in thermal shutdown							
SysBatLim	0 = Charge current is not being actively reduced to regulate SYS 1 = Charge current actively being reduced to regulate SYS collapse							
ChgSysLim	0 = Input current limit normal 1 = Input current limit being reduced to regulate CHGIN collapse							

**Table 13. SystemError Register (0x0B)**

ADDRESS:	0x0B							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	SystemError[7:0]							
SystemError[7:0]	<p>Last System Error Code:</p> <p>0x00 - MA_SYSError_NONE: No System Error</p> <p>0x01 - MA_SYSError_BOOT:</p> <p>0x02 - MA_SYSError_BOOT_WDT: Restart due to a watchdog event</p> <p>0x03 - MA_SYSError_BOOT_SWRSTREQ: Restart after Hard-Reset procedure</p> <p>0x04 - MA_SYSError_HPT_TIMEOUT: Haptic driver disabled after timeout set through HptDrvTmo[5:0] has expired</p> <p>0x10 - MA_SYSError_APCMD_INPROGRESS: Attempt to use an AP command before previous command completed</p> <p>0x11 - MA_SYSError_APCMD_WRITEPROTECT: Attempt to use a write protected command or invalid password</p> <p>0x12 - MA_SYSError_APCMD_UNKNOWN: Attempt to use an undefined command</p> <p>0x13 - MA_SYSError_APCMD_FAIL: AP command failed to execute</p> <p>0x20 - MA_SYSError_HPT_DRP_LOW: Haptic driver disabled due to overcurrent condition on the DRP low-side switch</p> <p>0x21 - MA_SYSError_HPT_DRP_HIG: Haptic driver disabled due to overcurrent condition on the DRP high-side switch</p> <p>0x22 - MA_SYSError_HPT_DRN_LOW: Haptic driver disabled due to overcurrent condition on the DRN low-side switch</p> <p>0x23 - MA_SYSError_HPT_DRN_HIG: Haptic driver disabled due to overcurrent condition on the DRN high-side switch</p> <p>0x24 - MA_SYSError_HPT_THM_ERR: Haptic driver disabled due to thermal shutdown</p> <p>0x25 - MA_SYSError_HPT_SYS_THR_HIT: Haptic driver disabled due to SYS falling below HptSysUVLO[7:0] threshold</p>							

## Interrupt Mask Registers

**Table 14. IntMask0 Register (0x0C)**

ADDRESS:	0x0C							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	ThmStat IntM	ChgStat IntM	ILimIntM	UsbOVP IntM	UsbOk IntM	ChgJEITASD IntM	ThmJEITA RegIntM	ChgTmo IntM
ThmStatIntM	ThmStatIntM masks the ThmStatInt interrupt in the Int0 register (0x03). 0 = Masked 1 = Not masked							
ChgStatIntM	ChgStatIntM masks the ChgStatInt interrupt in the Int0 register (0x03). 0 = Masked 1 = Not masked							
ILimIntM	ILimIntM masks the ILimInt interrupt in the Int0 register (0x03). 0 = Masked 1 = Not masked							
UsbOVPIntM	UsbOVPIntM masks the UsbOVPInt interrupt in the Int0 register (0x03). 0 = Masked 1 = Not masked							
UsbOkIntM	UsbOkIntM masks the UsbOkInt interrupt in the Int0 register (0x03). 0 = Masked 1 = Not masked							
ChgJEITASDIntM	ChgThmSDIntM masks the ChgThmSDInt interrupt in the Int0 register (0x03). 0 = Masked 1 = Not masked							
ChgJEITARegIntM	ThmRegIntM masks the ThmRegInt interrupt in the Int0 register (0x03). 0 = Masked 1 = Not masked							
ChgTmoIntM	ChgTmoIntM masks the ChgTmoInt interrupt in the Int0 register (0x03). 0 = Masked 1 = Not masked							

**Table 15. IntMask1 Register (0x0D)**

ADDRESS:	0x0D							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	ThmSd IntM	BstFitIntM	ThmBuck 2IntM	ThmBuck 1IntM	UVLOLDO 2IntM	UVLOLDO 1IntM	ThmLDO 2IntM	ThmLDO 1IntM
ThmSdIntM	ThmSdIntM masks the ThmSdInt interrupt in the Int1 register (0x04). 0 = Masked 1 = Not masked							
BstFitIntM	BstFitIntM masks the BstFitInt interrupt in the Int1 register (0x04). 0 = Masked 1 = Not masked							
ThmBuck2IntM	ThmBuck2IntM masks the ThmBuck2Int interrupt in the Int1 register (0x04). 0 = Masked 1 = Not masked							
ThmBuck1IntM	Masks the ThmBuck1Int interrupt in the Int1 register (0x04). 0 = Masked 1 = Not masked							
UVLOLDO2IntM	Masks the UVLOLDO2Int interrupt in the Int1 register (0x04). 0 = Masked 1 = Not masked							
UVLOLDO1IntM	Masks the UVLOLDO1Int interrupt in the Int1 register (0x04). 0 = Masked 1 = Not masked							
ThmLDO2IntM	Masks the ThmLDO2Int interrupt in the Int1 register (0x04). 0 = Masked 1 = Not masked							
ThmLDO1IntM	Masks the ThmLDO1Int interrupt in the Int1 register (0x04). 0 = Masked 1 = Not masked							

**Table 16. IntMask2 Register (0x0E)**

ADDRESS:	0x0E							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	APCmd RespIntM	SysErr IntM	—	LRALock IntM	LRAAct IntM	BBstThm IntM	SysBatLim IntM	ChgSys LimIntM
APCmdRespIntM	Masks the APCmdRespInt interrupt in the Int2 register (0x05). 0 = Masked 1 = Not masked							
SysErrIntM	Masks the SysErrInt interrupt in the Int2 register (0x05). 0 = Masked 1 = Not masked							
LRALockIntM	Masks the LRALockInt interrupt in the Int2 register (0x05). 0 = Masked 1 = Not masked							
LRAActIntM	Masks the LRAActInt interrupt in the Int2 register (0x05). 0 = Masked 1 = Not masked							
BBstThmIntM	Masks the BBstThmInt interrupt in the Int2 register (0x05). 0 = Masked 1 = Not masked							
SysBatLimIntM	Masks the SysBatLimInt interrupt in the Int2 register (0x05). 0 = Masked 1 = Not masked							
ChgSysLimIntM	Masks the ChgSysLimInt interrupt in the Int2 register (0x05). 0 = Masked 1 = Not masked							

**AP Interface Registers****Table 17. APDataOut0 Register (0x0F)**

ADDRESS:	0x0F							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	APDataOut0[7:0]							
APDataOut0[7:0]	Data register 0 for AP write commands.							

**Table 18. APDataOut1 Register (0x10)**

ADDRESS:	0x10							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	APDataOut1[7:0]							
APDataOut1[7:0]	Data register 1 for AP write commands.							

**Table 19. APDataOut2 Register (0x11)**

ADDRESS:	0x11							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	APDataOut2[7:0]							
APDataOut2[7:0]	Data register 2 for AP write commands.							

**Table 20. APDataOut3 Register (0x12)**

ADDRESS:	0x12							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	APDataOut3[7:0]							
APDataOut3[7:0]	Data register 3 for AP write commands.							

**Table 21. APDataOut4 Register (0x13)**

ADDRESS:	0x13							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	APDataOut4[7:0]							
APDataOut4[7:0]	Data register 4 for AP write commands.							

**Table 22. APDataOut5 Register (0x14)**

ADDRESS:	0x14							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	APDataOut5[7:0]							
APDataOut5[7:0]	Data register 5 for AP write commands.							

**Table 23. APDataOut6 Register (0x15)**

ADDRESS:	0x15							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	APDataOut6[7:0]							
APDataOut6[7:0]	Data register 6 for AP write commands.							

**Table 24. APCmdOut Register (0x17)**

ADDRESS:	0x17							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	APCmdOut[7:0]							
APCmdOut[7:0]	Opcode command register							

**Table 25. APResponse Register (0x18)**

ADDRESS:	0x18							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	APResponse [7:0]							
APResponse[7:0]	AP command response register							

**Table 26. APDataIn0 Register (0x19)**

ADDRESS:	0x19							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	APDataIn0[7:0]							
APDataIn0[7:0]	Data register 0 for AP read commands.							

**Table 27. APDataIn1 Register (0x1A)**

ADDRESS:	0x1A							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	APDataIn1[7:0]							
APDataIn1[7:0]	Data register 1 for AP read commands.							

**Table 28. APDataIn2 Register (0x1B)**

ADDRESS:	0x1B							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	APDataIn2[7:0]							
APDataIn2[7:0]	Data register 2 for AP read commands.							

**Table 29. APDataIn3 Register (0x1C)**

ADDRESS:	0x1C							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	APDataIn3[7:0]							
APDataIn3[7:0]	Data register 3 for AP read commands.							

**Table 30. APDataIn4 Register (0x1D)**

ADDRESS:	0x1D							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	APDataOut4[7:0]							
APDataOut4[7:0]	Data register 4 for AP write commands.							

**Table 31. APDataIn5 Register (0x1E)**

ADDRESS:	0x1E							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	APDataIn5[7:0]							
APDataIn5[7:0]	Data register 5 for AP read commands.							

**LDO Direct Register****Table 32. LDODirect Register (0x20)**

ADDRESS:	0x20							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	—	—	—	LDO2Dir En	LDO1Dir En
LDO2DirEn	LDO2 Direct Enable. Valid only if LDO2En = 11 0 = LDO2 Off 1 = LDO2 On							
LDO1DirEn	LDO1 Direct Enable Valid only if LDO1En = 11 0 = LDO1 Off 1 = LDO1 On							



**MPC Direct Registers****Table 33. MPCDirectWrite Register (0x21)**

ADDRESS:	0x21							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	MPC4Write	MPC3Write	MPC2Write	MPC1Write	MPC0Write
MPC4Write	MPC4 Direct Write (returns 0 if MPC is configured as output (GPIO_HiZB = 1)) 0 = set MPC4 low 1 = set MPC4 high							
MPC3Write	MPC3 Direct Write (returns 0 if MPC is configured as output (GPIO_HiZB = 1)) 0 = set MPC3 low 1 = set MPC3 high							
MPC2Write	MPC2 Direct Write (returns 0 if MPC is configured as output (GPIO_HiZB = 1)) 0 = set MPC2 low 1 = set MPC2 high							
MPC1Write	MPC1 Direct Write (returns 0 if MPC is configured as output (GPIO_HiZB = 1)) 0 = set MPC1 low 1 = set MPC1 high							
MPC0Write	MPC0 Direct Write (returns 0 if MPC is configured as output (GPIO_HiZB = 1)) 0 = set MPC0 low 1 = set MPC0 high							

**Table 34. MPCDirectRead Register (0x22)**

ADDRESS:	0x22							
MODE:	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	MPC4Read	MPC3Read	MPC2Read	MPC1Read	MPC0Read
MPC4Read	MPC4 Direct Readback 0 = MPC4 is low 1 = MPC4 is high							
MPC3Read	MPC3 Direct Readback 0 = MPC3 is low 1 = MPC3 is high							
MPC2Read	MPC2 Direct Readback 0 = MPC2 is low 1 = MPC2 is high							
MPC1Read	MPC1 Direct Readback 0 = MPC1 is low 1 = MPC1 is high							
MPC0Read	MPC0 Direct Readback 0 = MPC0 is low 1 = MPC0 is high							

**Haptic RAM Registers**

**Table 35. HptRAMAddr Register (0x28)**

ADDRESS:	0x28							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	HptRAMAdd[7:0]							
HptRAMAdd[7:0]	RAM address to which haptic pattern data in registers 0x29, 0x2A, 0x2B will be written.							

**Table 36. HptRAMDataH Register (0x29)**

ADDRESS:	0x29							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	nLSx[1:0]		AmpSign	Amp[6:2]				

**Table 37. HptRAMDataM Register (0x2A)**

ADDRESS:	0x2A							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	Amp[1:0]		Dur[4:0]				Wait[4]	

**Table 38. HptRAMDataL Register (0x2B)**

ADDRESS:	0x2B							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	Wait[3:0]				Rpt[3:0]			

## LED Direct Registers

Table 39. LEDStepDirect Register (0x2C)

ADDRESS:	0x2C							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	LED2Open	LED1Open	LED0Open	—	—	—	LEDIStep[1:0]	
LED2Open	LED2 Open detection (Read only) 0 = $V_{LED2} > V_{LED\_DET}$ 1 = $V_{LED2} \leq V_{LED\_DET}$ or LED2 disabled							
LED1Open	LED1 Open detection (Read only) 0 = $V_{LED1} > V_{LED\_DET}$ 1 = $V_{LED1} \leq V_{LED\_DET}$ or LED1 disabled							
LED0Open	LED0 Open detection (Read only) 0 = $V_{LED0} > V_{LED\_DET}$ 1 = $V_{LED0} \leq V_{LED\_DET}$ or LED0 disabled							
LEDIStep[1:0]	LED Direct Current Step Register 00 = 0.6mA 01 = 1.0mA 10 = 1.2mA 11 = RESERVED							

Table 40. LED0Direct Register (0x2D)

ADDRESS:	0x2D							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	LED0En[2:0]				LED0ISet[4:0]			
LED0En[2:0]	LED0 Driver Enable 000 = Off 001 = LED0 On 010 = Controlled by internal charger status signal 011 = Controlled by MPC0 100 = Controlled by MPC1 101 = Controlled by MPC2 110 = Controlled by MPC3 111 = Controlled by MPC4							
LED0ISet[4:0]	LED0 Direct Step Count LED0 current in mA is given by $(LED0ISet[4:0] + 1) \times LEDIStep[1:0]$ 0x00 = 0.6mA/1.0mA/1.2mA 0x01 = 1.2mA/2.0mA/2.4mA ... 0x18 = 15mA/25mA/30mA							

**Table 41. LED1Direct Register (0x2E)**

ADDRESS:	0x2E							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	LED1En[2:0]				LED1ISet[4:0]			
LED1En[2:0]	<p>LED1 Driver Enable</p> <p>000 = Off</p> <p>001 = LED1 On</p> <p>010 = Controlled by internal charger status signal</p> <p>011 = Controlled by MPC0</p> <p>100 = Controlled by MPC1</p> <p>101 = Controlled by MPC2</p> <p>110 = Controlled by MPC3</p> <p>111 = Controlled by MPC4</p>							
LED1ISet[4:0]	<p>LED1 Direct Step Count</p> <p>LED1 current in mA is given by <math>(LED1ISet[4:0] + 1) \times LED1Step[1:0]</math></p> <p>0x00 = 0.6mA/1.0mA/1.2mA</p> <p>0x01 = 1.2mA/2.0mA/2.4mA</p> <p>...</p> <p>0x18 = 15mA/25mA/30mA</p>							

**Table 42. LED2Direct Register (0x2F)**

ADDRESS:	0x2F							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	LED2En[2:0]				LED2ISet[4:0]			
LED2En[2:0]	<p>LED2 Driver Enable</p> <p>000 = Off</p> <p>001 = LED2 On</p> <p>010 = Controlled by internal charger status signal</p> <p>011 = Controlled by MPC0</p> <p>100 = Controlled by MPC1</p> <p>101 = Controlled by MPC2</p> <p>110 = Controlled by MPC3</p> <p>111 = Controlled by MPC4</p>							
LED2ISet[4:0]	<p>LED2 Direct Step Count</p> <p>LED2 current in mA is given by <math>(LED2ISet[4:0] + 1) \times LED2Step[1:0]</math></p> <p>0x00 = 0.6mA/1.0mA/1.2mA</p> <p>0x01 = 1.2mA/2.0mA/2.4mA</p> <p>...</p> <p>0x18 = 15mA/25mA/30mA</p>							

## Haptic Direct Registers

**Table 43. HptDirect0 Register (0x30)**

ADDRESS:	0x30							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	—	—	HptOffImp	HptThmProt Dis	HptOCPr otDis
HptOffImp	<p>Haptic Driver Output Off State Impedance</p> <p>0 = When haptic driver is disabled, outputs are strongly shorted to GND through low-side driver FETs.</p> <p>1 = When haptic driver is disabled, outputs are shorted to GND with 15kΩ pull-down.</p>							
HptThmProtDis	<p>Haptic Driver Thermal Protection Disable</p> <p>If HptThmProtDis = 0 and the haptic driver shuts down due to an over temperature condition, SystemError[7:0] = 0x24 is issued and HptLock = 1. See Opcode 0xA8 for restarting the haptic driver</p> <p>0 = Thermal protection enabled. Haptic driver will shut down if <math>T_J \geq 150^\circ\text{C}</math> (typ)</p> <p>1 = Thermal protection disabled.</p>							
HptOCProtDis	<p>Haptic Driver Overcurrent Protection Disable</p> <p>If HptOCProtDis = 0 and the haptic driver shuts down due to an overcurrent condition, SystemError[7:0] will equal to one of four codes (0x20-0x23) is issued and HptLock = 1. See Opcode 0xA8 for restarting the haptic driver</p> <p>0 = Overcurrent protection enabled. Haptic driver will shut down if current exceeds 1A (typ)</p> <p>1 = Overcurrent protection disabled.</p>							

**Table 44. HptDirect1 Register (0x31)**

ADDRESS:	0x31							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	HptExtTrig	HptRamEn	HptDrvEn	HptDrvMode[4:0]				
HptExtTrig	Haptic driver external trigger pattern for ETRG and RAMHPI driver mode (HptDrvMode = 01100, 10010, respectively). 0 = No pattern triggered. 1 = Vibration triggered							
HptRamEn	Haptic RAM Block Enable 0 = RAM disabled. 1 = RAM enabled.							
HptDrvEn	Haptic Driver Enable In all modes, the haptic driver must be enabled at the same time or before providing the desired mode in HptDrvMod[4:0]. The HptDrvEn bit must remain set during the vibration. Once vibration finishes, HptDrvMod[4:0] must be set to "00000" before the haptic driver may be disabled via HptDrvEn = 0 for power savings. 0 = Haptic driver block disabled. 1 = Haptic driver block enabled.							
HptDrvMode [4:0]	Haptic Driver Mode Selection 00000 = Disable haptic driver 00001 = Enable PPWM0 mode and provide amplitude based on PWM duty cycle on MPC0 00010 = Enable PPWM1 mode and provide amplitude based on PWM duty cycle on MPC1 00011 = Enable PPWM2 mode and provide amplitude based on PWM duty cycle on MPC2 00100 = Enable PPWM3 mode and provide amplitude based on PWM duty cycle on MPC3 00101 = Enable PPWM4 mode and provide amplitude based on PWM duty cycle on MPC4 00110 = Enable RTI2C mode and provide current output amplitude based on the contents of HptRTI2CAmp(0x32) 00111 = Enable ETRG0 mode. Provide a pulse on MPC0 to start vibration (See "ETRG Mode" section for details) 01000 = Enable ETRG1 mode. Provide a pulse on MPC1 to start vibration (See "ETRG Mode" section for details) 01001 = Enable ETRG2 mode. Provide a pulse on MPC2 to start vibration (See "ETRG Mode" section for details) 01010 = Enable ETRG3 mode. Provide a pulse on MPC3 to start vibration (See "ETRG Mode" section for details) 01011 = Enable ETRG4 mode. Provide a pulse on MPC4 to start vibration (See "ETRG Mode" section for details) 01100 = Enable ETRGI mode via I2C. Set HptExtTrg(0x31[7]) bit to start vibration (See "ETRG Mode" section for details) 01101 = Enable RAMHP0 mode. Provide a pulse on MPC0 to start vibration (See "RAMHP Mode" section for details) 01110 = Enable RAMHP1 mode. Provide a pulse on MPC1 to start vibration (See "RAMHP Mode" section for details) 01111 = Enable RAMHP2 mode. Provide a pulse on MPC2 to start vibration (See "RAMHP Mode" section for details) 10000 = Enable RAMHP3 mode. Provide a pulse on MPC3 to start vibration (See "RAMHP Mode" section for details) 10001 = Enable RAMHP4 mode. Provide a pulse on MPC4 to start vibration (See "RAMHP Mode" section for details) 10010 = Enable RAMHPI mode via I2C. Set HptExtTrg(0x31[7]) bit to start vibration (See "RAMHP Mode" section for details)							

**Table 45. HptRTI2CAmp Register (0x32)**

ADDRESS:	0x32							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	HptRTI2C Sign	HptRTI2CAmp[6:0]						
HptRTI2CSign	Sign of haptic pattern amplitude in RTI2C mode (HptDrvMode = 00110)							
HptRTI2CAmp [6:0]	Amplitude of haptic pattern in RTI2C mode (HptDrvMode = 00110). LSB = $V_{SYS}/128$							

**Table 46. HptPatRAMAddr Register (0x33)**

ADDRESS:	0x33							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	HptPatRAMAddr[7:0]							
HptPatRAMAddr [7:0]	Address of first sample in vibration pattern to be run in RAMHP_ mode (HptDrvMode = 01101, 01111, 10000, 10001, 10010)							

## AP Command Register Descriptions

### GPIO Config Commands

**Table 47. 0x01 – GPIO\_Config\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x01)	0	0	0	0	0	0	0	1
APDataOut0	—	—	—	GPIO0Cmd	GPIO0OD	GPIO0HiZB	GPIO0Res	GPIO0Pup
APDataOut1	—	—	—	GPIO1Cmd	GPIO1OD	GPIO1HiZB	GPIO1Res	GPIO1Pup
APDataOut2	—	—	—	GPIO2Cmd	GPIO2OD	GPIO2HiZB	GPIO2Res	GPIO2Pup
APDataOut3	—	—	—	GPIO3Cmd	GPIO3OD	GPIO3HiZB	GPIO3Res	GPIO3Pup
APDataOut4	—	—	—	GPIO4Cmd	GPIO4OD	GPIO4HiZB	GPIO4Res	GPIO4Pup
<b>GPIO_Cmd</b>	GPIO Output Control Valid only if GPIO_ is configured as output (GPIO_HiZB = 1) 0 = MPC_ output controlled by AP command 1 = MPC_ output controlled by I <sup>2</sup> C direct register							
<b>GPIO_OD</b>	GPIO Output Configuration Valid only if GPIO_ is configured as output (GPIO_HiZB = 1) 0 = MPC_ is push-pull connected to BK2OUT 1 = MPC_ is open drain							
<b>GPIO_HiZB</b>	GPIO Direction 0 = MPC_ is Hi-Z. Input buffer enabled 1 = MPC_ is not Hi-Z. Output buffer enabled							
<b>GPIO_Res</b>	GPIO Resistor Presence Valid only if GPIO_ is configured as input (GPIO_HiZB = 0) 0 = Resistor not connected to MPC_ 1 = Resistor connected to MPC_							
<b>GPIO_Pup</b>	GPIO Resistor Configuration Valid only if there is a resistor on GPIO_ (GPIO_Res = 1) 0 = Pulldown connected to MPC_ 1 = Pullup to V <sub>CCINT</sub> connected MCP_							



**Table 48. GPIO\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x01)	0	0	0	0	0	0	0	1

**Table 49. 0x02 – GPIO\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x02)	0	0	0	0	0	0	1	0

**Table 50. GPIO\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x02)	0	0	0	0	0	0	1	0
APDataIn0	—	—	—	GPIO0Cmd	GPIO0OD	GPIO0HiZB	GPIO0Res	GPIO0Pup
APDataIn1	—	—	—	GPIO1Cmd	GPIO1OD	GPIO1HiZB	GPIO1Res	GPIO1Pup
APDataIn2	—	—	—	GPIO2Cmd	GPIO2OD	GPIO2HiZB	GPIO2Res	GPIO2Pup
APDataIn3	—	—	—	GPIO3Cmd	GPIO3OD	GPIO3HiZB	GPIO3Res	GPIO3Pup
APDataIn4	—	—	—	GPIO4Cmd	GPIO4OD	GPIO4HiZB	GPIO4Res	GPIO4Pup

**Table 51. 0x03 – GPIO\_Control\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x03)	0	0	0	0	0	0	1	1
APDataOut0	—	—	—	GPIO4Out	GPIO3Out	GPIO2Out	GPIO1Out	GPIO0Out
GPIO_Out	Valid only if GPIO_ is configured as output driven by AP Command (GPIO_Cmd = 0) 0 = Set GPIO_ LOW 1 = Set GPIO_ HIGH (if GPIO_OD = 0)/Hi-Z (if GPIO_OD = 1)							

Table 52. GPIO\_Control\_Write Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x03)	0	0	0	0	0	0	1	1

Table 53. 0x04 – GPIO\_Control\_Read

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x04)	0	0	0	0	0	1	0	0

Table 54. GPIO\_Control\_Read Response

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x04)	0	0	0	0	0	1	0	0
APDataIn0	—	—	—	GPIO4Out	GPIO3Out	GPIO2Out	GPIO1Out	GPIO0Out
APDataIn1	—	—	—	GPIO4Stat	GPIO3Stat	GPIO2Stat	GPIO1Stat	GPIO0Stat
GPIO_Stat	GPIO State 0 = GPIO_LOW 1 = GPIO_HIGH (if GPIO_Od = 0) / Hi-Z (if GPIO_Od = 1)							

Table 55. 0x06 – MPC\_Config\_Write

MODE	Write								
BIT	B7	B6	B5	B4	B3	B2	B1	B0	
APCmdOut (0x06)	0	0	0	0	0	1	1	0	
APDataOut0	MPC0	BBstMPC En	SFOUTM PCEn	CPMP CEn	LDO2MP CEn	LDO1MP CEn	Buck2MP CEn	Buck1MP CEn	BstMP CEn
APDataOut1	MPC1	BBstMPC En	SFOUTM PCEn	CPMP CEn	LDO2MP CEn	LDO1MP CEn	Buck2MP CEn	Buck1MP CEn	BstMP CEn
APDataOut2	MPC2	BBstMPC En	SFOUTM PCEn	CPMP CEn	LDO2MP CEn	LDO1MP CEn	Buck2MP CEn	Buck1MP CEn	BstMP CEn
APDataOut3	MPC3	BBstMPC En	SFOUTM PCEn	CPMP CEn	LDO2MP CEn	LDO1MP CEn	Buck2MP CEn	Buck1MP CEn	BstMP CEn
APDataOut4	MPC4	BBstMPC En	SFOUTM PCEn	CPMP CEn	LDO2MP CEn	LDO1MP CEn	Buck2MP CEn	Buck1MP CEn	BstMP CEn

Shaded fields are defaulted to 1 if the corresponding resources contain the following OTP setting:  
 XXXSeq = 111 (controlled by BstEn after 100% of Boot/POR Process Delay Control)  
 XXXEn = 10 (MPC registers control)

**Table 55. 0x06 – MPC\_Config\_Write**

BBstMPCEn	Buck-Boost Enable Configuration Effective only when BBstSeq = 111 and BBstEn = 10 0 = MPC_ has no effect on Buck-boost 1 = Buck-boost enabled when MPC_ is high
SFOUTMPCEn	SFOUT LDO Enable Configuration Effective only when SFOUTEn = 10 0 = MPC_ has no effect on SFOUT LDO 1 = SFOUT LDO enabled when CHGIN is present and MPC_ is high
CPMPCEn	Charge Pump Enable Configuration Effective only when CPSeq = 111 and CPEn = 10 0 = MPC_ has no effect on Charge Pump 1 = Charge Pump enabled when MPC_ is high
LDO2MPCEn	LDO2 Enable Configuration Effective only when LDO2Seq = 111 and LDO2En = 10 0 = MPC_ has no effect on LDO2 1 = LDO2 enabled when MPC_ is high
LDO1MPCEn	LDO1 Enable Configuration Effective only when LDO1Seq = 111 and LDO1En = 10 0 = MPC_ has no effect on LDO1 1 = LDO1 enabled when MPC_ is high
Buck2MPCEn	Buck2 Enable Configuration Effective only when Buck2Seq = 111 and Buck2En = 10 0 = MPC_ has no effect on Buck2 1 = Buck2 enabled when MPC_ is high
Buck1MPCEn	Buck1 Enable Configuration Effective only when Buck1Seq = 111 and Buck1En = 10 0 = MPC_ has no effect on Buck1 1 = Buck1 enabled when MPC_ is high
BstMPCEn	Boost Enable Configuration Effective only when BstSeq = 111 and BstEn = 10 0 = MPC_ has no effect on Boost 1 = Boost enabled when MPC_ is high

**Table 56. MPC\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x06)	0	0	0	0	0	1	1	0

**Table 57. 0x07 – MPC\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x07)	0	0	0	0	0	1	1	1

**Table 58. MPC\_Config\_Read Response**

BIT		B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x07)		0	0	0	0	0	1	1	1
APDataIn0	MPC0	BBstMPC En	SFOUTM PCEn	CPMP CEn	LDO2MP CEn	LDO1MP CEn	Buck2MP CEn	Buck1MP CEn	BstMP CEn
APDataIn1	MPC1	BBstMPC En	SFOUTM PCEn	CPMP CEn	LDO2MP CEn	LDO1MP CEn	Buck2MP CEn	Buck1MP CEn	BstMP CEn
APDataIn2	MPC2	BBstMPC En	SFOUTM PCEn	CPMP CEn	LDO2MP CEn	LDO1MP CEn	Buck2MP CEn	Buck1MP CEn	BstMP CEn
APDataIn3	MPC3	BBstMPC En	SFOUTM PCEn	CPMP CEn	LDO2MP CEn	LDO1MP CEn	Buck2MP CEn	Buck1MP CEn	BstMP CEn
APDataIn4	MPC4	BBstMPC En	SFOUTM PCEn	CPMP CEn	LDO2MP CEn	LDO1MP CEn	Buck2MP CEn	Buck1MP CEn	BstMP CEn

### Input Current Limit Commands

Note: Registers written using opcodes 0x10, 0x14, 0x16, 0x18, 0x1A, and 0x1C are reset on charger insertion. After receiving a UsbOk interrupt, wait 10ms before writing any data using these opcodes. Failure to wait 10ms may result in the data being overwritten to the default.

**Table 59. 0x10 – InputCurrent\_Config\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x10)	0	0	0	1	0	0	0	0
APDataOut0	—	—	—	ILimBlank[1:0]		ILimCntl[2:0]		
ILimBlank [1:0]	CHGIN Current Limiter Blanking Time 00 = No debounce (allow a few clock cycles for resampling) 01 = 0.5ms 10 = 1ms 11 = 10ms							
ILimCntl[2:0]	CHGIN Programmable Input Current Limit (See EC table for details) 000 = 50mA 001 = 100mA 010 = 150mA 011 = 200mA 100 = 300mA 101 = 400mA 110 = 500mA 111 = 1000mA							

**Table 60. InputCurrent\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x10)	0	0	0	1	0	0	0	0

**Table 61. 0x11 – InputCurrent\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x11)	0	0	0	1	0	0	0	0

**Table 62. InputCurrent\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x11)	0	0	0	1	0	0	0	0
APDataIn0	—	—	—	ILimBlank[1:0]		ILimCntl[2:0]		

**Thermal Shutdown Configuration Commands****Table 63. 0x12 – ThermalShutdown\_Config\_Read**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x12)	0	0	0	1	0	0	1	0
APDataOut0	—	—	—	—	—	—	TShdnTmo[1:0]	
TShdnTmo [1:0]	Thermal Shutdown Retry Timeout Boot sequence only 00 = Latch-Off (See <i>Power State</i> diagrams (Figure 1a to Figure 1f) for restart procedure) 01 = 500ms 10 = 1s 11 = 5s							

**Table 64. ThermalShutdown\_Config\_Read Response**

	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x12)	0	0	0	1	0	0	1	0

## Charger Configuratioin Commands

Table 65. 0x14 – Charger\_Config\_Write

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x14)	0	0	0	1	0	1	0	0
APDataOut0	—	—	MtChgTmr[1:0]		FChgTmr[1:0]		PChgTmr[1:0]	
APDataOut1	—	VPChg[2:0]			IPChg[1:0]		ChgDone[1:0]	
APDataOut2	ChgAuto Stp	ChgAuto Re	BatReChg[1:0]		BatReg[3:0]			
APDataOut3	—	—	—	—	SysMinVlt[2:0]			
MtChgTmr[1:0]	Maintain Charge Timer Setting 00 = 0min 01 = 15min 10 = 30min 11 = 60min							
FChgTmr[1:0]	Fast Charge Timer Setting 00 = 75min 01 = 150min 10 = 300min 11 = 600min							
PChgTmr[1:0]	Pre-charge Timer Setting 00 = 30min 01 = 60min 10 = 120min 11 = 240min							
VPChg[2:0]	Precharge Voltage Threshold Setting 000 = 2.1V 001 = 2.25V 010 = 2.40V 011 = 2.55V 100 = 2.70V 101 = 2.85V 110 = 3.00V 111 = 3.15V							
IPChg[1:0]	Precharge Current Setting 00 = 0.05 x IFChg 01 = 0.1 x IFChg 10 = 0.2 x IFChg 11 = 0.3 x IFChg							

**Charger Configuratoin Commands (continued)****Table 65. 0x14 – Charger\_Config\_Write (continued)**

ChgDone[1:0]	Charge Done Threshold Setting 00 = 0.05 x IFChg 01 = 0.1 x IFChg 10 = 0.2 x IFChg 11 = 0.3 x IFChg
ChgAutoStp	Charger Auto-Stop Controls the transition from Maintain Charger to Maintain Charger Done. 0 = Auto-Stop disabled. 1 = Auto-Stop enabled.
ChgAutoRe	Charger Auto-Restart Control 0 = Charger remains in maintain charge done even when $V_{BAT}$ is less than charge restart threshold (see Charger state diagram) 1 = Charger automatically restarts when $V_{BAT}$ drops below charge restart threshold
BatReChg[1:0]	Recharge Threshold in Relation to BatReg[3:0] 00 = BatReg - 70mV 01 = BatReg - 120mV 10 = BatReg - 170mV 11 = BatReg - 220mV
BatReg[3:0]	Battery Regulation Voltage 0000 = 4.05V 0001 = 4.10V 0010 = 4.15V 0011 = 4.20V 0100 = 4.25V 0101 = 4.30V 0110 = 4.35V 0111 = 4.40V 1000 = 4.45V 1001 = 4.5V 1010 = 4.55V 1011 = 4.6V
SysMinVlt[2:0]	System Voltage Minimum Threshold 000 : 3.6V 001: 3.7V 010: 3.8V 011: 3.9V 100: 4.0V 101: 4.1V 110: 4.2V 111: 4.3V



**Table 66. Charger\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x14)	0	0	0	1	0	1	0	0

**Table 67. 0x15 – Charger\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x15)	0	0	0	1	0	1	0	1

**Table 68. Charger\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x15)	0	0	0	1	0	1	0	1
APDataIn0	—	—	MtChgTmr[1:0]		FChgTmr[1:0]		PChgTmr[1:0]	
APDataIn1	—	VPChg[2:0]			IPChg[1:0]		ChgDone[1:0]	
APDataIn2	ChgAuto Stp	ChgAuto Re	BatReChg[1:0]		BatReg[3:0]			
APDataIn3	—	—	—	—	SysMinVlt[2:0]			

**Table 69. 0x16 – ChargerThermalLimits\_Config\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x16)	0	0	0	1	0	1	1	0
APDataOut0	ColdLim[7:0]							
APDataOut1	CoolLim[7:0]							
APDataOut2	WarmLim[7:0]							
APDataOut3	HotLim[7:0]							
APDataOut4	Password[15:8]							
APDataOut5	Password[7:0]							
ColdLim[7:0]	Cold Zone Boundary Defines the falling threshold voltage on THM that defines the cold charging temperature zone. 8-bit value, 1.8V full-scale voltage.							
CoolLim[7:0]	Cool Zone Boundary Defines the falling threshold voltage on THM that defines the cool charging temperature zone. 8-bit value, 1.8V full-scale voltage.							
WarmLim[7:0]	Warm Zone Boundary Defines the rising threshold voltage on THM that defines the cool charging temperature zone. 8-bit value, 1.8V full-scale voltage.							
HotLim[7:0]	Hot Zone Boundary Defines the rising threshold voltage on THM that defines the hot charging temperature zone. 8-bit value, 1.8V full-scale voltage.							
Password[15:0]	Thermal Limit Configuration Password If Write-Protect enabled, ChargerThermalLimits can be configured using the following password: 0x1E7A. If Write-Protect enabled, incorrect password will result in SystemError[7:0] = 0x11.							

**Table 70. ChargerThermalLimits\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x16)	0	0	0	1	0	1	1	0

**Table 71. 0x17 – ChargerThermalLimits\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x17)	0	0	0	1	0	1	1	1

**Table 72. ChargerThermalLimits\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x17)	0	0	0	1	0	1	1	0
APDataIn0	ColdLim[7:0]							
APDataIn1	CoolLim[8:0]							
APDataIn2	WarmLim[7:0]							
APDataIn3	HotLim[7:0]							

**Table 73. 0x18 – ChargerThermalReg\_Config\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x18)	0	0	0	1	1	0	0	0
APDataOut0	ColdChgEn	—	—	ColdBatReg[1:0]		ColdFChg[2:0]		
APDataOut1	CoolChgEn	—	—	CoolBatReg[1:0]		CoolFChg[2:0]		
APDataOut2	—	—	—	RoomBatReg[1:0]		RoomFChg[2:0]		
APDataOut3	WarmChgEn	—	—	WarmBatReg[1:0]		WarmFChg[2:0]		
APDataOut4	HotChgEn	—	—	HotBatReg[1:0]		HotFChg[2:0]		
APDataOut5	Password[15:8]							
APDataOut6	Password[7:0]							
ColdChgEn	Cold Zone Charger Control Determines if charger is enabled for cold temperature zone. 0 = Charging disabled in cold temperature zone. 1 = Charging enabled in cold temperature zone.							
ColdBatReg [1:0]	Cold Zone Battery Regulation Voltage Sets modified BatReg[3:0] in the cold temperature zone. 00 = BatReg-150mV 01 = BatReg-100mV 10 = BatReg-50mV 11 = BatReg							
ColdFChg [2:0]	Cold Zone Fast Charge Current Scaling Sets modified fast charge in the cold temperature zone. 000 = 0.2 x IFChg 001 = 0.3 x IFChg 010 = 0.4 x IFChg 011 = 0.5 x IFChg 100 = 0.6 x IFChg 101 = 0.7 x IFChg 110 = 0.8 x IFChg 111 = 1.0 x IFChg							

**Table 73. 0x18 – ChargerThermalReg\_Config\_Write (continued)**

CoolChgEn	<p>Cool Zone Charger Control</p> <p>Determines if charger is enabled for cool temperature zone.</p> <p>0 = Charging disabled in cool temperature zone.</p> <p>1 = Charging enabled in cool temperature zone.</p>
CoolBatReg [1:0]	<p>Cool Zone Battery Regulation Voltage</p> <p>Sets modified BatReg[3:0] in the cool temperature zone.</p> <p>00 = BatReg-150mV</p> <p>01 = BatReg-100mV</p> <p>10 = BatReg-50mV</p> <p>11 = BatReg</p>
CoolFChg [2:0]	<p>Cool Zone Fast Charge Current Scaling</p> <p>Sets modified fast charge in the cool temperature zone.</p> <p>000 = 0.2 x IFChg</p> <p>001 = 0.3 x IFChg</p> <p>010 = 0.4 x IFChg</p> <p>011 = 0.5 x IFChg</p> <p>100 = 0.6 x IFChg</p> <p>101 = 0.7 x IFChg</p> <p>110 = 0.8 x IFChg</p> <p>111 = 1.0 x IFChg</p>
RoomBat Reg[4:3]	<p>Room Zone Battery Regulation Voltage</p> <p>Sets the modified BatReg[3:0] in the room temperature zone.</p> <p>00 = BatReg-150mV</p> <p>01 = BatReg-100mV</p> <p>10 = BatReg-50mV</p> <p>11 = BatReg</p>
RoomFChg [2:0]	<p>Room Zone Fast Charge Current Scaling</p> <p>Sets the modified fast charge in the room temperature zone.</p> <p>000 = 0.2 x IFChg</p> <p>001 = 0.3 x IFChg</p> <p>010 = 0.4 x IFChg</p> <p>011 = 0.5 x IFChg</p> <p>100 = 0.6 x IFChg</p> <p>101 = 0.7 x IFChg</p> <p>110 = 0.8 x IFChg</p> <p>111 = 1.0 x IFChg</p>
WarmChg En	<p>Warm Zone Charger Control</p> <p>Determines if charger is enabled for warm temperature zone.</p> <p>0 = Charging disabled in warm temperature zone.</p> <p>1 = Charging enabled in warm temperature zone.</p>

**Table 73. 0x18 – ChargerThermalReg\_Config\_Write (continued)**

WarmBatReg[1:0]	<p>Warm Zone Battery Regulation Voltage</p> <p>Sets the modified BatReg[3:0] in the warm temperature zone.</p> <p>00 = BatReg-150mV  01 = BatReg-100mV  10 = BatReg-50mV  11 = BatReg</p>
WarmFChg[2:0]	<p>Warm Zone Fast Charge Current Scaling</p> <p>Sets the modified fast charge in the warm temperature zone.</p> <p>000 = 0.2 x IFChg  001 = 0.3 x IFChg  010 = 0.4 x IFChg  011 = 0.5 x IFChg  100 = 0.6 x IFChg  101 = 0.7 x IFChg  110 = 0.8 x IFChg  111 = 1.0 x IFChg</p>
HotChgEn	<p>Hot Zone Charger Control</p> <p>Determines if charger is enabled for hot temperature zone.</p> <p>0 = Charging disabled in hot temperature zone.  1 = Charging enabled in hot temperature zone.</p>
HotBatReg[1:0]	<p>Hot Zone Battery Regulation Voltage</p> <p>Sets the modified BatReg[3:0] in the hot temperature zone.</p> <p>00 = BatReg-150mV  01 = BatReg-100mV  10 = BatReg-50mV  11 = BatReg</p>
HotFChg[2:0]	<p>Hot Zone Fast Charge Current Scaling</p> <p>Sets the modified fast charge in the hot temperature zone.</p> <p>000 = 0.2 x IFChg  001 = 0.3 x IFChg  010 = 0.4 x IFChg  011 = 0.5 x IFChg  100 = 0.6 x IFChg  101 = 0.7 x IFChg  110 = 0.8 x IFChg  111 = 1.0 x IFChg</p>
Password[15:0]	<p>Charger Thermal Limit Configuration Password</p> <p>If Write protect enabled, ChargerThermalLimits can be configured using the following password: 0x1E7A</p> <p>If Write Protect enabled, incorrect password will result in System Error 0x11.</p>

**Table 74. ChargerThermalReg\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x18)	0	0	0	1	1	0	0	0

**Table 75. 0x19 – ChargerThermalReg\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x19)	0	0	0	1	1	0	0	1

**Table 76. ChargerThermalReg\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x19)	0	0	0	1	1	0	0	1
APDataIn0	ColdChgEn	—	—	ColdBatReg[1:0]		ColdFChg[2:0]		
APDataIn1	CoolChgEn	—	—	CoolBatReg[1:0]		CoolFChg[2:0]		
APDataIn2	—	—	—	RoomBatReg[1:0]		RoomFChg[2:0]		
APDataIn3	WarmChgEn	—	—	WarmBatReg[1:0]		WarmFChg[2:0]		
APDataIn4	HotChgEn	—	—	HotBatReg[1:0]		HotFChg[2:0]		

**Table 77. 0x1A – Charger\_ControlWrite**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x1A)	0	0	0	1	1	0	1	0
APDataOut0	—	—	—	—	—	—	ThmEn	ChgEn
ThmEn	On/Off Control for Thermal Monitor 0 = Thermal monitor disabled 1 = Thermal monitor enabled							
ChgEn	On/Off Control for Charger (does not affect SYS node). 0 = Charger disabled 1 = Charger enabled							

**Table 78. Charger\_ControlWrite Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x1A)	0	0	0	1	1	0	1	0

**Table 79. 0x1B – Charger\_ControlRead**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x1B)	0	0	0	1	1	0	1	1

**Table 80. Charger\_Control\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x1B)	0	0	0	1	1	0	1	1
APDataIn0	—	—	—	—	—	—	ThmEn	ChgEn

**Table 81. 0x1C – Charger\_ JEITAHyst\_ControlWrite**

MODE	Write								
BIT	B7	B6	B5	B4	B3	B2	B1	B0	
APCmdOut (0x1C)	0	0	0	1	1	1	0	0	
APDataOut0	JEITAHys En	—	—	JEITAHysLvl					
JEITAHys En	JEITA Hysteresis Control 0 = Hysteresis disabled. 1 = Hysteresis enabled.								
JEITAHys Lvl	Amplitude of JEITA Hysteresis (LSB = 0.39%V <sub>DIG</sub> ) 00001 = 0.39%V <sub>DIG</sub> 00010 = 0.78%V <sub>DIG</sub> ... 11111 = 12.09%V <sub>DIG</sub>								

**Table 82. Charger\_ JEITAHyst\_ControlWrite Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x1C)	0	0	0	1	1	1	0	0

**Table 83. Charger\_ JEITAHyst\_ControlRead**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x1D)	0	0	0	1	1	1	0	1

**Table 84. Charger\_ JEITAHyst\_ControlRead Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x1D)	0	0	0	1	1	1	0	1
APDataIn0	JEITAHysEn	—	—	JEITAHysLvl				

## Boost Configuration Commands

Table 85. 0x30 – Bst\_Config\_Write

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x30)	0	0	1	1	0	0	0	0
APDataOut0	—	—	—	—	—	—	BstEn[1:0]	
APDataOut1	—	—	—	—	BstPsvDsc	BstlAdptEn	BstFastStrt	BstFetScale
APDataOut2	—	—	—	—	BstlSet[3:0]			
APDataOut3	—	—	BstVSet[5:0]					
BstEn[1:0]	Boost Enable Configuration (effective only when BstSeq = 111) 00 = Disabled 01 = Enabled 10 = Controlled by MPC_Config_Write command 11 = RESERVED							
BstPsvDsc	Boost Passive Discharge Control 0 = Boost output will be discharged only when entering Off and Hard-Reset modes. 1 = Boost output will be discharged only when entering Off and Hard-Reset modes and when BstEn is set to 000.							
BstlAdptEn	Boost Adaptive Peak Current Control 0 = Inductor peak current fixed at the programmed value by means of BstlSet 1 = Inductor peak current automatically increased to provide better load regulation							
BstFastStrt	Boost Fast Start Time 0 = Time to full current capability during Startup = 100ms 1 = Time to full current capability during Startup = 50ms. Precharge with 2x current							
BstFetScale	Boost FET Scaling 0 = No FET scaling 1 = Active boost FET size scaled down by half to optimize efficiency for low inductor peak current settings							
BstlSet[3:0]	Boost Nominal inductor Peak Current Setting 25mA step resolution 0000 = 100mA 0001 = 125mA 0010 = 150mA .... 1111 = 475mA							
BstVSet[5:0]	Boost Output Voltage Setting Linear scale from 5V to 20V in 250mV increments 000000 = 5V 000001 = 5.25V ... 111011 = 19.75V 111011 = 20V >111100 = Reserved							



**Table 86. Bst\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x30)	0	0	1	1	0	0	0	0

**Table 87. 0x31 – Bst\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x31)	0	0	1	1	0	0	0	1

**Table 88. Bst\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x31)	0	0	1	1	0	0	0	1
APDataIn0	—	—	—	—	—	—	BstEn[1:0]	
APDataIn1	—	—	—	—	BstPsvDsc	BstAdptEn	BstFastStrt	BstFetScale
APDataIn2	—	—	—	—	BstISet[3:0]			
APDataIn3	RESERVED	—	BstVSet[5:0]					
APDataIn4	—	—	—	—	—	BstSeq[2:0]		
BstSeq[2:0]	Boost Enable Configuration (Read only) 000 = Disabled 001 = RESERVED 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = RESERVED 110 = RESERVED 111 = Controlled by Bst1En after 100% of Boot/POR Process Delay Control							

## Buck Configuration Commands

Table 89. 0x35 – Buck1\_Config\_Write

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x35)	0	0	1	1	0	1	0	1
APDataOut0	—	Buck1Psv Dsc	Buck1Sft Strt	Buck1Act Dsc	Buck1Low EMI	Buck1IAdpt En	Buck1Fet Scale	—
APDataOut1	—	—	Buck1VSet[5:0]					
APDataOut2	—	—	Buck1IZCSet[1:0]		Buck1ISet[3:0]			
APDataOut3	—	—	—	—	—	—	Buck1En[1:0]	
Buck1Psv Dsc	Buck1 Passive Discharge Control 0 = Buck1 passively discharged only in Hard-Reset 1 = Buck1 passively discharged in Hard-Reset or Enable Low							
Buck1Sft Strt	Buck1 Soft Start Time Buck1 has reduced current capability during soft-start 0 = 50ms 1 = 25ms							
Buck1Act DSC	Buck1 Active Discharge Control 0 = Buck1 actively discharged only in Hard-Reset 1 = Buck1 actively discharged in Hard-Reset or Enable Low							
Buck1Low EMI	Buck1 Low EMI Mode 0 = Normal operation 1 = Increase rise/fall time on BLX by 3x							
Buck1IAdpt En	Buck1 Adaptive Peak Current Mode 0 = Inductor peak current fixed at the programmed value by means of Buck1ISet 1 = Inductor peak current automatically increased to provide better load regulation							
Buck1FET Scale	Buck1 Force FET Scaling Reduce the FET size by factor 2. Use it to optimize the efficiency for Buck1Iset <100mA 0: FET scaling disabled 1: FET scaling enabled							
Buck1VSet [5:0]	Buck1 Output Voltage Setting 0.8V to 2.375V, Linear Scale, 25mV increments 000000 = 0.8V 000001 = 0.825V ... 111111 = 2.375V							

**Table 89. 0x35 – Buck1\_Config\_Write (continued)**

Buck1IZC Set[1:0]	Buck1 Zero Crossing Current Threshold Optimizes Buck1 for a given voltage setting. 00 = 10mA, Use for Buck1VSet < 1V 01 = 20mA, Use for 1V < Buck1VSet < 1.8V 10 = 30mA, Use for 1.8V < Buck1VSet < 3V 11 = 40mA, Use for Buck1Vset > 3V
Buck1ISet [3:0]	Buck1 Inductor current Peak Current Setting 25mA step 0000 = 0mA 0001 = 25mA 1111 = 375mA
Buck1En [1:0]	Buck1 Enable Configuration (effective only when Buck1Seq == 111) 00 = Disabled: BK1OUT not actively discharged unless Hard-Reset/Shutdown/Off mode 01 = Enabled 10 = Controlled by MPC_ (See MPC_Config_Write) 11 = RESERVED

**Table 90. Buck1\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x35)	0	0	1	1	0	1	0	1

**Table 91. 0x36 – Buck1\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x36)	0	0	1	1	0	1	1	0

**Table 92. Buck1\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
<b>APResponse (0x36)</b>	0	0	1	1	0	1	1	0
<b>APDataIn0</b>	—	Buck1Psv Dsc	Buck1Fast	Buck1Act Dsc	Buck1Low EMI	Buck1En Fmax	Buck1Fet Scale	—
<b>APDataIn1</b>	—	—	Buck1VSet[5:0]					
<b>APDataIn2</b>	—	—	Buck1IZCSet[1:0]		Buck1Set[3:0]			
<b>APDataIn3</b>	—	—	—	—	—	—	Buck1En[1:0]	
<b>APDataIn4</b>	—	—	—	—	—	Buck1Seq[2:0]		
Buck1Seq [2:0]	Buck1 Enable Configuration (Read only) 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/ POR Process Delay Control 011 = Enabled at 25% of Boot/ POR Process Delay Control 100 = Enabled at 50% of Boot/ POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by Buck1En [1:0] after 100% of Boot/POR Process Delay Control							

**Table 93. 0x37 – Buck1\_DVSConfig\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
<b>APCmdOut (0x37)</b>	0	0	1	1	0	1	1	1
<b>APDataOut0</b>	—	—	Buck1VSet[5:0]					
<b>APDataOut1</b>	—	—	Buck1AlternateVSet[5:0]					
<b>APDataOut2</b>	—	—	—	MPC4	MPC3	MPC2	MPC1	MPC0
Buck1VSet [5:0]	Buck1 Voltage Setting for Dynamic Voltage Scaling Function: This is the voltage set on Buck1 after a positive edge on MPC_. 0.8V to 2.375V, Linear Scale, 25mV increments 000000 = 0.8V 000001 = 0.825V ... 111111 = 2.375V							
Buck1AlternateVSet[5:0]	Buck1 Alternate Voltage Setting for Dynamic Voltage Scaling Function: This is the voltage set on Buck1 upon writing this command or after a negative edge on MPC_. 0.8V to 2.375V, Linear Scale, 25mV increments 000000 = 0.8V 000001 = 0.825V ... 111111 = 2.375V							
MPC_	This selects the MPC pin used for alternate voltage function. If an MPC is used for dynamic voltage scaling, all other functions of that MPC are disabled. MPC works on edge, so the static value of MPC does not matter.							

**Table 94. Buck1\_DVSCfg\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x37)	0	0	1	1	0	1	1	1

**Table 95. 0x3A – Buck2\_Config\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x3A)	0	0	1	1	1	0	1	0
APDataOut0	—	Buck2Psv Dsc	Buck2Sft Strt	Buck2Act Dsc	Buck2Low EMI	Buck2IAdpt En	Buck2Fet Scale	—
APDataOut1	—	—	Buck2VSet[5:0]					
APDataOut2	—	—	Buck2IZCSet[1:0]		Buck2ISet[3:0]			
APDataOut3	—	—	—	—	—	—	Buck2En[1:0]	
Buck2Psv DSC	Buck2 Passive Discharge Control 0 = Buck2 passively discharged only in Hard-Reset 1 = Buck2 passively discharged in Hard-Reset or Enable Low							
Buck2SftStrt	Buck2 Soft Start Time Buck2 has reduced current capability during soft-start 0 = 50ms 1 = 25ms							
Buck2Act DSC	Buck2 Active Discharge Control 0 = Buck2 actively discharged only in Hard-Reset 1 = Buck2 actively discharged in Hard-Reset or Enable Low							
Buck2Low EMI	Buck2 Low EMI Mode 0 = Normal operation 1 = Increase rise/fall time on BLX by 3x							
Buck2IAdpt En	Buck2 Adaptive Peak Current Mode 0 = Inductor peak current fixed at the programmed value by means of Buck1Iset 1 = Inductor peak current automatically increased to provide better load regulation							
Buck2FET Scale	Buck2 Force FET Scaling Reduce the FET size by factor 2. Use it to optimize the efficiency for Buck1Iset <100mA 0 = FET scaling disabled 1 = FET scaling enabled							
Buck2VSet [5:0]	Buck2 Output Voltage Setting 0.8V to 3.95V, Linear Scale, 50mV increments 000000 = 0.8V 000001 = 0.85V ... 111111 = 3.95V							

**Table 95. 0x3A – Buck2\_Config\_Write (continued)**

Buck2IZCSet [1:0]	Buck2 Zero Crossing Current Threshold Optimizes Buck2 for a given voltage setting. 00 = 10mA, Use for Buck2VSet < 1V 01 = 20mA, Use for 1V < Buck2VSet < 1.8V 10 = 30mA, Use for 1.8V < Buck2VSet < 3V 11 = 40mA, Use for Buck2Vset > 3V
Buck2ISet [3:0]	Buck2 Inductor Current Peak Current Setting 25mA step 0000 = 0mA 0001 = 25mA 1111 = 375mA
Buck2En[1:0]	Buck2 Enable Configuration (effective only when Buck2Seq == 111) 00 = Disabled 01 = Enabled 10 = Controlled by MPC_Config_Write command 11 = Reserved

**Table 96. Buck2\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x3B)	0	0	1	1	1	0	1	0

**Table 97. 0x3B – Buck2\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x3B)	0	0	1	1	1	0	1	1

**Table 98. Buck2\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
<b>APResponse (0x3B)</b>	0	0	1	1	1	0	1	1
APDataIn0	—	Buck2Psv Dsc	Buck2Sft Strt	Buck2Act Dsc	Buck2Low EMI	Buck2IAdpt En	Buck2Fet Scale	—
APDataIn1	—	—	Buck2VSet[5:0]					
APDataIn2	—	—	Buck2IZCSet[1:0]		Buck2ISet[3:0]			
APDataIn3	—	—	—	—	—	—	Buck2En[1:0]	
APDataIn4	—	—	—	—	—	Buck2Seq[2:0]		
Buck2Seq [2:0]	Buck2 Enable Configuration (Read Only) 000 = Disabled 001 = RESERVED 010 = Enabled at 0% of Boot/ POR Process Delay Control 011 = Enabled at 25% of Boot/ POR Process Delay Control 100 = Enabled at 50% of Boot/ POR Process Delay Control 101 = RESERVED 110 = RESERVED 111 = Controlled by Buck2En [1:0] after 100% of Boot/POR Process Delay Control							

**Table 99. 0x3C – Buck2\_DVSConfig\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
<b>APCmdOut (0x3C)</b>	0	0	1	1	1	1	0	0
APDataOut0	—	—	Buck2VSet[5:0]					
APDataOut1	—	—	Buck2AlternateVSet[5:0]					
APDataOut2	—	—	—	MPC4	MPC3	MPC2	MPC1	MPC0
Buck2VSet [5:0]	Buck2 Voltage Setting for Dynamic Voltage Scaling Function: This is the voltage set on Buck2 after a positive edge on MPC_ 0.8V to 3.95V, Linear Scale, 50mV increments 000000 = 0.8V 000001 = 0.85V ... 111111 = 3.95V							
Buck2AlternateVSet[5:0]	Buck2 Alternate Voltage Setting for Dynamic Voltage Scaling Function: This is the voltage set on Buck2 upon writing this command or after a negative edge on MPC_ 0.8V to 3.95V, Linear Scale, 50mV increments 000000 = 0.8V 000001 = 0.85V ... 111111 = 3.95V							
MPC_	This selects the MPC pin used for alternate voltage function. If an MPC is used for dynamic voltage scaling, all other functions of that MPC are disabled. MPC works on edge, so the static value of MPC does not matter.							

**Table 100. Buck2\_DVSConfig\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x3C)	0	0	1	1	1	1	0	0

**LDO Configuration Commands****Table 101. 0x40 – LDO1\_Config\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x40)	0	1	0	0	0	0	0	0
APDataOut0	—	—	—	LDO1Pas Dsc	LDO1Act Dsc	LDO1Md	LDO1En[1:0]	
APDataOut1	—	—	LDO1VSet[5:0]					
LDO1Pas Dsc	LDO1 Passive Discharge Control 0 = LDO1 output will be discharged only entering Off and Hard-Reset modes. 1 = LDO1 output will be discharged only entering Off and Hard-Reset modes and when the enable is Low							
LDO1Act Dsc	LDO1 Active Discharge Control 0 = LDO1 output will be actively discharged only in Hard-Reset mode 1 = LDO1 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low							
LDO1Md	LDO1 Mode Control When FET is On, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled. 0 = Normal LDO operating mode 1 = Load switch mode. FET is either fully On or Off depending on state of LDO1En.							
LDO1En [1:0]	LDO1 Enable Configuration (effective only when LDO1Seq[2:0] == 111) 00 = Disabled 01 = Enabled 10 = Controlled by MPC_Config_Write command 11 = Controlled by LDODirect register							
LDO1VSet [5:0]	LDO1 Output Voltage Setting—Limited by input supply 0.5V to 1.95V, Linear Scale, 25mV increments 000000 = 0.5V 000001 = 0.525V ... 111010 = 1.95V >111010 = Limited by input supply							



**Table 102. LDO1\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x40)	0	1	0	0	0	0	0	0

**Table 103. 0x41 – LDO1\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x41)	0	1	0	0	0	0	0	1

**Table 104. LDO1\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x41)	0	1	0	0	0	0	0	1
APDataIn0	—	—	—	LDO1Pas Dsc	LDO1Act Dsc	LDO1Md	LDO1En[1:0]	
APDataIn1	—	—	—	LDO1VSet[4:0]				
APDataIn2	—	—	—	—	—	LDO1Seq[2:0]		
LDO1Seq [2:0]	LDO1 Enable Configuration (Read only) 000 = Disabled 001 = RESERVED 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = RESERVED 110 = RESERVED 111 = Controlled by LDO1En [1:0] after 100% of Boot/POR Process Delay Control							

Table 105. 0x42 – LDO2\_Config\_Write

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x42)	0	1	0	0	0	0	1	0
APDataOut0	—	—	—	LDO2Pas Dsc	LDO2Act Dsc	LDO2Md	LDO2En[1:0]	
APDataOut1	—	—	—	LDO2VSet[4:0]				
LDO2Pas Dsc	LDO2 Passive Discharge Control 0 = LDO2 output will be discharged only entering Off and Hard-Reset modes. 1 = LDO2 output will be discharged only entering Off and Hard-Reset modes and when the enable is low.							
LDO2Act Dsc	LDO2 Active Discharge Control 0 = LDO2 output will be actively discharged only in Hard-Reset mode 1 = LDO2 output will be actively discharged in Hard-Reset mode and also when its Enable goes Low							
LDO2Md	LDO2 Mode Control When FET is On, the output is unregulated. This setting is internally latched and can change only when the LDO2 is disabled. 0 = Normal LDO2 operating mode 1 = Load switch mode. FET is either fully On or Off depending on state of LDO2En							
LDO2En [1:0]	LDO2 Enable Configuration (effective only when LDO2Seq[2:0] == 111) 00 = Disabled 01 = Enabled 10 = Controlled by MPC_Config_Write command 11 = Controlled by LDODirect register							
LDO2VSet [4:0]	LDO2 Output Voltage Setting—Limited by input supply 0.9V to 4V, Linear Scale, 100mV increments 000000 = 0.9V 000001 = 1V ... 111110 = 3.9V 111111 = 4V							

**Table 106. LDO2\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x42)	0	1	0	0	0	0	1	0

**Table 107. 0x43 – LDO2\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x43)	0	1	0	0	0	0	1	1

**Table 108. LDO2\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x43)	0	1	0	0	0	0	1	1
APDataIn0	—	—	—	LDO2Pas Dsc	LDO2Act Dsc	LDO2Md	LDO2En[1:0]	
APDataIn1	—	—	—	LDO2VSet[4:0]				
APDataIn2	—	—	—	—	—	LDO2Seq[2:0]		
LDO2Seq [2:0]	LDO2 Enable Configuration (Read only) 000 = Disabled 001 = Enabled always when BAT/SYS is present 010 = Enabled at 0% of Boot/ POR Process Delay Control 011 = Enabled at 25% of Boot/ POR Process Delay Control 100 = Enabled at 50% of Boot/ POR Process Delay Control 101 = RESERVED 110 = RESERVED 111 = Controlled by LDO2En [1:0] after 100% of Boot/POR Process Delay Control							

## Charge Pump Configuration Commands

### Table 109. 0x46 – ChargePump\_Config\_Write

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x46)	0	1	0	0	0	1	1	0
APDataOut0	—	—	—	—	—	—	CPEn[1:0]	
APDataOut1	—	—	—	—	—	—	CPPscDisch	CPVSet
CPEn[1:0]	Charge Pump Enable Configuration (effective only when CPSeq = 111) 00 = Disabled 01 = Enabled 10 = Controlled by MPC_Config_Write command 11 = RESERVED							
CPpsvDisch	Charge Pump Passive Discharge Enable 0 = Disabled 1 = Enabled							
CPVSet	0 = 6.6V 1 = 5V							

### Table 110. ChargePump\_Config\_Write Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x46)	0	1	0	0	0	1	1	0

### Table 111. 0x47 – ChargePump\_Config\_Read

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x47)	0	1	0	0	0	1	1	1

**Table 112. ChargePump\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x47)	0	1	0	0	0	1	1	1
APDataIn0	—	—	—	—	—	—	CPEn[1:0]	
APDataIn1	—	—	—	—	—	—	CPPscDisch	CPVSet
APDataIn2	—	—	—	—	—	CPSeq[2:0]		
CPSeq[2:0]	Charge Pump Enable Configuration (Read only) 000 = Disabled 001 = RESERVED 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = RESERVED 110 = RESERVED 111 = Controlled by CPEn after 100% of Boot/POR Process Delay Control							

**SFOUT Configuration Commands****Table 113. 0x48 – SFOUT\_Config\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x48)	0	1	0	0	1	0	0	0
APDataOut0	—	—	—	—	—	SFOUTV Set	SFOUTEn[1:0]	
SFOUTV Set	SFOUT Output Voltage Setting 0 = 5V 1 = 3.3V							
SFOUTE n[1:0]	SFOUT LDO Enable Configuration 00 = Disabled (regardless of CHGIN) 01 = Enabled when CHGIN is present 10 = Enabled when CHGIN is present and Controlled by MPC_Config_Write command 11 = RESERVED							

**Table 114. SFOUT\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x48)	0	1	0	0	1	0	0	0

**Table 115. 0x49 – SFOUT\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x49)	0	1	0	0	1	0	0	1

**Table 116. SFOUT\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x49)	0	1	0	0	1	0	0	1
APDataIn0	—	—	—	—	—	SFOUTVSet	SFOUTEn[1:0]	

## MON Mux Configuration Commands

Table 117. 0x50 – MONMux\_Config\_Write

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x50)	0	1	0	1	0	0	0	0
APDataOut0	MONEn	—	MONHiZ	MONRatioCfg[1:0]		MONCtrl[2:0]		
MONEn	Enable Signal For MON Mux 0 = MON is not connected to any internal node and its state depends on MONHiZ 1 = MON is connected based on MONCtrl[2:0] configuration							
MONHiZ	MON Off Mode Condition 0 = Pulled LOW by 59kΩ pulldown resistor 1 = Hi-Z							
MONRatio Cfg[1:0]	MON Resistive Partition Selector 00 = 1:1 01 = 2:1 10 = 3:1 11 = 4:1							
MONCtrl[2:0]	MON Pin Source Selection (80μs BBM after any change of MONCtrl[2:0]) 000 = MON connected to a resistive partition of BAT 001 = MON connected to a resistive partition of SYS 010 = MON connected to a resistive partition of BK2OUT 011 = MON connected to a resistive partition of BK1OUT 100 = MON connected to a resistive partition of L2OUT 101 = MON connected to a resistive partition of L1OUT 110 = MON connected to a resistive partition of SFOUT 111 = MON connected to a resistive partition of BBOUT							

Table 118. MONMux\_Config\_Write Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x51)	0	1	0	1	0	0	0	0

Table 119. 0x51 – MONMux\_Config\_Read

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x51)	0	1	0	1	0	0	0	1

**Table 120. MONMux\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x51)	0	1	0	1	0	0	0	1
APDataIn0	MONEN	—	MONHiZ	MONRatioCfg[1:0]		MONCtrl[2:0]		

**Table 121. 0x53 – ADC\_Measure\_Launch**

MODE	Launch							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x53)	0	1	0	1	0	0	1	1
APDataOut0	—	—	ADCAvgSiz[2:0]			ADCSel[2:0]		
ADCAvgSiz[2:0]	ADC Averaging Size ADC performs $2^{\text{ADCAvgSiz}[2:0]}$ consecutive averaged measurements							
ADCSel[2:0]	ADC Channel Selection 000 = SYS 001 = MON 010 = THM 011 = CHGIN 100 = CPOUT 101 = BSTOUT 11x = RESERVED							

**Table 122. ADC\_Measure\_Launch Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x53)	0	1	0	1	0	0	1	1
APDataIn0	—	—	—	—	—	—	ADCResult[1:0]	
APDataIn1	ADCMax[7:0]							
APDataIn2	ADCMin[7:0]							
APDataIn3	ADCAvg[7:0]							
ADCResult	ADC Result Ready 00 = Success, measurement completed 01 = ADC busy 10 = ADC measurement aborted by Haptic Automatic Level Compensation engine 11 = RESERVED							
ADCMax[7:0]	ADC Maximum Value Contains the maximum value measured by the ADC							
ADCMin[7:0]	ADC Minimum Value Contains the minimum value measured by the ADC							
ADCAvg[7:0]	ADC Average Value Contains the average value of $2^{\text{ADCAvgSiz}[2:0]}$ ADC measurements							



## Buck-Boost Configuration Commands

Table 123. 0x70 – BBst\_Config\_Write

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x70)	0	1	1	1	0	0	0	0
APDataOut0	RESERVED (Set to 0x00)							
APDataOut1	—	—	—	—	—	BBstlSet[2:0]		
APDataOut2	—	—	BBstVSet[4:0]					
APDataOut3	—	BBstRip Red	BBstAct Dsc	BBstPas Dsc	BBstMd	BBstlnd	BBstEn[1:0]	
BBstlSet [2:0]	Buck-Boost Peak Current Limit Setting 000 = 0 (Minimum On-time) 001 = 50mA 010 = 100mA 011 = 150mA 100 = 200mA 101 = 250mA 110 = 300mA 111 = 350mA							
BBstVSet [4:0]	Buck-Boost Output Voltage Setting This setting is internally latched and can change only when Buck-Boost is Disabled. 2.5V to 5.0V, Linear Scale, 100mV increments 000000 = 2.5V 000001 = 2.6V ... 011001 = 5.0V >011001 = 5.0V							
BBstRip Red	Buck-Boost Ripple Reduction Leave set to 1							
BBstAct Dsc	Buck-Boost Active Discharge Control 0 = Actively discharged only in Hard-Reset 1 = Actively discharged in Hard-Reset or Enable Low							
BBstPas Dsc	Buck-Boost Passive Discharge Control 0 = Passively discharged only in Hard-Reset 1 = Passively discharged in Hard-Reset or Enable Low							

**Table 123. 0x70 – BBst\_Config\_Write (continued)**

BBstMd	Buck-Boost EMI Reduction 0 = Damping enabled 1 = Damping disabled
BBstInd	Buck-Boost Inductance select 0 = Inductance is 4.7 $\mu$ H 1 = Inductance is 3.3 $\mu$ H
BBstEn [1:0]	Buck-Boost Enable Configuration (effective only when BBstSeq[2:0] == 111) 00 = Disabled 01 = Enabled 10 = Controlled by MPC_Config_Write command 11 = RESERVED

**Table 124. BBst\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x70)	0	1	1	1	0	0	0	0

**Table 125. 0x71 – BBst\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x71)	0	1	1	1	0	0	0	1

Table 126. BBst\_Config\_Read Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x71)	0	1	1	1	0	0	0	1
APDataIn0	ClkDiv Ena	ClkDivSet[6:0]						
APDataIn1	—	—	—	—	—	BBstISet[2:0]		
APDataIn2	—	—	—	BBstVSet[4:0]				
APDataIn3	—	—	BBstActDsc	BBstPasDsc	BBstMd	BBstInd	BBstEn[1:0]	
APDataIn4	—	—	—	—	—	BBstSeq[2:0]		
BBstSeq [2:0]	Buck-Boost Enable Configuration (Read only) 000 = Disabled 001 = RESERVED 010 = Enabled at 0% of Boot/ POR Process Delay Control 011 = Enabled at 25% of Boot/ POR Process Delay Control 100 = Enabled at 50% of Boot/ POR Process Delay Control 101 = RESERVED 110 = RESERVED 111 = Controlled by BBstEn [1:0] after 100% of Boot/POR Process Delay Control							

## Haptic Configuration Commands

Table 127. 0xA0 – Hpt\_Config\_Write0

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xA0)	1	0	1	0	0	0	0	0
APDataOut0	—	—	—	—	EmfEn	HptSel	AlcMod	ZccHysEn
APDataOut1	IniGss[7:0]							
APDataOut2	ZccSlowEn	—	—	FltrCntrEn	IniGss[11:8]			
APDataOut3	—	—	—	IniDly[4:0]				
APDataOut4	—	—	WidWdw[5:0]					
APDataOut5	—	—	NarWdw[5:0]					
EmfEn	Back EMF and Resonance Detection Control Can also be set using opcode 0xAD. 0 = Disabled 1 = Enabled							
HptSel	Haptic Mode Select Can also be set using opcode 0xAD. 0 = ERM Mode 1 = LRA Mode							
AlcMod	Automatic Level Compensation (ALC) Control Can also be set using opcode 0xAD. 0 = Disabled 1 = Enabled							
ZccHysEn	Zero-Crossing Comparator Hysteresis Control Can also be set using opcode 0xAD 0 = Disabled 1 = Enabled (6mV typ).							
IniGss [11:0]	Back EMF Initial Guess Can also be set using opcode 0xAE. Initial estimate for BEMF frequency = $((25.6\text{MHz}/64) / \text{IniGss}[11:0])$							
ZccSlowEn	Zero-Crossing Comparator Slow-Down Enable Can also be set using opcode 0xBA. 0 = Zero-crossing comparator operates in normal mode. 1 = Slows down the zero-crossing comparator by 2X for stronger antialiasing filtering.							

**Table 127. 0xA0 – Hpt\_Config\_Write0 (continued)**

FtrCntrEn	Zero-Crossing Event Capturing Filter Enable Can also be set using opcode 0xBA 0 = Zero-crossing measured using single comparator. 1 = Zero-crossing measured using an up/down counter (samples at 25.6MHz). Samples the output of the comparator for the whole duration of the enabled window (wide or narrow). The counter starts at zero (mid-code) and will end at a positive or negative code depending on whether the average zero-crossing event occurs before or after than the expected time. The closer the zero-crossing is on average to the expected time, the closer to zero code returned at the end of the window will be. Phase error (in 25.6MHz period units) can be calculated by dividing the resulting code at the end of the window by 2. The usage of the up/down counter enables filtering/noise rejection that could otherwise cause a systematic shift in the phase error detected.
IniDly[4:0]	Number of sine wave periods to be skipped before (re)starting BEMF measurement after: Start of vibration pattern. Change of output polarity (e.g., braking) Programmed percentage output amplitude (w.r.t. $V_{FS}$ ) becomes again higher than EmfSkipTh[6:0] after having previously gone below it. Can also be set using Opcode 0xAF.
WidWdw [5:0]	Wide window duration for BEMF zero-crossing detection (LSB is (1/64) of currently imposed sinewave period). Can also be set using Opcode 0xB0
NarWdw [5:0]	Narrow window duration for BEMF zero-crossing detection (LSB is (1/64) of currently imposed sinewave period). Can also be set using Opcode 0xB0

**Table 128. Hpt\_Config\_Write0 Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xA0)	1	0	1	0	0	0	0	0

**Table 129. 0xA1 – Hpt\_Config\_Read0**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xA1)	1	0	1	0	0	0	0	1

Table 130. Hpt\_Config\_Read0 Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xA1)	1	0	1	0	0	0	0	1
APDataIn0	—	—	—	—	EmfEn	HptSel	AlcMod	ZccHysEn
APDataIn1	IniGss[7:0]							
APDataIn2	ZccSlow En	—	—	FltrCntrEn	IniGss[11:8]			
APDataIn3	—	—	—	IniDly[4:0]				
APDataIn4	—	—	WidWdw[5:0]					
APDataIn5	—	—	NarWdw[5:0]					

Table 131. 0xA2 – Hpt\_Config\_Write1

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xA2)	1	0	1	0	0	0	1	0
APDataOut0	EmfSkipCyc[7:0]							
APDataOut1	BlankWdw[7:0]							
APDataOut2	—	—	—	—	—	BlankWdw[10:8]		
APDataOut3	HptVfs[7:0]							
APDataOut4	ETRGdAmp[7:0]							
APDataOut5	ETRGdDur [7:0]							
EmfSkipCyc [7:0]	Sets number of consecutive sine wave periods during which BEMF detection is skipped after a BEMF detection completes. Can also be set using opcode 0xB1.							
BlankWdw [10:0]	Zero-crossing comparator blanking time after enable (LSB = 1/25.6MHz) Can also be set using opcode 0xB9.							
HptVfs[7:0]	Stores the full-scale voltage ( $V_{FS}$ ) to which the desired percentage output amplitude is referred. The actual $V_{FS}$ will be the minimum between the value programmed on HptVfs[7:0] and the current SYS value. LSB = 21.57mV Can also be set using opcode 0xB2.							
ETRGdAmp[7:0]	Sets amplitude of the overdrive period as a percentage of $V_{FS}$ (ETRG mode). LSB = 0.78% $V_{FS}$ . Note that the MSB represents the sign of the amplitude to be driven. Can also be set using opcode 0xB3.							
ETRGdDur [7:0]	Sets duration of the overdrive period. LSB = 5ms Can also be set using opcode 0xB3. (ETRG mode)							

Table 132. Hpt\_Config\_Write1 Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xA2)	1	0	1	0	0	0	1	0

Table 133. 0xA3 – Hpt\_Config\_Read1

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xA3)	1	0	1	0	0	0	1	1

Table 134. Hpt\_Config\_Read1 Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xA3)	1	0	1	0	0	0	1	1
APDataIn0	EmfSkipCyc[7:0]							
APDataIn1	BlankWdw[7:0]							
APDataIn2	—	—	—	—	—	BlankWdw[10:8]		
APDataIn3	HptVfs[7:0]							
APDataIn4	ETRGdAmp[7:0]							
APDataIn5	ETRGdDur [7:0]							

Table 135. 0xA4— Hpt\_Config\_Write2

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xA4)	1	0	1	0	0	1	0	0
APDataOut0	ETRActAmp[7:0]							
APDataOut1	ETRActDur[7:0]							
APDataOut2	ETRBrkAmp[7:0]							
APDataOut3	ETRBrkDur[7:0]							
APDataOut4	—	NarLpGain[2:0]			—	WidLpGain[2:0]		
APDataOut5	—	—	NarCntLck[5:0]					
ETRActAmp[7:0]	Sets amplitude of the normal drive period as a percentage of $V_{FS}$ (ETRG mode). LSB = $0.78\%V_{FS}$ plus sign bit. Can also be set using opcode 0xB3.							
ETRActDur[7:0]	Sets duration of the normal drive period. LSB = 10ms (ETRG mode) Can also be set using opcode 0xB3.							
ETRBrkAmp[7:0]	Sets amplitude of the braking period as a percentage of $V_{FS}$ (ETRG mode). LSB = $0.78\%V_{FS}$ plus sign bit. Can also be set using opcode 0xB3.							
ETRBrkDur[7:0]	Sets duration of the braking period. LSB = 5ms (ETRG mode) Can also be set using opcode 0xB3.							
NarLpGain [2:0]	Sets gain by which the phase delay found by the zero-crossing comparator is multiplied to calculate the shift for the new sinewave period with respect to the previously imposed sinewave. This value is used when the narrow window is active. Can also be set using opcode 0xB4. 000 = 1 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 1/32 110 = 1/64 111 = 1/128							
WidLpGain [2:0]	Sets gain by which the phase delay found by the zero-crossing comparator is multiplied to calculate the shift for the new sinewave period with respect to the previously imposed sinewave. This value is used when the wide window is active. Can also be set using opcode 0xB4. 000 = 1 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 1/32 110 = 1/64 111 = 1/128							
NarCntLck [5:0]	Sets number of consecutive periods where phase delay falls within the narrow window before detection window is reduced from wide to narrow. Can also be set using opcode 0xB5.							



Table 136. Hpt\_Config\_Write2 Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xA4)	1	0	1	0	0	1	0	0

Table 137. 0xA5 – Hpt\_Config\_Read2

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xA5)	1	0	1	0	0	1	0	1

Table 138. Hpt\_Config\_Read2 Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xA5)	1	0	1	0	0	1	0	1
APDataIn0	ETRGActAmp[7:0]							
APDataIn1	ETRGActDur[7:0]							
APDataIn2	ETRGBrkAmp[7:0]							
APDataIn3	ETRGBrkAmp[7:0]							
APDataIn4	—	NarLpGain[2:0]			—	WidLpGain[2:0]		
APDataIn5	—	—	NarCntLck[5:0]					

Table 139. 0xA6 – Hpt\_SYS\_Threshold\_Config\_Write

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xA6)	1	0	1	0	0	1	1	0
APDataOut0	HptSysUVLO[7:0]							
HptSys UVLO[7:0]	Haptic SYS UVLO Threshold Sets the SYS undervoltage threshold. If $V_{SYS}$ falls below this UVLO threshold, the haptic driver is locked (HptLock = 1) and System-Error[7:0] = 0x25 is issued. See Opcode 0xA8 for details on restarting the haptic driver. LSB = 5.5V/255							

Table 140. Hpt\_SYS\_threshold\_Config\_Write Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xA6)	1	0	1	0	0	1	1	0

**Table 141. 0xA7—Hpt\_SYS\_threshold\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xA7)	1	0	1	0	0	1	1	1

**Table 142. Hpt\_SYS\_threshold\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xA7)	1	0	1	0	0	1	1	1
APDataIn0	HptSysUVLO[7:0]							

**Table 143. 0xA8 – Hpt\_Lock\_Config\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xA8)	1	0	1	0	1	0	0	0
APDataOut0	—	—	—	—	—	—	—	HptLock
HptLock	Haptic Driver Lock When a fault condition causes the haptic driver to lock, this bit can only be cleared by manually writing HptLock = 0 to opcode 0xA8. The haptic driver output will be off while HptLock = 1. 0 = Unlock Haptic Driver 1 = Lock Haptic Driver							

**Table 144. Hpt\_Lock\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xA8)	1	0	1	0	1	0	0	0

**Table 145. 0xA9 – Hpt\_Lock\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xA9)	1	0	1	0	1	0	0	1

**Table 146. Hpt\_Lock\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xA9)	1	0	1	0	1	0	0	1
APDataIn0	—	—	—	—	—	—	—	HptLock

**Table 147. 0xAA – Hpt\_EMF\_Threshold\_Config\_Write**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xAA)	1	0	1	0	1	0	1	0
APDataOut0	—	EmfSkipTh[6:0]						
EMFSkipTh [6:0]	Back EMF Skip Threshold Percentage of the full-scale output amplitude under which to skip the BEMF measurement as the returned BEMF would be too small to measure in these cases.							

**Table 148. Hpt\_EMF\_Threshold\_Config\_Write Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xAA)	1	0	1	0	1	0	1	0

**Table 149. 0xAB – Hpt\_EMF\_Threshold\_Config\_Read**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xAB)	1	0	1	0	1	0	1	1

**Table 150. HPT\_EMF\_Threshold\_Config\_Read Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xAB)	1	0	1	0	1	0	1	1
APDataIn0	—				EmfSkipTh[6:0]			

**Table 151. 0xAC—HPT\_Autotune**

MODE	Launch							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xAC)	1	0	1	0	1	1	0	0

**Table 152. HPT\_Autotune Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xAC)	1	0	1	0	1	1	0	0
APDataIn0	Result[7:0]							
APDataIn1	BEMFPeriod[7:0]							
APDataIn2	—	—	—	—	BEMFPeriod[11:8]			
Result [7:0]	0x00 = Auto-tune done, BEMFPeriod[11:0] available. 0x01 = Auto-tune failed.							
BEMFPeriod [11:0]	Resonant frequency resolved by autotune function = $((25.6\text{MHz} / 64) / \text{BEMF\_freq})$							

**Table 153. 0xAD— HPT\_SetMode**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xAD)	1	0	1	0	1	1	0	1
APDataOut0	—	—	—	—	EmfEn	HptSel	AlcMod	ZccHysEn

**Table 154. HPT\_SetMode Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xAD)	1	0	1	0	1	1	0	1

**Table 155. 0xAE— HPT\_SetInitialGuess**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xAE)	1	0	1	0	1	1	1	0
APDataOut0	IniGss[7:0]							
APDataOut1	—	—	—	—	IniGss[11:8]			

**Table 156. HPT\_SetInitialGuess Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xAE)	1	0	1	0	1	1	1	0

**Table 157. 0xAF— HPT\_SetInitialDelay**

MODE	Write								
BIT	B7	B6	B5	B4	B3	B2	B1	B0	
APCmdOut (0xAF)	1	0	1	0	1	1	1	1	
APDataOut0	—	—	—	IniDly[4:0]					

**Table 158. HPT\_SetInitialDelay Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xAF)	1	0	1	0	1	1	1	1

**Table 159. 0xB0—HPT\_SetWindow**

MODE	Write								
BIT	B7	B6	B5	B4	B3	B2	B1	B0	
APCmdOut (0xB0)	1	0	1	1	0	0	0	0	
APDataOut0	—	—	WidWdw[5:0]						
APDataOut1	—	—	NarWdw[5:0]						

**Table 160. HPT\_SetWindow Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xB0)	1	0	1	1	0	0	0	0

**Table 161. 0xB1 – HPT\_SetBackEMFCycle**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xB1)	1	0	1	1	0	0	0	1
APDataOut0	EmfSkipCyc[7:0]							

**Table 162. HPT\_SetBackEMFCycle Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xB1)	1	0	1	1	0	0	0	1

**Table 163. 0xB2—HPT\_SetFullScale**

MODE	Write—							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xB2)	1	0	1	1	0	0	1	0
APDataOut0	HptVfs[7:0]							

**Table 164. HPT\_SetFullScale Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xB2)	1	0	1	1	0	0	1	0

**Table 165. 0xB3—Hpt\_SetHptPattern**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xB3)	1	0	1	1	0	0	1	1
APDataOut0	ETRGdAmp[7:0]							
APDataOut1	ETRGdDur[7:0]							
APDataOut2	ETRGActAmp[7:0]							
APDataOut3	ETRGActDur[7:0]							
APDataOut4	ETRGBrkAmp[7:0]							
APDataOut5	ETRGBrkDur[7:0]							

**Table 166. Hpt\_SetHptPattern Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xB3)	1	0	1	1	0	0	1	1

**Table 167. 0xB4—Hpt\_SetGain**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xB4)	1	0	1	1	0	1	0	0
APDataOut0	—	NarLpGain[2:0]			—	WidLpGain[2:0]		

**Table 168. Hpt\_SetGain Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xB4)	1	0	1	1	0	1	0	0

**Table 169. 0xB5—HPT\_SetLock**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xB5)	1	0	1	1	0	1	0	1
APDataOut0	—	—	NarCntLck[5:0]					

**Table 170. Hpt\_SetLock Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xB5)	1	0	1	1	0	1	0	1

**Table 171. 0xB6—Hpt\_ReadResonanceFrequency**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xB6)	1	0	1	1	0	1	1	0

**Table 172. Hpt\_ReadResonanceFrequency Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xB6)	1	0	1	1	0	1	1	0
APDataIn0	BEMFPeriod[7:0]							
APDataIn1	—	—	—	—	BEMFPeriod[11:8]			

**Table 173. 0xB7—Hpt\_SetTimeout**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xB7)	1	0	1	1	0	1	1	1
APDataOut0	—	—	HptDrvTmo[5:0]					
	Haptic Driver Timeout See Opcode 0xA8 for details on restarting the haptic driver. 1s Step resolution. If timeout is reached, the haptic driver is locked (HptLock = 1) and SystemError[7:0] = 0x04 is issued. 000000 = Disabled 000001 = 1s							

**Table 174. Hpt\_SetTimeout Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xB7)	1	0	1	1	0	1	1	1

**Table 175. 0xB8—Hpt\_GetTimeout**

MODE	Read							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xB8)	1	0	1	1	1	0	0	0

**Table 176. Hpt\_GetTimeout Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0	
APResponse (0xB8)	1	0	1	1	1	0	0	0	
APDataIn0	—	—	HptDrvTmo[5:0]						

**Table 177. 0xB9—Hpt\_SetBlankingWindow**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xB9)	1	0	1	1	1	0	0	1
APDataOut0	BlankWdw[7:0]							
APDataOut1	—	—	—	—	—	BlankWdw[10:8]		

**Table 178. Hpt\_SetBlankingWindow Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xB9)	1	0	1	1	1	0	0	1

**Table 179. 0xBA—Hpt\_SetZCC**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0xBA)	1	0	1	1	1	0	1	0
APDataOut0	—	—	—	—	—	—	ZccSlowEn	FiltrCntrEn

**Table 180. Hpt\_SetZCC Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0xBA)	1	0	1	1	1	0	1	0



## Power and Reset Commands

Table 181. 0x80—PowerOff\_Command

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x80)	1	0	0	0	0	0	0	0
APDataOut0	PwrOffCmd[7:0]							
PwrOffCmd [7:0]	Power-Off Command Writing 0xB2 to this register will immediately place the part in the OFF state. All other codes = Do nothing							

Table 182. PowerOff\_Command Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x80)	1	0	0	0	0	0	0	0
APDataIn0	—	—	—	—	—	—	—	PwrOffResponse
PwrOffResponse	Power-Off Response 0 = Password good, preparing Off mode 1 = Password is wrong							

Table 183. 0x81 – SoftReset\_Command

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x81)	1	0	0	0	0	0	0	1
APDataOut0	SoftResetCmd[7:0]							
SoftReset Cmd [7:0]	Soft-Reset Command Writing 0xB3 to this register will force a Soft-Reset, all registers will be reset to their default values and the RST line will be asserted. All other codes = Do nothing							

Table 184. SoftReset\_Command Response

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x81)	1	0	0	0	0	0	0	1
APDataIn0	—	—	—	—	—	—	—	SoftResetResponse
SoftReset Response	Soft-Reset Response 0 = Password good, preparing Soft-Reset 1 = Password is wrong							

**Table 185. 0x82—Hard-Reset\_Command**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x82)	1	0	0	0	0	0	1	0
APDataOut0	HardResetCmd [7:0]							
HardReset Cmd[7:0]	Hard-Reset Command Writing 0xB4 to this register will force the system to perform a Hard-Reset. All supplies will turn Off and system will perform a full power-on sequence. All other codes = Do nothing							

**Table 186. Hard-Reset\_Command Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x82)	1	0	0	0	0	0	1	0
APDataIn0	—	—	—	—	—	—	—	HardReset Response
HardReset Response	Hard-Reset Response 0 = Password good, preparing Hard-Reset 1 = Password is wrong							

**Table 187. 0x83—StayOn\_Command**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x83)	1	0	0	0	0	0	1	1
APDataOut0	—	—	—	—	—	—	—	StayOn
StayOn	Stay On This bit must be set within 5s of power-on to prevent the part from shutting down and returning to the power-off condition. This bit has no effect after being set. 0 = Shut down 5s after $\overline{\text{RST}}$ goes HIGH 1 = Stay on							

**Table 188. 0x83—StayOn\_Command Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x83)	1	0	0	0	0	0	1	1

**Table 189. 0x84—PowerOff\_Command\_Delay**

MODE	Write							
BIT	B7	B6	B5	B4	B3	B2	B1	B0
APCmdOut (0x84)	1	0	0	0	0	1	0	0
APDataOut0	PwrOffDlyCmd[7:0]							
PwrOffDly Cmd [7:0]	Power-Off Command with Delay Writing 0xB2 to this register will place the part in the Off state after a 30ms delay. All other codes = Do nothing							

**Table 190. PowerOff\_Command\_Delay Response**

BIT	B7	B6	B5	B4	B3	B2	B1	B0
APResponse (0x84)	1	0	0	0	0	1	0	0
APDataIn0	—	—	—	—	—	—	—	PwrOffDly Response
PwrOffDly Response	Power-Off with Delay Response 0 = Password good, preparing Off mode 1 = Password is wrong							

## Fuel Gauge I<sup>2</sup>C Registers

### Register Summary

All registers must be written and read as 16-bit words; 8-bit writes cause no effect. Any bits marked X (don't care) or read only must be written with the rest of the register, but the value written is ignored by the IC. The values read from don't care bits are undefined. Calculate the register's value by multiplying the 16-bit word by the register's LSb value, as shown in [Table 191](#).

#### VCELL Register (0x02)

The MAX20303 measures VCELL between the V<sub>DD</sub> and GND pins. VCELL is the average of four ADC conversions. The value updates every 250ms in active mode and every 45s in hibernate mode.

#### SOC Register (0x04)

The ICs calculate SOC using the ModelGauge algorithm. This register automatically adapts to variation in battery size since ModelGauge naturally recognizes relative SOC.

The upper byte least-significant bit has units of 1%. The lower byte provides additional resolution.

The first update is available approximately 1s after POR of the IC. Subsequent updates occur at variable intervals depending on application conditions.

#### MODE Register (0x06)

The MODE register allows the system processor to send special commands to the IC (see [Figure 16](#)).

- **Quick-Start** generates a first estimate of OCV and SOC based on the immediate cell voltage. Use with caution; see the [Quick-Start](#) section.
- **EnSleep** enables sleep mode. See the [Sleep Mode](#) section.
- **HibStat** indicates when the IC is in hibernate mode (read only).

#### VERSION Register (0x08)

The value of this read-only register indicates the production version of the IC.

**Table 191. Register Summary**

ADDRESS	REGISTER NAME	16-BIT LSb	DESCRIPTION	READ/WRITE	DEFAULT
0x02	VCELL	78.125μV/cell	ADC measurement of VCELL.	R	—
0x04	SOC	1%/256	Battery state of charge.	R	—
0x06	MODE	—	Initiates quick-start, reports hibernate mode, and enables sleep mode.	W	0x0000
0x08	VERSION	—	IC production version.	R	0x001_
0x0A	HIBRT	—	Controls thresholds for entering and exiting hibernate mode.	R/W	0x8030
0x0C	CONFIG	—	Compensation to optimize performance, sleep mode, alert indicators, and configuration.	R/W	0x971C
0x14	VALRT	—	Configures the VCELL range outside of which alerts are generated.	R/W	0x00FF
0x16	CRATE	0.208%/hr	Approximate charge or discharge rate of the battery.	R	—
0x18	VRESET/ID	—	Configures VCELL threshold below which the IC resets itself, ID is a one-time factory-programmable identifier.	R/W	0x96__
0x1A	STATUS	—	Indicates overvoltage, undervoltage, SOC change, SOC low, and reset alerts.	R/W	0x01__
0x40 to 0x7F	TABLE	—	Configures battery parameters.	W	—
0xFE	CMD	—	Sends POR command.	R/W	0xFFFF

**HIBRT Register (0x0A)**

To disable hibernate mode, set HIBRT = 0x0000. To always use hibernate mode, set HIBRT = 0xFFFF (see Figure 17).

- **ActThr** (active threshold): If at any ADC sample |OCV-CELL| is greater than ActThr, the IC exits hibernate mode. 1 LSb = 1.25mV.
- **HibThr** (hibernate threshold). If the absolute value of CRATE is less than HibThr for longer than 6min, the IC enters hibernate mode. 1 LSb = 0.208%/hr.

**CONFIG Register (0x0C)**

See Figure 18

- **RCOMP** is an 8-bit value that can be adjusted to optimize IC performance for different lithium chemistries or different operating temperatures. Contact Maxim for instructions for optimization. The POR value of RCOMP is 0x97.
- **SLEEP** forces the IC in or out of sleep mode if Mode.EnSleep is set. Writing 1 forces the IC to enter

sleep mode, and 0 forces the IC to exit. The POR value of SLEEP is 0.

- **ALSC** (SOC change alert) enables alerting when SOC changes by at least 1%. Each alert remains until STATUS.SC is cleared, after which the alert automatically clears until SOC again changes by 1%. Do not use this alert to accumulate changes in SOC.
- **ALRT** (alert status bit) is set by the IC when an alert occurs. When this bit is set, the  $\overline{\text{ALRT}}$  pin asserts low. Clear this bit to service and deassert the  $\overline{\text{ALRT}}$  pin. The power-up default value for ALRT is 0. The STATUS register specifies why the  $\overline{\text{ALRT}}$  pin was asserted.
- **ATHD** (empty alert threshold) sets the SOC threshold, where an interrupt is generated on the  $\overline{\text{ALRT}}$  pin and can be programmed from 1% up to 32%. The value is (32 - ATHD)% (e.g., 00000b → 32%, 00001b → 31%, 00010b → 30%, 11111b → 1%). The POR value of ATHD is 0x1C, or 4%. The alert only occurs on a falling edge past this threshold.

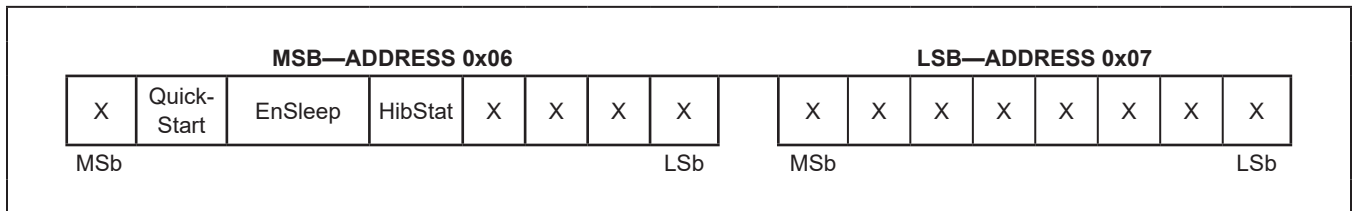


Figure 16. MODE Register Format

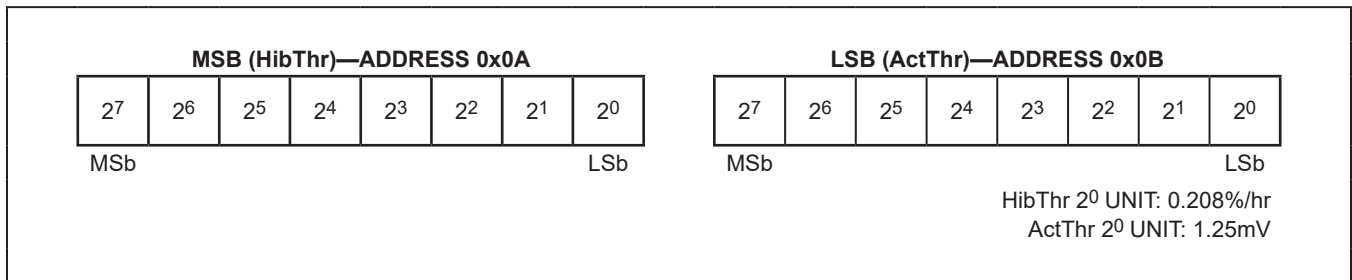


Figure 17. HIBRT Register Format

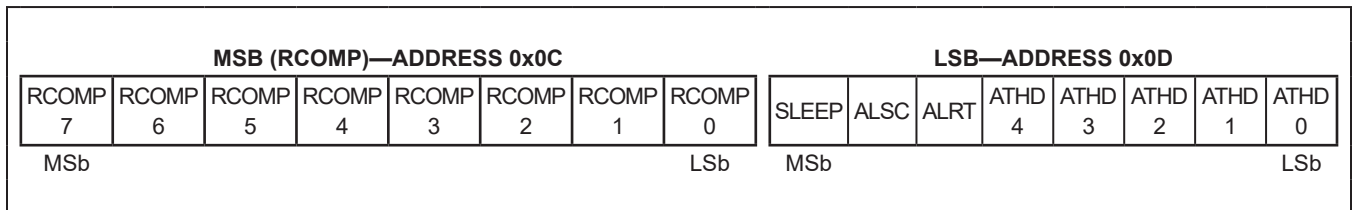


Figure 18. CONFIG Register Format

**VALRT Register (0x14)**

This register is divided into two thresholds: Voltage alert maximum (VALRT.MAX) and minimum (VALRT.MIN). Both registers have 1 LSb = 20mV. The IC alerts while VCELL > VALRT.MAX or VCELL < VALRT.MIN (see Figure 19).

**CRATE Register (0x16)**

The IC calculates an approximate value for the average SOC rate of change. 1 LSb = 0.208% per hour (not for conversion to ampere).

**VRESET/ID Register (0x18)**

See Figure 20.

- **ID** is an 8-bit read-only value that is one-time programmable at the factory, which can be used as an

identifier to distinguish multiple cell types in production. Writes to these bits are ignored.

- **VRESET[7:1]** adjusts a fast analog comparator and a slower digital ADC threshold to detect battery removal and reinsertion. For captive batteries, set to 2.5V. For removable batteries, set to at least 300mV below the application’s empty voltage, according to the desired reset threshold for your application. If the comparator is enabled, the IC resets 1ms after VCELL rises above the threshold. Otherwise, the IC resets 250ms after the VCELL register rises above the threshold.
- **Dis.** Set Dis = 1 to disable the analog comparator in hibernate mode to save approximately 0.5µA

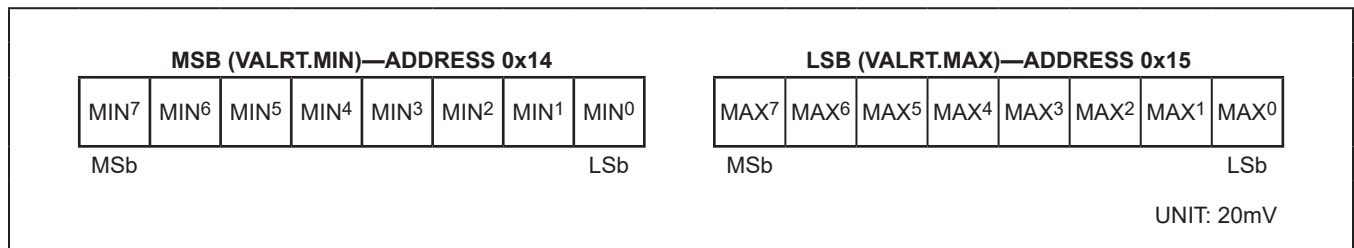


Figure 19. VALRT Register Format

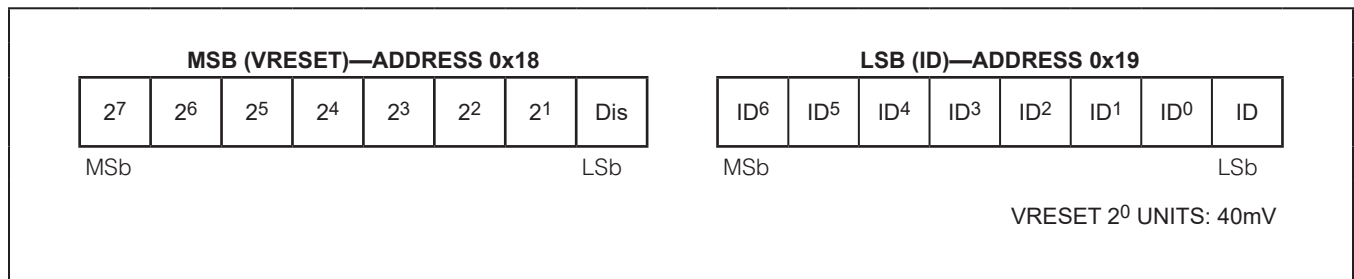


Figure 20. VRESET/ID Register Format

**STATUS Register (0x1A)**

An alert can indicate many different conditions. The STATUS register identifies which alert condition was met. Clear the corresponding bit after servicing the alert (see [Figure 21](#)).

**Reset Indicator:**

- **RI** (reset indicator) is set when the device powers up. Any time this bit is set, the IC is not configured, so the model should be loaded and the bit should be cleared.

**Alert Descriptors:**

These bits are set only when they cause an alert (e.g., if CONFIG.ALSC = 0, then SC is never set).

- **VH** (voltage high) is set when VCELL has been above ALRT.VALRTMAX.
- **VL** (voltage low) is set when VCELL has been below ALRT.VALRTMIN.
- **VR** (voltage reset) is set after the device has been reset regardless of EnVr.
- **HD** (SOC low) is set when SOC crosses the value in CONFIG.ATHD.
- **SC** (1% SOC change) is set when SOC changes by at least 1% if CONFIG.ALSC is set.

**Enable or Disable VRESET Alert:**

- **EnVr** (enable voltage reset alert) when set to 1 asserts the  $\overline{\text{ALRT}}$  pin when a voltage-reset event occurs under the conditions described by the VRESET/ ID register.

**TABLE Registers (0x40 to 0x7F)**

Contact Maxim for details on how to configure these registers. The default value is appropriate for some Li+ batteries.

To unlock the TABLE registers, write 0x57 to address 0x3F, and 0x4A to address 0x3E. While TABLE is unlocked, no ModelGauge registers are updated, so reload as soon as possible by writing 0x00 to address 0x3F, and 0x00 to address 0x3E.

**CMD Register (0xFE)**

Writing a value of 0x5400 to this register causes the device to completely reset as if power had been removed (see the *Power-On Reset (POR)* section). The reset occurs when the last bit has been clocked in. The IC does not respond with an I<sup>2</sup>C ACK after this command sequence.

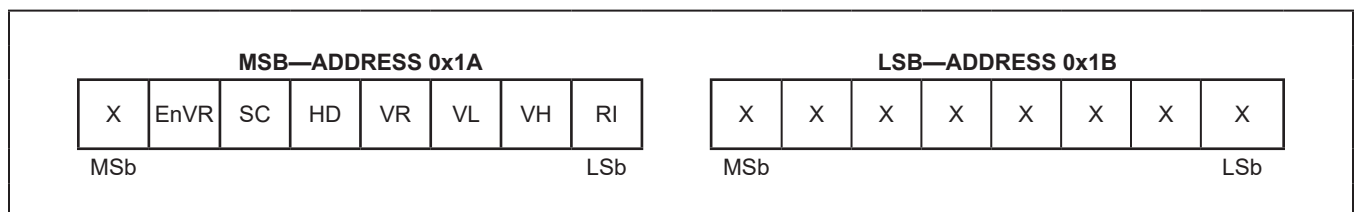


Figure 21. STATUS Register Format

Table 192. Register Bit Default Values

REGISTER BITS	DEFAULT VALUE									
	MAX20303A	MAX20303B	MAX20303C	MAX20303D	MAX20303E	MAX20303G	MAX20303H			
PFN2PUD_CFG*	PU/PD Connected	Hi-Z	PU/PD Connected	Hi-Z	Hi-Z	Hi-Z	Hi-Z			
PFN1PUD_CFG*	Hi-Z	PU/PD Connected	Hi-Z	PU/PD Connected	PU/PD Connected	PU/PD Connected	PU/PD Connected			
WriteProtect	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled			
ILimBlank	10ms	10ms	10ms	10ms	10ms	Disabled	Disabled			
ILimCntrl	500mA	1000mA	500mA	1000mA	200mA	500mA	500mA			
MtChgTmr	15min	15min	15min	15min	0min	0min	0min			
FChgTmr	150min	150min	150min	150min	150min	600min	600min			
PChgTmr	30min	30min	30min	30min	60min	30min	30min			
TShdnTmo	5s	5s	5s	5s	5s	5s	5s			
ChgAutoRe	Disabled	Disabled	Disabled	Disabled	Auto-Restart	Auto-Restart	Auto-Restart			
VPChg	2.7V	3V	2.7V	2.7V	3V	3.15V	3.15V			
IPChg	5% IFCHG	5% IFCHG	5% IFCHG	5% IFCHG	10% IFCHG	10% IFCHG	10% IFCHG			
ChgDone	10% IFCHG	10% IFCHG	10% IFCHG	10% IFCHG	5% IFCHG	10% IFCHG	10% IFCHG			
ChgEn	Enabled	Enabled	Enabled	Enabled	Enabled	Disabled	Disabled			
ChgAutoStp	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled			
BatReChg	200mV	200mV	200mV	200mV	100mV	200mV	200mV			
BatReg	4.20V	4.20V	4.20V	4.20V	4.20V	4.35V	4.35V			
ColdLim	1397.65mV	1397.65mV	1397.65mV	1397.65mV	1327.06mV	1397.65mV	1397.65mV			
HotLim	529.41mV	529.41mV	529.41mV	529.41mV	416.47mV	529.41mV	529.41mV			
Bst1Set	325mA	100mA	325mA	100mA	275mA	425mA	425mA			
Bst1AdptEn	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled			
BstFastSirt	100ms	100ms	100ms	100ms	100ms	50ms	50ms			
BstFetScale	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled			
BstIVSet	12V	13V	12V	13V	13V	20V	20V			
Buck1FetScale	Enabled	Disabled	Enabled	Disabled	Disabled	Disabled	Disabled			
Buck2FetScale	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled			
BstSeq	BstEn After 100%	BstEn After 100%	Disabled	Disabled	BstEn After 100%	BstEn After 100%	Disabled			
BstEn	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled			
Buck1VSet	1.2V	1.2V	1.2V	1.2V	1.8V	1.8V	1.8V			
Buck1IZCSet	20mA	20mA	20mA	20mA	30mA	30mA	30mA			
Buck2VSet	1.8V	1.8V	1.8V	1.8V	0.95V	0.9V	0.9V			
Buck2IZCSet	30mA	30mA	30mA	30mA	10mA	10mA	10mA			



Table 192. Register Bit Default Values (continued)

REGISTER BITS	DEFAULT VALUE							
	MAX20303A	MAX20303B	MAX20303C	MAX20303D	MAX20303E	MAX20303G	MAX20303H	
Buck2Iset	150mA	150mA	150mA	150mA	150mA	150mA	150mA	
Buck1Iset	50mA	150mA	50mA	150mA	150mA	150mA	150mA	
BootDly**	80ms	80ms	80ms	80ms	80ms	120ms	120ms	
Buck2SftSirt	50ms Soft-Start	50ms Soft-Start	50ms Soft-Start	50ms Soft-Start	25ms Soft-Start	50ms Soft-Start	50ms Soft-Start	
Buck1SftSirt	50ms Soft-Start	50ms Soft-Start	50ms Soft-Start	50ms Soft-Start	25ms Soft-Start	50ms Soft-Start	50ms Soft-Start	
Buck2En	Enabled	Enabled	Enabled	Enabled	Disabled	Disabled	Disabled	
Buck1En	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	
LDO1Md	LDO	LDO	LDO	LDO	Load Switch	LDO	LDO	
LDO1En	Enabled	Disabled	Enabled	Disabled	Disabled	Disabled	Disabled	
LDO2Md	LDO	LDO	LDO	LDO	Load Switch	LDO	LDO	
LDO2En	Enabled	Disabled	Enabled	Disabled	Disabled	Disabled	Disabled	
PassDiscEna***	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	
LDO2VSet	3.0V	3.2V	3.0V	3.2V	1.8V	3.2V	3.2V	
StayOn	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	
SFOUVSet	3.3V	3.3V	3.3V	3.3V	5.0V	3.3V	3.3V	
LDO1VSet	1.2V	1.1V	1.2V	1.1V	1.8V	1.2V	1.2V	
SysMinVlt	4.0V	4.0V	4.0V	4.0V	3.6V	3.6V	3.6V	
SFOUEN	CHGIN	CHGIN	CHGIN	CHGIN	Disabled	CHGIN	CHGIN	
CPVSet	5.0V	5.0V	5.0V	5.0V	5.0V	6.6V	6.6V	
CPEn	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	
CPSeq	CPEn After 100%	CPEn After 100%	CPEn After 100%	CPEn After 100%	CPEn After 100%	CPEn After 100%	Disabled	
PwrRstCfg	0b0100	0b0110	0b0100	0b0110	0b0111	0b0111	0b0111	
Buck2Seq	50%	Buck2En After 100%	50%	Buck2En After 100%	Buck2En After 100%	Buck2En After 100%	Buck2En After 100%	
Buck1Seq	50%	Buck1En After 100%	50%	Buck1En After 100%	0%	Buck1En After 100%	Buck1En After 100%	
BBsEn	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	
LDO2Seq	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%	LDO2En After 100%	
LDO1Seq	LDO1En After 100%	LDO1En After 100%	LDO1En After 100%	LDO1En After 100%	LDO1En After 100%	LDO1En After 100%	LDO1En After 100%	
ThmEn	Enabled	Enabled	Enabled	Enabled	Enabled	Disabled	Disabled	

**Table 192. Register Bit Default Values (continued)**

REGISTER BITS	DEFAULT VALUE							
	MAX20303A	MAX20303B	MAX20303C	MAX20303D	MAX20303E	MAX20303G	MAX20303H	
BBstVset	5V	5V	5V	5V	3V	5V	5V	
BBstIset	250mA	150mA	250mA	150mA	100mA	100mA	100mA	
BatOcThr	1000mA	1000mA	1000mA	1000mA	200mA	1000mA	1000mA	
BBstRipRed	Lower Ripple	Lower Ripple	Lower Ripple	Lower Ripple	Lower Ripple	Lower Ripple	Lower Ripple	
BBstIInd	4.7µH	4.7µH	4.7µH	4.7µH	4.7µH	4.7µH	4.7µH	
BBstSeq	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%	BBstEn After 100%	
EmfEn	Enabled	Enabled	Enabled	Enabled	Enabled	Disabled	Disabled	
HptSel	LRA	LRA	LRA	LRA	ERM	ERM	ERM	
AlcMod	Enabled	Enabled	Enabled	Enabled	Disabled	Enabled	Enabled	
HptSysUVLO	3.3V	3.28V	3.3V	3.28V	3V	3V	3V	
HptDrvTmo	5s	Disabled	5s	Disabled	Disabled	10s	10s	
ILimMax****	1000mA	1000mA	1000mA	1000mA	450mA	1000mA	1000mA	
TCHGIN_SHDN	120°C	120°C	120°C	120°C	100°C	100°C	100°C	

\*See Table 193

\*\*Sets t<sub>RST</sub> time. See Figure 3

\*\*\*If enabled, passive discharge is enabled for all rails in off mode.

\*\*\*\*Current limit during t<sub>ILimBlank</sub>

**Table 193. Register Bit Default Values**

FUNCTION	DEVICE CONFIGURATION							
	MAX20303A	MAX20303B	MAX20303C	MAX20303D	MAX20303E	MAX20303G	MAX20303H	
PFN1	Hi-Z	Pullup	Hi-Z	Pullup	Pullup	Pullup	Pullup	
PFN2	Pulldown	Hi-Z	Pulldown	Hi-Z	Hi-Z	Hi-Z	Hi-Z	
ON STATE LOGIC LEVELS*	V <sub>IO_IH</sub> , V <sub>IO_IL</sub>	V <sub>PFN_IH</sub> , V <sub>PFN_IL</sub>	V <sub>IO_IH</sub> , V <sub>IO_IL</sub>	V <sub>PFN_IH</sub> , V <sub>PFN_IL</sub>	V <sub>PFN_IH</sub> , V <sub>PFN_IL</sub>	V <sub>PFN_IH</sub> , V <sub>PFN_IL</sub>	V <sub>PFN_IH</sub> , V <sub>PFN_IL</sub>	

\*Values in this row reference [Electrical Characteristics](#) table parameters. In OFF mode, V<sub>PFN\_IH</sub> and V<sub>PFN\_IL</sub> logic levels always apply.

Table 194. I2C Direct Register Default Values

REGISTER	NAME	DEFAULT VALUE										
		MAX20303A	MAX20303B	MAX20303C	MAX20303D	MAX20303E	MAX20303G	MAX20303H				
0x00	HardwareID	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02
0x01	FirmwareID	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02
0x0B	SystemError	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0C	IntMask0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0D	IntMask1	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0E	IntMask2	0x40	0x40	0x40	0x40	0x40	0x40	0x40	0x40	0x40	0x40	0x40
0x0F	APDataOut0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x10	APDataOut1	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x11	APDataOut2	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x12	APDataOut3	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x13	APDataOut4	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x14	APDataOut5	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x15	APDataOut6	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x17	APCmdOut	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x18	APResponse	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x19	APDataIn0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x1A	APDataIn1	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x1B	APDataIn2	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x1C	APDataIn3	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x1D	APDataIn4	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x1E	APDataIn5	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x20	LDODirect	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x21	MPCDirectWrite	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x28	HptRAMAddr	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x29	HptRAMDataH	0x4A	0x4A	0x4A	0x4A	0x4A	0x4A	0x4A	0x4A	0x4A	0x4A	0x4A
0x2A	HptRAMDataM	0x74	0x74	0x74	0x74	0x74	0x74	0x74	0x74	0x74	0x74	0x74
0x2B	HptRAMDataL	0x63	0x63	0x63	0x63	0x63	0x63	0x63	0x63	0x63	0x63	0x63
0x2C	LEDStepDirect	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x2D	LED0Direct	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x2E	LED1Direct	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x2F	LED2Direct	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x30	HptDirect0	0x04	0x04	0x04	0x04	0x04	0x04	0x04	0x04	0x04	0x04	0x04
0x31	HptDirect1	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x32	HptRTI2Camp	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x33	HptPatRAMAddr	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00

Table 195. Read Opcode Default Values

OPCODE	REGISTER	DEFAULT VALUE							
		MAX20303A	MAX20303B	MAX20303C	MAX20303D	MAX20303E	MAX20303G	MAX20303H	
GPIO_Config_Read (0x02)	APDataIn0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn1	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn2	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn3	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
GPIO_Control_Read (0x04)	APDataIn4	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn1	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn2	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
MPC_Config_Read (0x07)	APDataIn3	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn4	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn0	0x1E	0x1F	0x1E	0x1F	0x1B	0x06	0x06	0x06
	APDataIn1	0x03	0x03	0x03	0x03	0x03	0x03	0x03	0x03
ThermalShutdown_Config_Read (0x12)	APDataIn0	0x14	0x14	0x14	0x14	0x05	0x0C	0x0C	0x0C
	APDataIn1	0x41	0x61	0x41	0x41	0x64	0x75	0x75	0x75
	APDataIn2	0xB3	0xB3	0xB3	0xB3	0xD3	0xF6	0xF6	0xF6
	APDataIn3	0x04	0x04	0x04	0x04	0x00	0x00	0x00	0x00
ChargerThermalLimits_Config_Read (0x17)	APDataIn0	0xC6	0xC6	0xC6	0xC6	0xBC	0xC6	0xC6	0xC6
	APDataIn1	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn2	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn3	0x4B	0x4B	0x4B	0x4B	0x3B	0x4B	0x4B	0x4B
ChargerThermalReg_ConfigRead (0x19)	APDataIn0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn1	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn2	0x1F	0x1F	0x1F	0x1F	0x1F	0x1F	0x1F	0x1F
	APDataIn3	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
Charger_Control_Read (0x1B)	APDataIn4	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn0	0x03	0x03	0x03	0x03	0x03	0x03	0x03	0x03
Charger_JEITA Hyst_ControlRead (0x1D)	APDataIn0	0x06	0x06	0x06	0x06	0x86	0x86	0x86	0x86
	APDataIn1	0x06	0x06	0x06	0x06	0x86	0x86	0x86	0x86

Table 195. Read Opcode Default Values (continued)

OPCODE	REGISTER	DEFAULT VALUE							
		MAX20303A	MAX20303B	MAX20303C	MAX20303D	MAX20303E	MAX20303G	MAX20303H	
Bst_Config_Read (0x31)	APDataIn0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn1	0x04	0x04	0x04	0x04	0x04	0x06	0x06	0x06
	APDataIn2	0x09	0x00	0x09	0x00	0x07	0x0D	0x0D	0x0D
	APDataIn3	0x1C	0x20	0x1C	0x20	0x20	0x3C	0x3C	0x3C
Buck1_Config_Read (0x36)	APDataIn4	0x07	0x07	0x00	0x00	0x07	0x00	0x00	0x00
	APDataIn0	0x02	0x00	0x02	0x00	0x20	0x00	0x00	0x00
	APDataIn1	0x90	0x90	0x90	0x90	0xA8	0xA8	0xA8	0xA8
	APDataIn2	0x12	0x16	0x12	0x16	0x26	0x26	0x26	0x26
Buck2_Config_Read (0x3B)	APDataIn3	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01
	APDataIn4	0x04	0x07	0x04	0x07	0x02	0x07	0x07	0x07
	APDataIn0	0x00	0x00	0x00	0x00	0x20	0x00	0x00	0x00
	APDataIn1	0x94	0x94	0x94	0x94	0x83	0x82	0x82	0x82
LDO1_Config_Read (0x41)	APDataIn2	0x26	0x26	0x26	0x26	0x06	0x06	0x06	0x06
	APDataIn3	0x01	0x01	0x01	0x01	0x00	0x00	0x00	0x00
	APDataIn4	0x04	0x07	0x04	0x07	0x07	0x07	0x07	0x07
	APDataIn0	0x01	0x00	0x01	0x00	0x04	0x00	0x00	0x00
LDO2_Config_Read (0x43)	APDataIn1	0x1C	0x18	0x1C	0x18	0x34	0x1C	0x1C	0x1C
	APDataIn2	0x07	0x07	0x07	0x07	0x07	0x07	0x07	0x07
	APDataIn0	0x01	0x00	0x01	0x00	0x04	0x00	0x00	0x00
	APDataIn1	0x15	0x17	0x15	0x17	0x09	0x17	0x17	0x17
ChargePump_Config_Read (0x47)	APDataIn2	0x07	0x07	0x07	0x07	0x07	0x07	0x07	0x07
	APDataIn0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn1	0x01	0x01	0x01	0x01	0x01	0x00	0x00	0x00
	APDataIn2	0x07	0x07	0x07	0x07	0x07	0x07	0x07	0x07
SFOUT_Config_Read (0x49)	APDataIn0	0x05	0x05	0x05	0x05	0x00	0x05	0x05	0x05
MONMux_Config_Read (0x51)	APDataIn0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn0	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
	APDataIn1	0x05	0x03	0x05	0x03	0x02	0x02	0x02	0x02
	APDataIn2	0x19	0x19	0x19	0x19	0x05	0x19	0x19	0x19
BBst_Config_Read (0x71)	APDataIn3	0x50	0x50	0x50	0x50	0x50	0x50	0x50	0x50
	APDataIn4	0x07	0x07	0x07	0x07	0x07	0x07	0x07	0x07

Table 195. Read Opcode Default Values (continued)

OPCODE	REGISTER	DEFAULT VALUE									
		MAX20303A	MAX20303B	MAX20303C	MAX20303D	MAX20303E	MAX20303G	MAX20303H			
Hpt_Config_Read0 (0xA1)	APDataIn0	0x0E	0x0E	0x0E	0x0E	0x08	0x02	0x02			
	APDataIn1	0xD0	0xD0	0xD0	0xD0	0xD0	0xD0	0xD0			
	APDataIn2	0x97	0x97	0x97	0x97	0x97	0x97	0x97			
	APDataIn3	0x00	0x00	0x00	0x00	0x00	0x00	0x00			
	APDataIn4	0x05	0x05	0x05	0x05	0x05	0x05	0x05			
Hpt_Config_Read1 (0xA3)	APDataIn5	0x01	0x01	0x01	0x01	0x01	0x01	0x01			
	APDataIn0	0x01	0x01	0x01	0x01	0x01	0x01	0x01			
	APDataIn1	0x00	0x00	0x00	0x00	0x00	0x00	0x00			
	APDataIn2	0x02	0x02	0x02	0x02	0x02	0x02	0x02			
	APDataIn3	0x8B	0x8B	0x8B	0x8B	0x8B	0x8B	0x8B			
Hpt_Config_Read2 (0xA5)	APDataIn4	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F			
	APDataIn5	0x04	0x04	0x04	0x04	0x04	0x04	0x04			
	APDataIn0	0xCC	0xCC	0xCC	0xCC	0xCC	0xCC	0xCC			
	APDataIn1	0x32	0x32	0x32	0x32	0x32	0x32	0x32			
	APDataIn2	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF	0xFF			
Hpt_SYS_Threshold_Config_Read (0xA7)	APDataIn3	0x04	0x04	0x04	0x04	0x04	0x04	0x04			
	APDataIn4	0x24	0x24	0x24	0x24	0x24	0x24	0x24			
	APDataIn5	0x06	0x06	0x06	0x06	0x06	0x06	0x06			
	APDataIn0	0x99	0x98	0x99	0x98	0x8B	0x8B	0x8B			
	APDataIn1	0x00	0x00	0x00	0x00	0x00	0x00	0x00			
Hpt_EMF_Threshold_Config_Read (0xA9)	APDataIn0	0x19	0x19	0x19	0x19	0x19	0x19	0x19			
	APDataIn1	0x00	0x00	0x00	0x00	0x00	0x00	0x00			

## Ordering Information

PART*	TEMP RANGE	PIN-PACKAGE
MAX20303AEWN+	-40°C to +85°C	56 WLP
MAX20303AEWN+T	-40°C to +85°C	56 WLP
MAX20303BEWN+	-40°C to +85°C	56 WLP
MAX20303BEWN+T	-40°C to +85°C	56 WLP
MAX20303CEWN+	-40°C to +85°C	56 WLP
MAX20303CEWN+T	-40°C to +85°C	56 WLP
MAX20303DEWN+	-40°C to +85°C	56 WLP
MAX20303DEWN+T	-40°C to +85°C	56 WLP
MAX20303EEWN+	-40°C to +85°C	56 WLP
MAX20303EEWN+T	-40°C to +85°C	56 WLP
MAX20303GEWN+	-40°C to +85°C	56 WLP
MAX20303GEWN+T	-40°C to +85°C	56 WLP
MAX20303HEWN+*	-40°C to +85°C	56 WLP
MAX20303HEWN+T*	-40°C to +85°C	56 WLP

+Denotes a lead (Pb)-free package/RoHS-compliant package.

T = Tape and reel

\*Future product—contact factory for availability.

## Chip Information

PROCESS: BiCMOS

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/16	Initial release	—
1	1/17	Removed future product status from MAX20303A and made various other changes to register maps	19, 24, 45–49, 51, 60–62, 68–71, 73, 75, 77, 82, 103–105, 125–127, 131, 146
2	3/17	Updated Figure 1e and removed future product status from MAX20303D	49, 146
3	4/17	Removed future product status from MAX20303C part numbers and increased $V_{LIIIN}$ minimum value in <i>Electrical Characteristics</i> table	27, 146
4	5/17	Corrected external CP cap, updated figures, and added Table 193 and Table 194	1, 12, 31, 34, 38, 41, 43, 47, 49, 50, 51, 56, 70, 93, 121, 123, 145, 146–149
5	10/17	Updated Benefits and Features section, Timer Suspend Threshold typ in the <i>Electrical Characteristics</i> table, Driver Amplitude section, Table 63, Table 131, and Table 135. Corrected typos in Table 44 and Table 127. Added a new Table 193, and renumbered Tables 194–195. Replaced Table 192.	1, 19, 57, 86, 94, 124–125, 126, 128, 144–151
6	10/17	Updated Direct Access I <sup>2</sup> C Register Map table, and removed future part designation from MAX20303GEWN+ and MAX20303GEWN+T in the <i>Ordering Information</i> table.	68–69, 151

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

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