

# TPS50602-SP Radiation Hardened 3-V to 7-V Input, 12-A Single, 6-A Dual Output Synchronous Buck Converter

## 1 Features

- 5962R18207:
  - Radiation Hardened up to TID 100 krad(Si)
  - Single Event Latchup (SEL), Single Event Burnout (SEB), and Single Event Gate Rupture (SEGR) Immune to LET = 75 MeV-cm<sup>2</sup>/mg
  - SET/SEFI Cross-Section Plot Available
- Peak Efficiency: 95% (V<sub>O</sub> = 3.3 V)
- Integrated 48-mΩ/37-mΩ MOSFETs (PVIN = 5 V)
- Power Rail: 3 to 7 V on VIN
- 12-A Maximum Output Current in Single Output Configuration and 6-A Maximum Output Current in Dual Output Configuration
- Fixed 500-kHz Switching Frequency Using Internal Oscillator or External Clock Between 100 kHz to 1 MHz at 180° Out of Phase
- 0.804-V ±1.5% Voltage Reference over Temperature, Radiation Tolerance and Line and Load Regulation
- Monotonic Start-Up into Pre-biased Outputs
- Adjustable Soft Start Through External Capacitor
- Input Enable and Power-Good Output for Power Sequencing
- Power Good Output Monitor for Undervoltage and Overvoltage
- Adjustable Input Undervoltage Lockout (UVLO)
- 64-Pin Thermally-Enhanced Ceramic Quad Flatpack Package (HFG)
- Engineering Evaluation (/EM) Samples are Available<sup>(1)</sup>

## 2 Applications

- Space Satellite Point of Load Supply for FPGAs, Microcontrollers, Data Converters and ASICs
- Space Satellite Payloads
- Radiation Hardened and Tolerant Point of Load Applications
- Available in Military (–55°C to 125°C) Temperature Range

## 3 Description

The TPS50602-SP is a dual TPS50601A-SP die, TID and SEE radiation hardened, 7-V, 12-A single output or 6-A dual output synchronous step-down converter, which is optimized for ultra small form factor designs. This is achieved integrating highly efficiency high-side and low-side MOSFETs and excellent thermal performance. Further space savings are achieved through the dual output configuration, which reduces the overall solution size if multiple 6-A rails are needed. The output voltage startup ramp is controlled by the SS/TR pin which allows operation as either a stand alone power supply or in tracking applications. Power sequencing is also possible by correctly configuring the enable and the open drain power good pins. Thermal shutdown disables the part when die temperature exceeds thermal shutdown temperature.

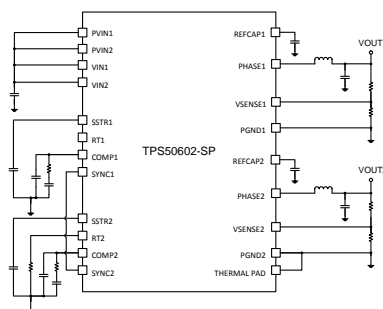
### Device Information<sup>(2)</sup>

| PART NUMBER     | GRADE                                 | PACKAGE  |
|-----------------|---------------------------------------|----------|
| 5962R1820701VXC | RHA – 100 krad(Si)                    | HFG (64) |
| TPS50602HFG/EM  | Engineering Evaluation <sup>(1)</sup> |          |

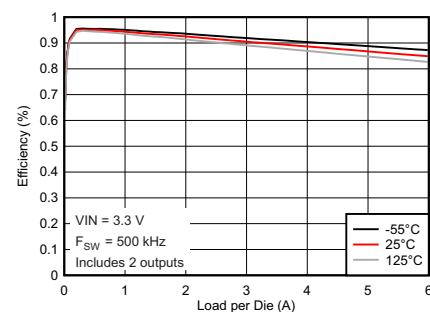
(1) These units are intended for engineering evaluation only. They are processed to a noncompliant flow. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to 125°C or operating life.

(2) For all available packages, see the orderable addendum at the end of the data sheet.

### Dual Output Configuration



### Efficiency at VIN = PVIN = 3.3 V



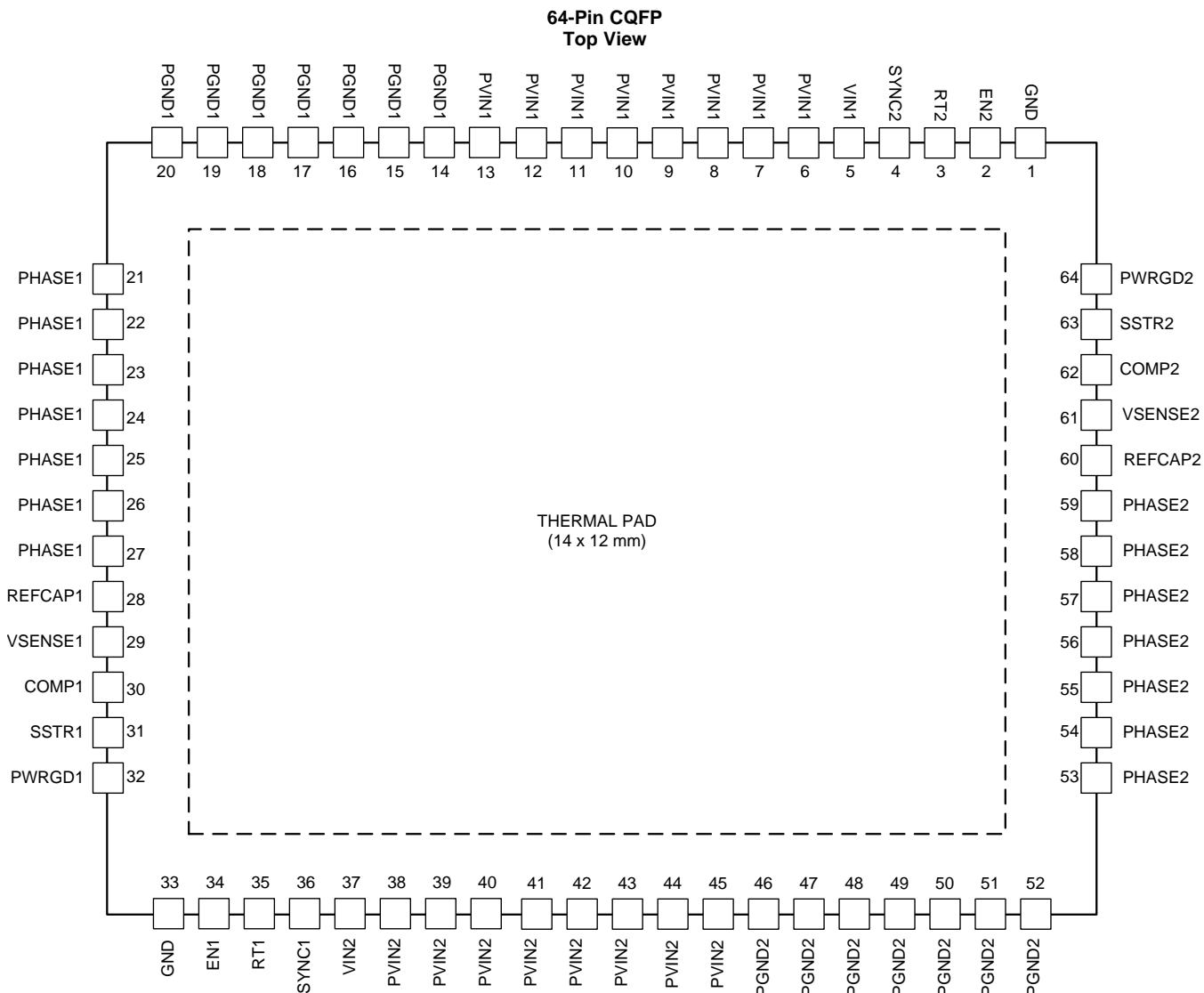
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## 4 Revision History

| DATE         | REVISION | NOTES            |
|--------------|----------|------------------|
| October 2018 | *        | Initial release. |

## 5 Pin Configuration and Functions



**ADVANCE INFORMATION**

### Pin Functions

| PIN                        |       | I/O | DESCRIPTION   |
|----------------------------|-------|-----|---|
| NO.                        | NAME  |     |   |
| 1, 33                      | GND   | —   | Return for control circuitry/thermal pad <sup>(1)</sup> .   |
| 2                          | EN2   | I   | Enable pin for die 2. This pin has an internal pullup so if left floating, the device is still enabled. Adjust the input undervoltage lockout (UVLO) with two resistors.                      |
| 3                          | RT2   | I/O | In internal oscillation mode, a resistor is connected between the RT pin and GND to set the switching frequency for die 2. A resistor corresponding to 500 kHz must be connected to this pin. |
| 4                          | SYNC2 | I/O | External system clock input for die 2. The clock from SYNC1 is connected to this pin to run at 500 kHz.   |
| 5                          | VIN1  | I   | Supplies the power to the controller for die 1.   |
| 6, 7, 8, 9, 10, 11, 12, 13 | PVIN1 | I   | Power input for die 1.  |
| 14, 15, 16, 17, 18, 19, 20 | PGND1 | —   | Return for low-side power MOSFET for die 1.   |

(1) Thermal pad and package lid are internally connected to GND.

**Pin Functions (continued)**

| PIN                                  |         | I/O | DESCRIPTION   |
|--------------------------------------|---------|-----|---|
| NO.                                  | NAME    |     |   |
| 21, 22, 23,<br>24, 25, 26,<br>27     | PHASE1  | O   | Switch node for die 1.  |
| 28                                   | REFCAP1 | O   | Capacitor for internal reference. A 470 nF is recommended to be connected between REFCAP1 pin and GND.  |
| 29                                   | VSENSE1 | I   | Inverting input of the gm error amplifier for die 1.  |
| 30                                   | COMP1   | I/O | Error amplifier output and input to the output switch current comparator. Connect frequency compensation to this pin.   |
| 31                                   | SSTR1   | I/O | Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing. |
| 32                                   | PWRGD1  | O   | Power Good fault pin is an open-drain connection. Power Good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage, or EN shutdown, or during slow start.                         |
| 34                                   | EN1     | I   | Enable pin for die 1. This pin has an internal pullup so if left floating, the device is still enabled. Adjust the input undervoltage lockout (UVLO) with two resistors.  |
| 35                                   | RT1     | I/O | Resistor to set switching frequency. RT1 should be left floating to generate an output clock at the SYNC1 pin.  |
| 36                                   | SYNC1   | I/O | External system clock input for die 1. This pin outputs a 500 kHz clock signal at 180° out of phase from the internal clock from die 1. This clock is used to drive SYNC2.  |
| 37                                   | VIN2    | I   | Supplies the power to the controller for die 2.   |
| 38, 39, 40,<br>41, 42, 43,<br>44, 45 | PVIN2   | I   | Power input for die 2.  |
| 46, 47, 48,<br>49, 50, 51,<br>52     | PGND2   | —   | Return for low-side power MOSFET for die 2.   |
| 53, 54, 55,<br>56, 57, 58,<br>59     | PHASE2  | O   | Switch node for die 2.  |
| 60                                   | REFCAP2 | O   | Capacitor for internal reference. A 470 nF is recommended to be connected between REFCAP2 pin and GND.  |
| 61                                   | VSENSE2 | I   | Inverting input of the gm error amplifier for die 2.  |
| 62                                   | COMP2   | I/O | Error amplifier output and input to the output switch current comparator. Connect frequency compensation to this pin.   |
| 63                                   | SSTR2   | I/O | Slow-start and tracking. An external capacitor connected to this pin sets the internal voltage reference rise time. The voltage on this pin overrides the internal reference. It can be used for tracking and sequencing. |
| 64                                   | PWRGD2  | O   | Power Good fault pin is an open-drain connection. Power Good fault pin. Asserts low if output voltage is low due to thermal shutdown, dropout, overvoltage, or EN shutdown, or during slow start.                         |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted)<sup>(1)</sup>

|                                       |                              | MIN           | MAX           | UNIT |   |
|---------------------------------------|------------------------------|---------------|---------------|------|---|
| Input voltage                         | VIN <sup>(2)</sup>           | -0.3          | 7.5           | V    |   |
|                                       | PVIN <sup>(2)</sup>          | -0.3          | 7.5           |      |   |
|                                       | EN                           | -0.3          | 5.5           |      |   |
|                                       | VSENSE                       | -0.3          | 3.3           |      |   |
|                                       | COMP                         | -0.3          | 3.3           |      |   |
|                                       | PWRGD                        | -0.3          | 5.5           |      |   |
|                                       | SS/TR                        | -0.3          | 5.5           |      |   |
|                                       | RT                           | -0.3          | 5.5           |      |   |
|                                       | SYNC                         | -0.3          | 7.5           |      |   |
| Output voltage                        | REFCAP                       | -0.3          | 3.3           | V    |   |
|                                       | PH                           | -1            | 7.5           |      |   |
|                                       | PH 10-ns transient           | -3            | 7.5           |      |   |
| Vdiff                                 | (GND to exposed thermal pad) |               | -0.2          | 0.2  | V |
| Source current                        | PH                           | Current limit | Current limit | A    |   |
|                                       | RT                           |               | ±100          | µA   |   |
| Sink current                          | PH                           | Current limit | Current limit | A    |   |
|                                       | PVIN                         | Current limit | Current limit | A    |   |
|                                       | COMP                         |               | ±200          | µA   |   |
|                                       | PWRGD                        | -0.1          | 5             | mA   |   |
| Operating junction temperature        |                              | -55           | 150           | °C   |   |
| Storage temperature, T <sub>stg</sub> |                              | -65           | 150           | °C   |   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) See derating curve.

### 6.2 ESD Ratings

|                    |                         |  | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±750  | V    |
| V <sub>(ESD)</sub> | Electrostatic discharge | Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | TBD   | V    |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

|                |                                | MIN | NOM | MAX | UNIT |
|----------------|--------------------------------|-----|-----|-----|------|
| T <sub>J</sub> | Junction operating temperature | -55 |     | 125 | °C   |

### 6.4 Thermal Information

| THERMAL METRIC        |  | TPS50602-SP | UNIT |
|-----------------------|--|-------------|------|
|                       |  | HFG (CQFP)  |      |
|                       |  | 64 PINS     |      |
| R <sub>θJC(bot)</sub> | Junction-to-case (bottom) thermal resistance | 0.56        | °C/W |

## 6.5 Electrical Characteristics

 $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{IN} = P_{VIN} = 3.0\text{ V}$  to  $7.0\text{ V}$  (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS   | MIN   | TYP       | MAX   | UNIT             |
|---|---|-------|-----------|-------|------------------|
| <b>SUPPLY VOLTAGE (VIN AND PVIN PINS)</b>                 |   |       |           |       |                  |
| PVIN operating input voltage                              |   | 3.0   |           | 7.0   | V                |
| PVIN internal UVLO threshold                              | PVIN rising   |       | 2.50      |       | V                |
| PVIN internal UVLO hysteresis                             |   |       | 450       |       | mV               |
| VIN operating input voltage                               |   | 3.0   |           | 7.0   | V                |
| VIN internal UVLO threshold                               | VIN rising  |       | 2.75      | 3.0   | V                |
| VIN internal UVLO hysteresis                              |   |       | 150       |       | mV               |
| VIN shutdown supply current                               | $V_{EN} = 0\text{ V}$   |       | 1.35      | 2.5   | mA               |
| VIN operating – non switching supply current              | $V_{SENSE} = V_{BG}$  |       | 5         | 10    | mA               |
| <b>ENABLE AND UVLO (EN PIN)</b>                           |   |       |           |       |                  |
| Enable threshold  | Rising  |       | 1.14      | 1.18  | V                |
|   | Falling   | 1.05  | 1.11      |       |                  |
| Input current   | $V_{EN} = 1.1\text{ V}$   |       | 6.1       |       | $\mu\text{A}$    |
| Hysteresis current  | $V_{EN} = 1.3\text{ V}$   |       | 3.0       |       | $\mu\text{A}$    |
| <b>VOLTAGE REFERENCE</b>                                  |   |       |           |       |                  |
| Voltage reference   | $0\text{ A} \leq I_{out} \leq 6\text{ A}$ , $-55$ to $125^\circ\text{C}$  | 0.792 | 0.804     | 0.816 | V                |
| REFCAP voltage  | 470 nF  |       | 1.211     |       | V                |
| <b>MOSFET</b>   |   |       |           |       |                  |
| High-side switch resistance <sup>(1)</sup>                | PVIN=VIN= 3.0 V, lead length = 4 mm                                       |       | 52        |       | m $\Omega$       |
| High-side switch resistance <sup>(1)</sup>                | PVIN=VIN= 5.0 V, lead length = 4mm  |       | 48        |       | m $\Omega$       |
| High-side switch resistance <sup>(1)</sup>                | PVIN=VIN= 7.0 V, lead length = 4 mm                                       |       | 46        |       | m $\Omega$       |
| Low-side switch resistance <sup>(1)</sup>                 | PVIN=VIN= 3.0 V, lead length = 4 mm                                       |       | 38        |       | m $\Omega$       |
| Low-side switch resistance <sup>(1)</sup>                 | PVIN=VIN= 5.0 V, lead length = 4 mm                                       |       | 37        |       | m $\Omega$       |
| Low-side switch resistance <sup>(1)</sup>                 | PVIN=VIN= 7.0 V, lead length = 4mm  |       | 36        |       | m $\Omega$       |
| <b>ERROR AMPLIFIER</b>                                    |   |       |           |       |                  |
| Error amplifier transconductance ( $g_m$ ) <sup>(2)</sup> | $-2\ \mu\text{A} < I_{COMP} < 2\ \mu\text{A}$ , $V_{(COMP)} = 1\text{ V}$ | 1000  | 1400      | 2000  | $\mu\text{S}$    |
| Error amplifier dc gain <sup>(2)</sup>                    | $V_{SENSE} = 0.804\text{ V}$  |       | 10000     |       | V/V              |
| Error amplifier source/sink <sup>(2)</sup>                | $V_{(COMP)} = 1\text{ V}$ , 100-mV input overdrive                        | -250  | $\pm 115$ | 250   | $\mu\text{A}$    |
| Error amplifier output resistance                         |   |       | 7         |       | M $\Omega$       |
| Start switching threshold <sup>(2)</sup>                  |   |       | 0.25      |       | V                |
| COMP to Iswitch $g_m$ <sup>(2)</sup>                      |   |       | 22        |       | S                |
| <b>CURRENT LIMIT</b>                                      |   |       |           |       |                  |
| High-side switch current limit threshold <sup>(3)</sup>   | $V_{IN} = 7.0\text{ V}$   |       | 11        |       | A                |
| Low-side switch sourcing current limit <sup>(3)</sup>     | $V_{IN} = 7.0\text{ V}$   |       | 10        |       | A                |
| Low-side switch sinking current limit                     | $V_{IN} = 7.0\text{ V}$   |       | 3         |       | A                |
| <b>THERMAL SHUTDOWN</b>                                   |   |       |           |       |                  |
| Thermal shutdown  |   |       | 170       |       | $^\circ\text{C}$ |
| Thermal shutdown hysteresis                               |   |       | 30        |       | $^\circ\text{C}$ |
| <b>INTERNAL SWITCHING FREQUENCY</b>                       |   |       |           |       |                  |
| Internally set frequency                                  | RT = Open   | 395   | 500       | 585   | kHz              |
| <b>EXTERNAL SYNCHRONIZATION</b>                           |   |       |           |       |                  |
| SYNC out low-to-high rise time (10%/90%)                  | $C_{load} = 25\text{ pF}$   |       | 70        | 111   | ns               |
| SYNC out high-to-low fall time (90%/10%)                  | $C_{load} = 25\text{ pF}$   |       | 6         | 15.5  | ns               |

(1) Measured at pins.

(2) Ensured by design only. Not tested in production.

(3) Parameter is not tested in production.

**Electrical Characteristics (continued)**
 $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V_{IN} = P_{VIN} = 3.0\text{ V}$  to  $7.0\text{ V}$  (unless otherwise noted)

| PARAMETER                                  | TEST CONDITIONS   | MIN  | TYP | MAX  | UNIT          |
|--|---|------|-----|------|---------------|
| Falling edge delay time <sup>(4)</sup>     |   |      | 180 |      | °             |
| SYNC out high level threshold              | $I_{OH} = 50\ \mu\text{A}$  | 2    |     |      | V             |
| SYNC out low level threshold               | $I_{OL} = 50\ \mu\text{A}$  |      |     | 600  | mV            |
| SYNC in low level threshold                | $P_{VIN}=V_{IN}= 3.0\text{ V}$  |      |     | 900  | mV            |
| SYNC in high level threshold               | $P_{VIN}=V_{IN}= 3.0\text{ V}$  | 2.45 |     |      | V             |
| SYNC in low level threshold                | $P_{VIN}=V_{IN}= 7.0\text{ V}$  |      |     | 900  | mV            |
| SYNC in high level threshold               | $P_{VIN}=V_{IN}= 7.0\text{ V}$  | 4.25 |     |      | V             |
| SYNC in frequency range <sup>(5)</sup>     | Percent of program frequency  | -5%  |     | 5%   |               |
|  |   | 100  |     | 1000 | kHz           |
| <b>PH (PH PIN)</b>                         |   |      |     |      |               |
| Minimum on time                            | Measured at 10% to 90% of $V_{IN}$ , $25^\circ\text{C}$ , $I_{PH} = 2\text{ A}$ |      | 190 | 235  | ns            |
| <b>SLOW START AND TRACKING (SS/TR PIN)</b> |   |      |     |      |               |
| SS charge current                          |   | 1.5  | 2.5 | 3    | $\mu\text{A}$ |
| SS/TR to VSENSE matching                   | $V_{(SS/TR)} = 0.4\text{ V}$  |      | 30  | 90   | mV            |
| <b>POWER GOOD (PWRGD PIN)</b>              |   |      |     |      |               |
| VSENSE threshold                           | $V_{SENSE}$ falling (fault)   |      | 91  |      | % Vref        |
|  | $V_{SENSE}$ rising (good)   |      | 94  |      | % Vref        |
|  | $V_{SENSE}$ rising (fault)  |      | 109 |      | % Vref        |
|  | $V_{SENSE}$ falling (good)  |      | 106 |      | % Vref        |
| Output high leakage                        | $V_{SENSE} = V_{ref}$ , $V(PWRGD) = 5\text{ V}$                                 |      | 30  | 181  | nA            |
| Output low                                 | $I_{(PWRGD)} = 2\text{ mA}$   |      |     | 0.3  | V             |
| Minimum $V_{IN}$ for valid output          | $V_{(PWRGD)} < 0.5\text{ V}$ at $100\ \mu\text{A}$                              |      | 0.6 | 1    | V             |
| Minimum SS/TR voltage for PWRGD            |   |      |     | 1.55 | V             |

(4) Bench verified. Not tested in production.

(5) Parameter is production tested at nominal voltage with  $V_{IN} = P_{VIN} = 5\text{ V}$ .

## 6.6 Typical Characteristics

System Efficiency curves (Figure 4, Figure 5, and Figure 6) include 2 outputs.

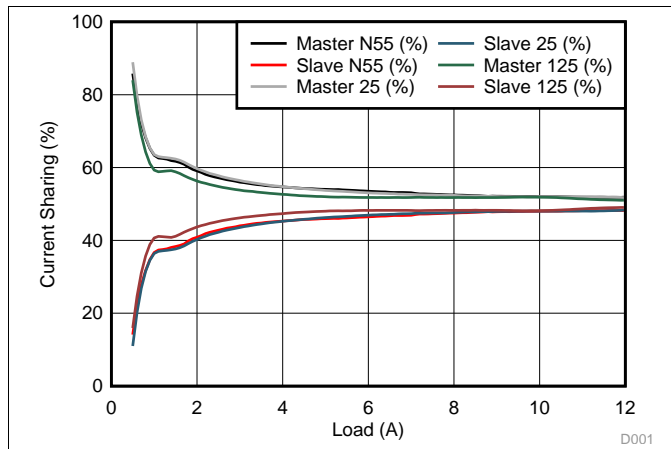


Figure 1. Current Sharing

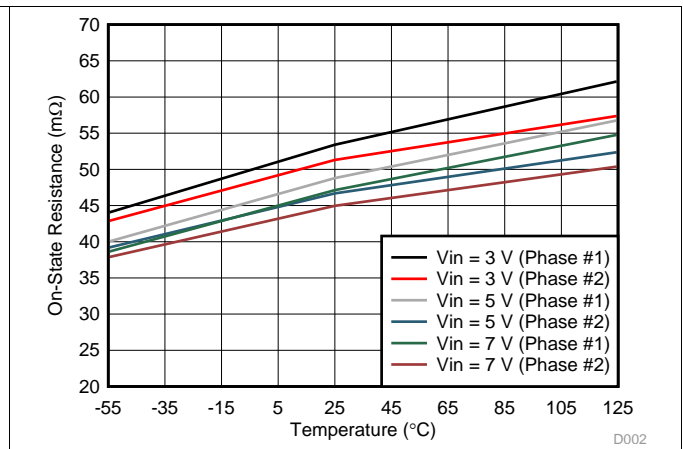


Figure 2. High-Side  $R_{DS(on)}$

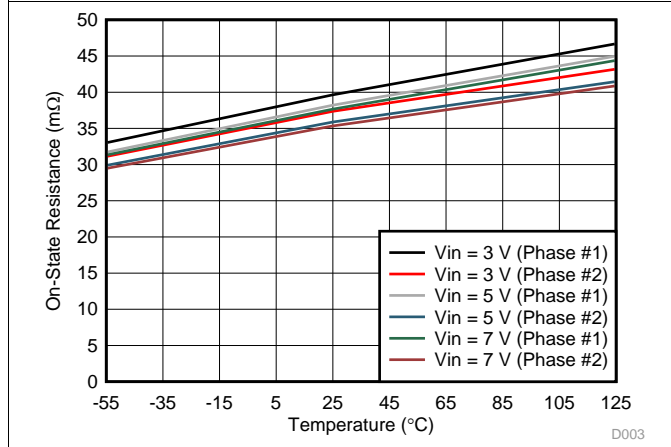


Figure 3. Low-Side  $R_{DS(on)}$

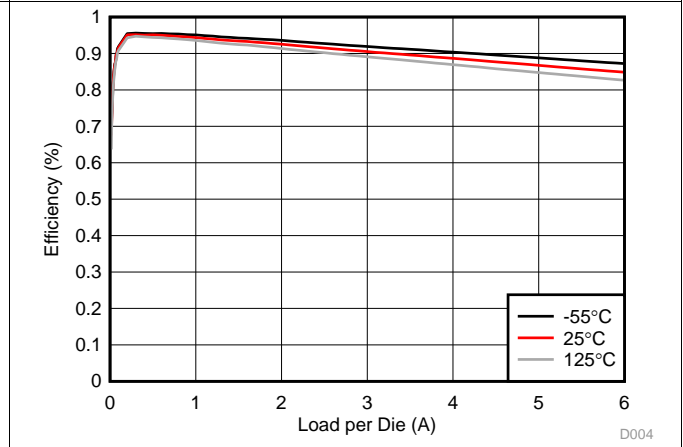


Figure 4. Efficiency at  $V_{IN} = P_{VIN} = 3.3\text{ V}$ ,  $F_{SW} = 500\text{ kHz}$

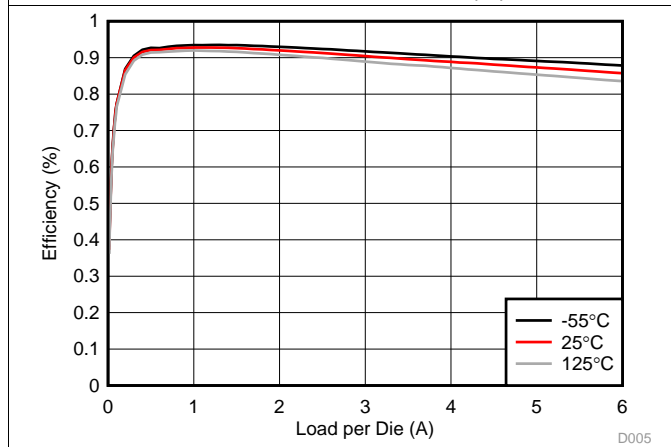


Figure 5. Efficiency at  $V_{IN} = P_{VIN} = 5\text{ V}$ ,  $F_{SW} = 500\text{ kHz}$

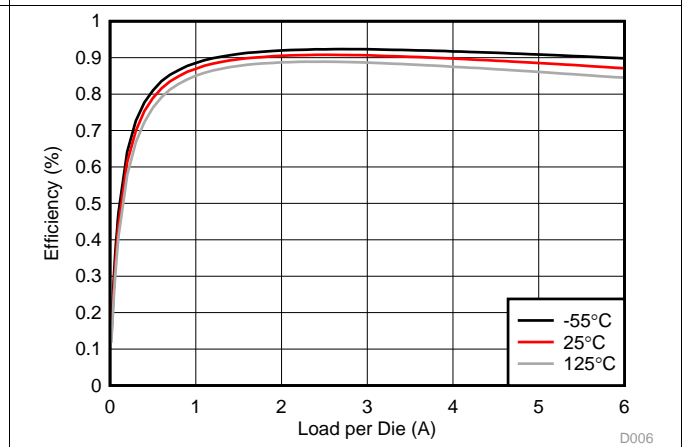


Figure 6. Efficiency at  $V_{IN} = P_{VIN} = 5\text{ V}$ ,  $F_{SW} = 100\text{ kHz}$  (External Clock)



## 7 Detailed Description

### 7.1 Overview

The TPS50602-SP is a dual TPS50601A-SP die device that can be configured in dual output or single output configuration. Each die is a 7-V, 6-A synchronous step-down (buck) converter with two integrated MOSFETs, a PMOS for the high side and a NMOS for the low side. To improve performance during line and load transients, the device implements a constant frequency, peak current mode control, which also simplifies external frequency compensation. The 500-kHz switching frequency allows for efficiency and size optimization when selecting the output filter components.

The device is designed for safe monotonic startup into prebiased loads. The default start up is when VIN is typically 3 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage UVLO with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pullup current. The total operating current for the device is approximately 5 mA when not switching and under no load. When the device is disabled, the supply current is typically less than 2.5 mA.

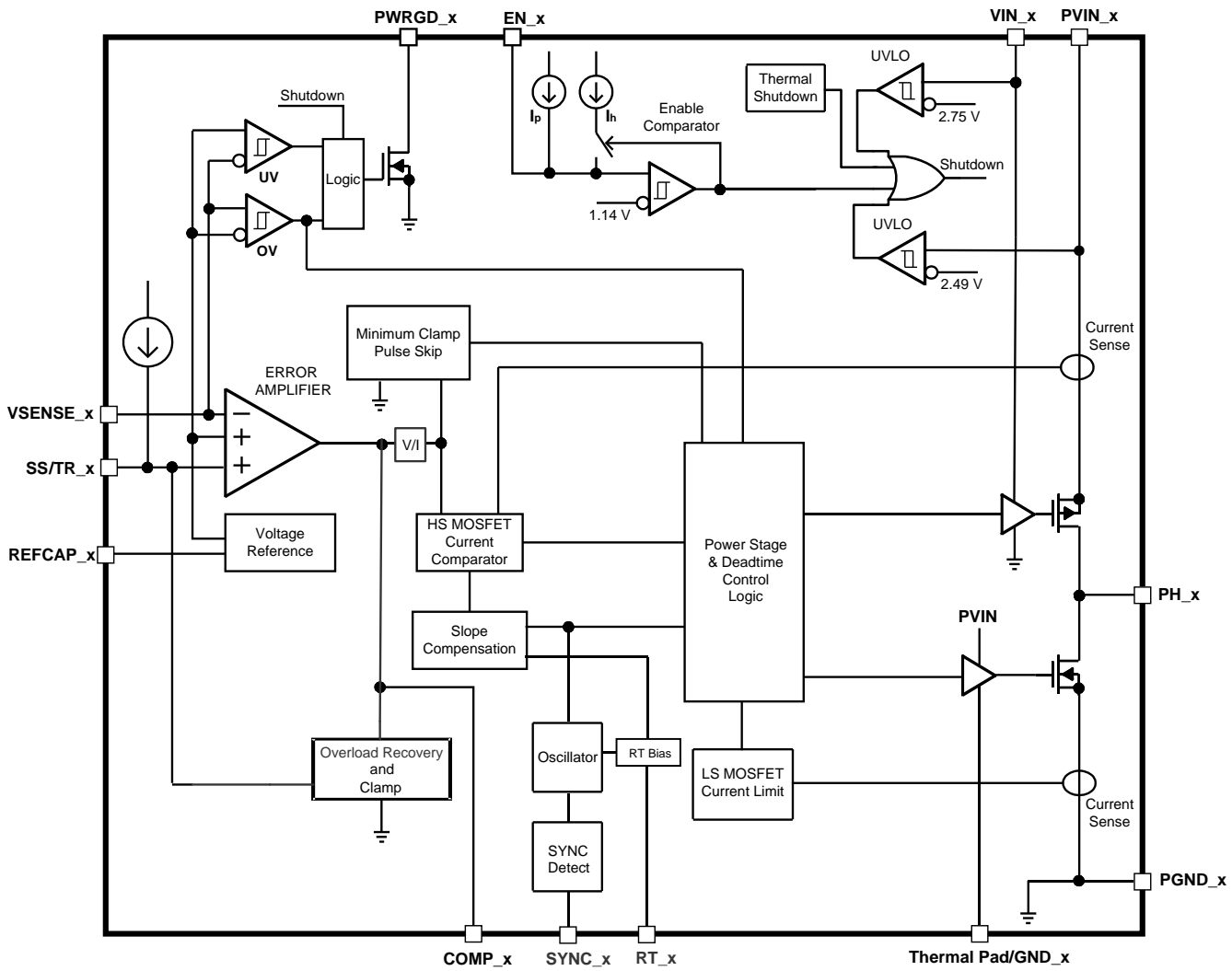
The integrated MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 6 A. The MOSFETs have been sized to optimize efficiency for lower duty cycle applications.

The device has a power good comparator (PWRGD) with hysteresis which monitors the output voltage through the VSENSE pin. The PWRGD pin is an open-drain MOSFET which is pulled low when the VSENSE pin voltage is less than 91% or greater than 109% of the reference voltage VREF and asserts high when the VSENSE pin voltage is 94% to 106% of the VREF.

The SS/TR (slow start/tracking) pin is used to minimize inrush currents or provide power-supply sequencing during power-up. A small-value capacitor or resistor divider should be coupled to the pin for slow start or critical power-supply sequencing requirements.

The device is protected from output overvoltage, overload, and thermal fault conditions. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage circuit power good comparator. When the overvoltage comparator is activated, the high-side MOSFET is turned off and prevented from turning on until the VSENSE pin voltage is lower than 106% of the VREF. The device implements both high-side MOSFET overload protection and bidirectional low-side MOSFET overload protections, which help control the inductor current and avoid current runaway. The device also shuts down if the junction temperature is higher than thermal shutdown trip point. The device is restarted under control of the slow-start circuit automatically when the junction temperature drops 10°C (typical) below the thermal shutdown trip point.

## 7.2 One of Two Dice of TPS50602-SP Functional Block Diagram



One of Two Dice

ADVANCE INFORMATION

### 7.3 Feature Description

#### 7.3.1 VIN and Power VIN Pins (VIN and PVIN)

The device allows for a variety of applications by using the VIN and PVIN pins together or separately. The VIN pin voltage supplies the internal control circuits of the device. The PVIN pin voltage provides the input voltage to the power converter system. Both pins have an input voltage range from 3 to 7 V. A voltage divider connected to the EN pin can adjust the input voltage UVLO appropriately. Adjusting the input voltage UVLO on the PVIN pin helps to provide consistent power-up behavior.

#### 7.3.2 Voltage Reference

The voltage reference system produces a precise voltage reference as indicated in [Electrical Characteristics](#).

#### 7.3.3 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output (VOUT) to the VSENSE pin. TI recommends to use 1% tolerance or better resistors. Start with a 10 kΩ for R<sub>TOP</sub> and use [Equation 1](#) to calculate R<sub>BOTTOM</sub>. To improve efficiency at light loads, consider using larger-value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

## Feature Description (continued)

$$R_{\text{BOTTOM}} = \frac{V_{\text{REF}}}{V_{\text{OUT}} - V_{\text{REF}}} \times R_{\text{TOP}}$$

where

- $V_{\text{REF}} = 0.804 \text{ V}$  (1)

### 7.3.4 Safe Start-Up into Prebiased Outputs

The device is designed to prevent the low-side MOSFET from discharging a prebiased output. During monotonic prebiased start-up, the low-side MOSFET is not allowed to sink current until the SS/TR pin voltage is higher than 1.55 V.

### 7.3.5 Error Amplifier

The device uses a transconductance error amplifier. The error amplifier compares the VSENSE pin voltage to the lower of the SS/TR pin voltage or the internal 0.804-V voltage reference. The transconductance of the error amplifier is 1400  $\mu\text{A/V}$  during normal operation. The frequency compensation network is connected between the COMP pin and ground. The error amplifier DC gain is typically 10,000 V/V.

### 7.3.6 Slope Compensation

The device adds a compensating ramp to the switch current signal. This slope compensation prevents subharmonic oscillations. The available peak inductor current remains constant over the full duty cycle range.

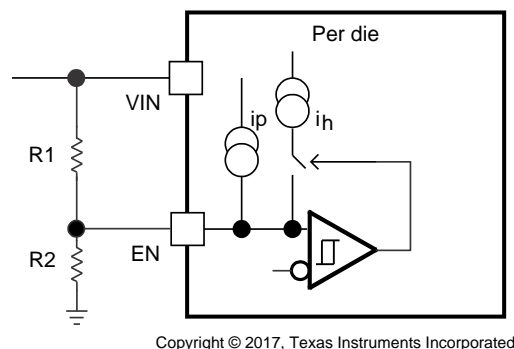
### 7.3.7 Enable and Adjust UVLO

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low  $I_q$  state. The EN pin has an internal pullup current source, allowing the user to float the EN pin for enabling the device. If an application requires controlling the EN pin, use open-drain or open-collector output logic to interface with the pin.

The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 150-mV typical.

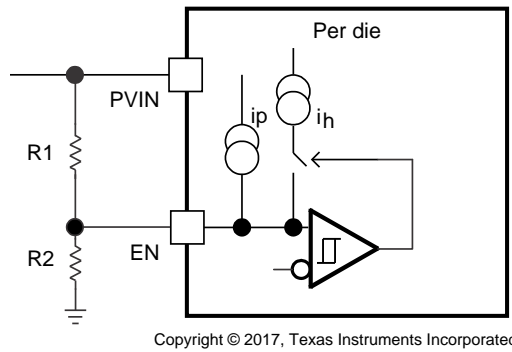
If an application requires either a higher UVLO threshold on the VIN pin or a secondary UVLO on the PVIN in split-rail applications, then the EN pin can be configured as shown in [Figure 7](#), [Figure 8](#), and [Figure 9](#). A ceramic capacitor in parallel with the bottom resistor  $R_2$  is recommended to reduce noise on the EN pin as used in the TPS50602-SP Evaluation Module, (see the TPS50602-SP EVM User's Guide, [SLVUB65](#)).

The EN pin has a small pullup current,  $I_p$ , which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function because it increases by  $I_h$  after the EN pin crosses the enable threshold. Calculate the UVLO thresholds with [Equation 2](#) and [Equation 3](#).

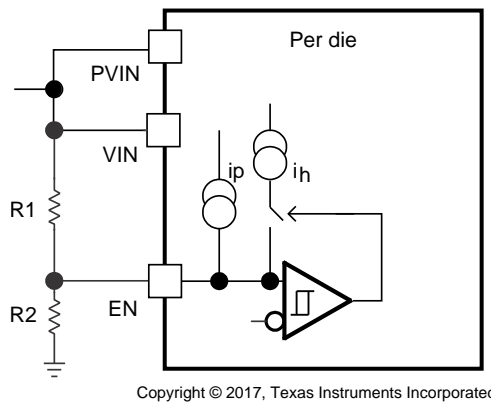


**Figure 7. Adjustable VIN UVLO**

**Feature Description (continued)**



**Figure 8. Adjustable PVIN UVLO**



**Figure 9. Adjustable VIN and PVIN UVLO**

$$R_1 = \frac{V_{START} \times \frac{V_{ENFALLING}}{V_{ENRISING}} - V_{STOP}}{I_p \left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \tag{2}$$

**ADVANCE INFORMATION**

## Feature Description (continued)

$$R_2 = \frac{R_1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_1(I_p + I_h)}$$

where

- $I_h = 3 \mu\text{A}$
- $I_p = 6.1 \mu\text{A}$
- $V_{ENRISING} = 1.14 \text{ V}$
- $V_{ENFALLING} = 1.11 \text{ V}$

(3)

### 7.3.8 Fixed Switching Frequency and Synchronization (SYNC)

The two dice in the TPS50602-SP must be operated at the same switching frequency and at 180° out of phase. There are then 2 main modes of operation: using the internal oscillator mode or using an external clock driving the SYNC pin. In internal oscillator mode, (500-kHz fixed switching frequency), one die must have its RT pin floating so that the synchronous pin becomes the output and there is a phase inversion. This output signal is used to drive the second die. The RT pin of the second die must have its RT pin populated such that the converter frequency of the slave converter must be within ±5% of the master converter. This is required because the RT pin also sets the proper operation of slope compensation.

In external synchronization mode, the switching frequency could be anywhere between 100 kHz and 1 MHz as long as the clocks feeding the 2 dice are 180° out of phase. In this mode of operation, a resistor is connected between the RT pin and GND. The SYNC pin requires a toggling signal for this mode to be effective. The switching frequency of the device goes 1:1 with that of SYNC pin. External system clock-user supplied sync clock signal determines the switching frequency. If no external clock signal is detected for 20 μs, then TPS50601A-SP transitions to its internal clock, which is typically 500 kHz. RT values of the master and slave converter must be within ±5% of the external synchronization frequency. This is necessary for proper slope compensation. A resistance in the RT pin is required for proper operation of the slope compensation circuit. To determine the RT resistance for a given switching frequency, use Equation 4 or the curve in Figure 10.

$$RT(F_{SW}) = 67009 \times F_{SW}^{-1.0549}$$

where

- RT in kΩ
- $F_{SW}$  in kHz

(4)

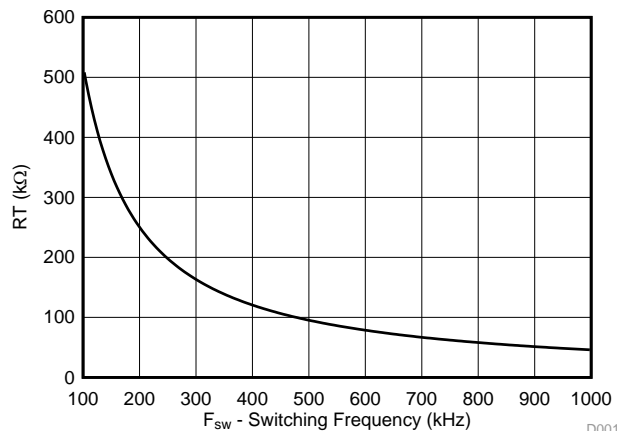


Figure 10. RT vs Switching Frequency

### 7.3.9 Slow Start (SS/TR)

The device uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a slow-start time. Equation 5 shows the calculations for the slow-start time ( $t_{SS}$ , 10% to 90%) and slow-start capacitor ( $C_{SS}$ ). The voltage reference ( $V_{REF}$ ) is 0.804 V and the slow-start charge current ( $I_{SS}$ ) is 2 μA.

## Feature Description (continued)

$$t_{SS}(\text{ms}) = \frac{C_{SS}(\text{nF}) \times V_{REF}(\text{V})}{I_{SS}(\mu\text{A})} \quad (5)$$

When any of the following 3 scenarios occur; the input UVLO is triggered, the EN pin is pulled below 1.05 V, or a thermal shutdown event occurs; the device stops switching and enters low current operation. At the subsequent power-up, when the shutdown condition is removed, the device does not start switching until it has discharged its SS/TR pin to ground ensuring proper soft-start behavior.

### 7.3.10 Power Good (PWRGD)

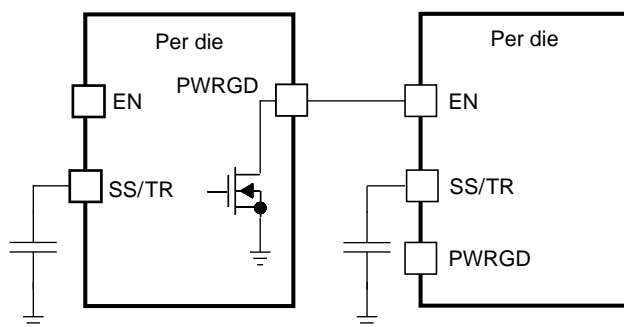
The PWRGD pin is an open-drain output. When the VSENSE pin is between 94% and 106% of the internal voltage reference, the PWRGD pin pulldown is deasserted and the pin floats. TI recommends to use a pullup resistor between 10 kΩ to 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD is in a defined state when the VIN input voltage is greater than 1 V but has reduced current sinking capability. The PWRGD achieves full current sinking capability when the VIN input voltage is above 3 V.

The PWRGD pin is pulled low when VSENSE is lower than 91% or greater than 109% of the nominal internal reference voltage. Also, the PWRGD is pulled low, if the input UVLO or thermal shutdown are asserted, the EN pin is pulled low or the SS/TR pin is below 1.55 V.

### 7.3.11 Sequencing (SS/TR)

Many of the common power-supply sequencing methods can be implemented using the SS/TR, EN, and PWRGD pins.

The sequential method is shown in [Figure 11](#) using two TPS50601A-SP devices. The power good of the first device is coupled to the EN pin of the second device, which enables the second power supply after the primary supply reaches regulation.



**Figure 11. Sequential Start-Up Sequence**

[Figure 12](#) shows the method implementing ratiometric sequencing by connecting the SS/TR pins of two devices together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow-start time, the pullup current source must be doubled in [Equation 5](#).

Feature Description (continued)

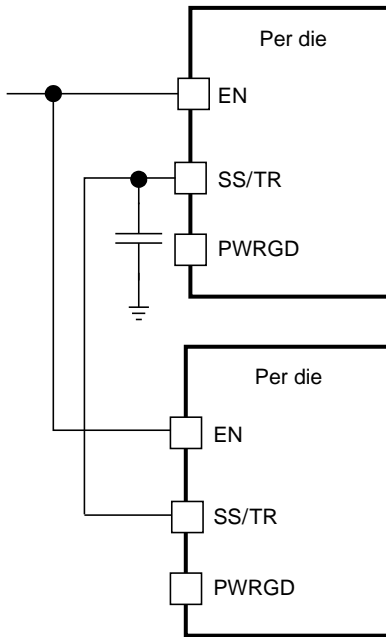


Figure 12. Ratiometric Start-Up Sequence

Ratiometric and simultaneous power-supply sequencing can be implemented by connecting the resistor network of  $R_1$  and  $R_2$  (shown in Figure 13) to the output of the power supply that needs to be tracked or another voltage reference source. Using Equation 6 and Equation 7, the tracking resistors can be calculated to initiate the  $VOUT_2$  slightly before, after, or at the same time as  $VOUT_1$ . Equation 8 is the voltage difference between  $VOUT_1$  and  $VOUT_2$ .

To design a ratiometric start-up in which the  $VOUT_2$  voltage is slightly greater than the  $VOUT_1$  voltage when  $VOUT_2$  reaches regulation, use a negative number in Equation 6 and Equation 7 for  $\Delta V$ . Equation 8 results in a positive number for applications where the  $VOUT_2$  is slightly lower than  $VOUT_1$  when  $VOUT_2$  regulation is achieved.

The  $\Delta V$  variable is 0 V for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset ( $V_{SS-OFFSET}$ , 30 mV) in the slow-start circuit and the offset created by the pullup current source ( $I_{SS} = 2 \mu A$ ) and tracking resistors, the  $V_{SS-OFFSET}$  and  $I_{SS}$  are included as variables in the equations.

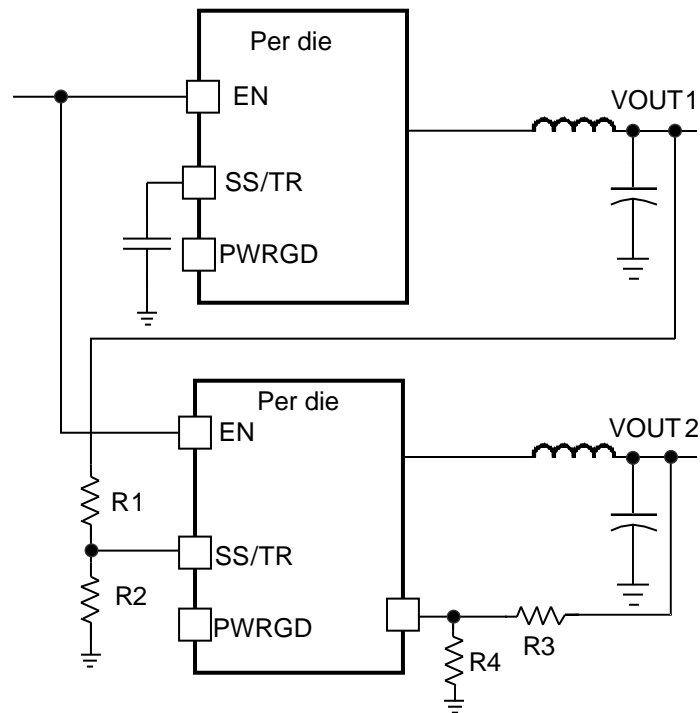
To ensure proper operation of the device, the calculated  $R_1$  value from Equation 6 must be greater than the value calculated in Equation 9.

$$R_1 = \frac{VOUT_2 + \Delta V}{V_{REF}} \times \frac{V_{SS-OFFSET}}{I_{SS}} \tag{6}$$

$$R_2 = \frac{V_{REF} \times R_1}{VOUT_2 + \Delta V - V_{REF}} \tag{7}$$

$$\Delta V = VOUT_1 - VOUT_2 \tag{8}$$

$$R_1 > 2800 \times VOUT_1 - 180 \times \Delta V \tag{9}$$

**Feature Description (continued)**

**Figure 13. Ratiometric and Simultaneous Start-Up Sequence**
**7.3.12 Output Overvoltage Protection (OVP)**

The device incorporates an output OVP circuit to minimize output voltage overshoot. For example, when the power supply output is overloaded, the error amplifier compares the actual output voltage to the internal reference voltage. If the VSENSE pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier demands maximum output current. After the condition is removed, the regulator output rises and the error amplifier output transitions to the steady-state voltage. In some applications with small output capacitance, the power supply output voltage can respond faster than the error amplifier. This leads to the possibility of an output overshoot. The OVP feature minimizes the overshoot by comparing the VSENSE pin voltage to the OVP threshold. If the VSENSE pin voltage is greater than the OVP threshold, the high-side MOSFET is turned off, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVP threshold, the high-side MOSFET is allowed to turn on at the next clock cycle.

**7.3.13 Overcurrent Protection**

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side and low-side MOSFET.

**7.3.13.1 High-Side MOSFET Overcurrent Protection**

The device implements current mode control which uses the COMP pin voltage to control the turn off of the high-side MOSFET and the turn on of the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the current reference generated by the COMP pin voltage are compared, when the peak switch current intersects the current reference, the high-side switch is turned off.



## Feature Description (continued)

### 7.3.13.2 Low-Side MOSFET Overcurrent Protection

While the low-side MOSFET is turned on its conduction current is monitored by the internal circuitry. During normal operation the low-side MOSFET sources current to the load. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current limit. If the low-side sourcing current is exceeded, the high-side MOSFET is not turned on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET is turned on again when the low-side current is below the low-side sourcing current limit at the start of a cycle.

The low-side MOSFET may also sink current from the load. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off immediately for the rest of that clock cycle. In this scenario, both MOSFETs are off until the start of the next cycle.

When the low-side MOSFET turns off, the switch node increases and forward biases the high-side MOSFET parallel diode (the high-side MOSFET is still off at this stage).

### 7.3.14 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 175°C (typical). The device reinitiates the power-up sequence when the junction temperature drops below 165°C (typical).

### 7.3.15 Turn-On Behavior

Minimum on-time specification determines the maximum operating frequency of the design. As the unit starts up and goes through its soft-start process, the required duty-cycle is less than the minimum controllable on-time. This can cause the converter to skip pulses. Thus, instantaneous output pulses can be higher or lower than the desired voltage. This behavior is only evident when operating at high frequency with high bandwidth. When the minimum on-pulse is greater than the minimum controllable on-time, the turn-on behavior is normal.

### 7.3.16 Small Signal Model for Frequency Compensation

The device uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits shown in Figure 14. In Type 2A, one additional high-frequency pole is added to attenuate high-frequency noise.

The following design guidelines are provided for advanced users who prefer to compensate using the general method. The step-by-step design procedure described in [Detailed Design Procedure](#) may also be used.

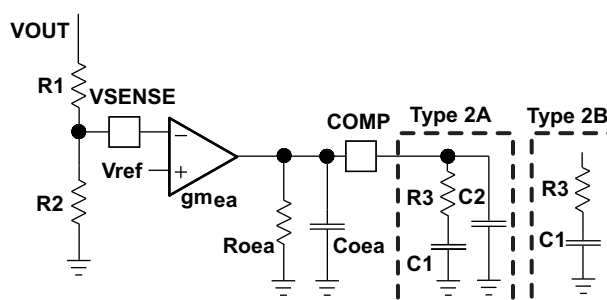


Figure 14. Types of Frequency Compensation

The general design guidelines for device loop compensation are as follows:

1. Determine the crossover frequency  $f_{co}$ . A good starting point is one-tenth of the switching frequency,  $F_{SW}$ .
2.  $R_3$  can be determined by:

$$R_3 = \frac{2\pi \times f_{co} \times V_{OUT} \times C_{OUT}}{g_{mea} \times V_{ref} \times g_{mps}} \quad (10)$$

where  $g_{mea}$  is the gm of the error amplifier (1400  $\mu$ S),  $g_{mps}$  is the gm of the power stage (22 S) and  $V_{REF}$  is the reference voltage (0.804 V).

**Feature Description (continued)**

3. Place a compensation zero at the dominant pole  $f_p = \frac{1}{C_{OUT} \times R_L \times 2\pi}$  using  $C_1$  and  $R_3$ .  
 $C_1$  can be determined by

$$C_1 = \frac{C_{OUT} \times R_L}{R_3} \quad (11)$$

4.  $C_2$  is optional. It can be used to cancel the zero from the equivalent series resistance (ESR) of the output capacitor  $C_{OUT}$ .

$$C_2 = \frac{C_{OUT} \times R_{ESR}}{R_3} \quad (12)$$

**7.4 Device Functional Modes**
**7.4.1 Fixed-Frequency PWM Control**

The device uses fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is converted into a current reference which compares to the high-side power switch current. When the power switch current reaches the current reference generated by the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on.

**7.4.2 Continuous Current Mode (CCM) Operation**

As a synchronous buck converter, the device normally works in CCM under all load conditions.

## 8 Application and Implementation

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### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 8.1 Application Information

The TPS50602-SP device is a highly-integrated synchronous step-down DC-DC converter. The device is used to convert a higher DC-DC input voltage to a lower DC output voltage with a maximum output current of 12-A in single output configuration or 6-A in dual output configuration.

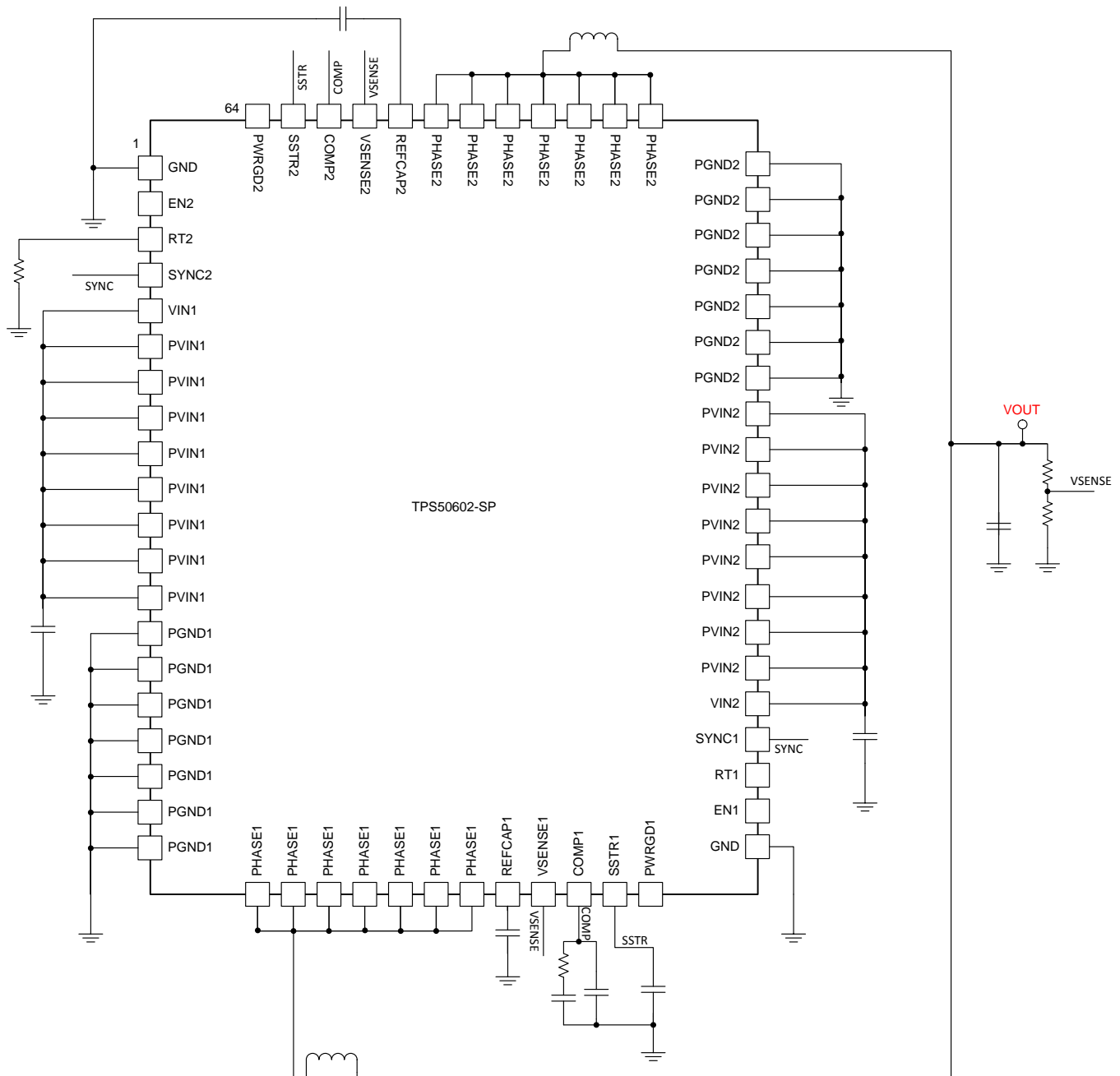
The TPS50602-SP user's guide is available on the TI website (see [SLVUB66](#)). The guide highlights standard EVM test results, schematic, and BOM for reference (basic design equations in following sections are provided for reference only).

### 8.2 Typical Application

## Typical Application (continued)

### 8.2.1 12-A Single Output Configuration

The TPS50602-SP can be configured for a 12-A single output voltage as shown in Figure 15. In this case, the 2 dice in the package run in master-slave configuration at an internal 500-kHz switching frequency (internal oscillator) or an external clock but 180° out of phase in both cases. If using internal oscillator, the RT1 pin is left floating since SYNC1 is used as an output clock signal for SYNC2. A resistor is then connected to the RT2 pin to set the frequency to 500 kHz. Please refer to [Fixed Switching Frequency and Synchronization \(SYNC\)](#) section for more details regarding switching frequency configuration. The SS, SSTR and VSENSE pins for each die are connected one to another.



**Figure 15. 12-A Single Output Configuration**

The design procedure to configure the master-slave operation using the internal oscillator is as follows:

## Typical Application (continued)

1. The RT pin of the master device must be left floating. This achieves 2 purposes, to set the frequency to 500 kHz (typical) using the internal oscillator and to configure the SYNC pin of the master device as an output pin with a 500-kHz clock, 180° out of phase respect to the internal oscillator of the master device. For more details, see [Fixed Switching Frequency and Synchronization \(SYNC\)](#) section.
2. The RT pin on slave device should be connected to a resistor such that the frequency of the slave device is within 5% of the master's frequency, 500 kHz in this case. See [Figure 10](#) for reference.
3. SYNC pin of the master device must be connected to the SYNC pin of the slave device.
4. Only a single feedback network is needed connected to the VSENSE pin of the master device. Therefore, both VSENSE pins must be connected.
5. Only a single compensation network is needed connected to the COMP pin of the master device. Therefore both COMP pins must be connected.
6. Only a single soft start capacitor is needed connected to the SS pin of the master device. Therefore both SS pins must be connected.
7. Only a single enable signal (or resistor divider) is needed connected to the EN pin of the master device. Therefore both EN pins must be connected.
8. Since the master device controls the compensation, soft start and enable networks, the factor of 2 must be taken into account when calculating the components associated with these pins.

The master-slave mode can also be implemented using an external clock. In such case, a different frequency other than 500 kHz can be used. When using an external clock, only the RT and SYNC pins configuration varies as follows:

1. RT pins of both master and slave device must be connected to a resistor matching the frequency of the external clock being used. See [Figure 10](#) for reference.
2. The external clock is connected to the SYNC pin of the master device. A 10-kΩ resistor to GND should be connected to the SYNC pin as well.
3. An inverted clock (180° out of phase respect to the master device) must be connected to the SYNC pin of the slave device. A 10-kΩ resistor to GND should be connected to the SYNC pin as well.

### 8.2.2 6-A Dual Output Configuration

The 6-A dual output configuration of the TPS50602-SP allows for great area savings. In this case, the 2 dice in the TPS50602-SP can be configured individually as shown in [Figure 16](#) but they must run 180° out of phase at an internal 500-kHz switching frequency (internal oscillator) or an external clock but. If using internal oscillator, the RT1 pin is left floating since SYNC1 is used as an output clock signal for SYNC2. A resistor is then connected to the RT2 pin to set the frequency to 500 kHz. Please refer to [Fixed Switching Frequency and Synchronization \(SYNC\)](#) section for more details regarding switching frequency configuration.

Typical Application (continued)

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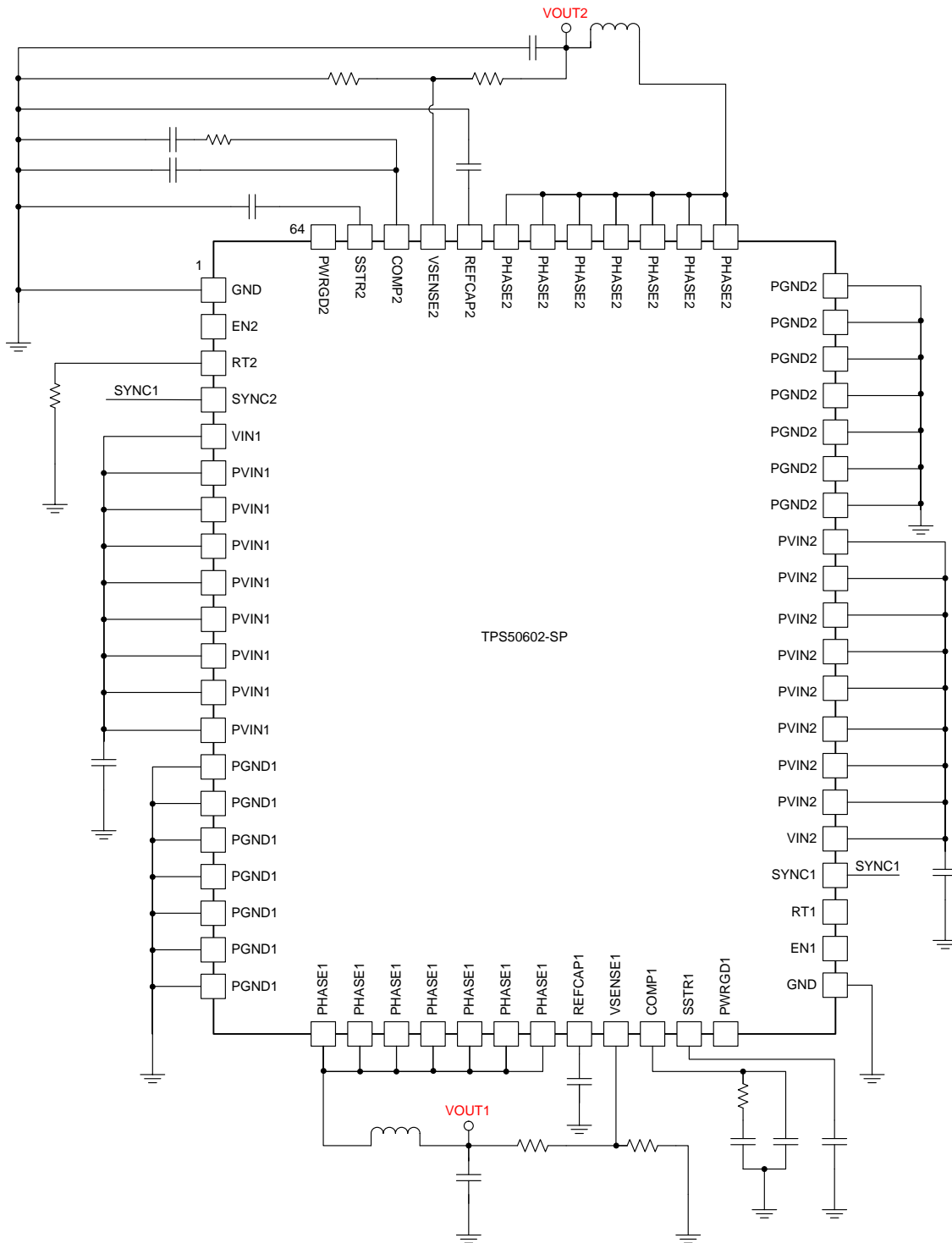


Figure 16. 6-A Dual Output Configuration

## Typical Application (continued)

### 8.2.3 Design Requirements

This example highlights a design for the TPS50601A-SP die (VOUT1) in the TPS50602-SP evaluation module in Dual Output Configuration. For more details, please refer to the EVM user's guide (see [SLVUB66](#)). A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

**Table 1. Design Parameters**

| DESIGN PARAMETER                       | EXAMPLE VALUE                 |
|--|-------------------------------|
| Output voltage                         | 2.5 V                         |
| Maximum output current                 | 6 A                           |
| Transient response 1-A load step       | $\Delta V_{OUT} = 5\%$        |
| Input voltage                          | 5-V nominal, 4.5 V to 7 V     |
| Output voltage ripple                  | 20 mVp-p                      |
| Start input voltage (rising $V_{IN}$ ) | 4.5 V                         |
| Stop input voltage (falling $V_{IN}$ ) | 4.3 V                         |
| Switching frequency                    | 500 kHz (internal oscillator) |

### 8.2.4 Detailed Design Procedure

#### 8.2.4.1 Operating Frequency

In this design, a switching frequency of 500 kHz is selected. Based on the [Fixed Switching Frequency and Synchronization \(SYNC\)](#) section, the RT1 is left floating and the SYNC1 pin is used to drive the SYNC2 pin and the RT2 pin must have a 95.3-k $\Omega$  resistor.

#### 8.2.4.2 Output Inductor Selection

To calculate the value of the output inductor, use [Equation 13](#).  $K_L$  is a coefficient that represents the amount of inductor ripple current relative to the maximum output current,  $I_O$ . The inductor ripple current is filtered by the output capacitor therefore, choosing high-inductor ripple currents impact the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer depending on specific system needs. Typical values for  $K_L$  range from 0.1 to 0.5. For low output currents, the value of  $K_L$  could be increased to reduce the value of the output inductor.

$$L = \frac{V_{INMAX} - V_{OUT}}{I_O \times K_L} \times \frac{V_{OUT}}{V_{INMAX} \times f_{SW}} \quad (13)$$

For this design example, use  $K_L = 0.45$  and the inductor value is calculated to be 1.8  $\mu\text{H}$  for nominal  $V_{IN} = 5 \text{ V}$ .

#### 8.2.4.3 Output Capacitor Selection

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load such as a transition from no load to full load. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change. [Equation 14](#) shows the minimum output capacitance, from the electrical point of view, necessary to accomplish this.

$$C_{OUT} > \frac{2 \times I_O}{f_{SW} \times \Delta V_{OUT}} \quad (14)$$

Where  $\Delta I_O$  is the change in output current,  $F_{SW}$  is the regulator switching frequency and  $\Delta V_{OUT}$  is the allowable change in the output voltage. For this example, the transient load response is specified as a 5% change in  $V_{OUT}$  for a load step of 1 A. For this example,  $\Delta I_O = 1$  A and  $\Delta V_{OUT} = 0.05 \times 2.5 = 0.125$  V. Using these numbers gives a minimum capacitance of 160  $\mu$ F. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. However, for space applications and large capacitance values, tantalum capacitors are typically used which have a certain ESR value to take into consideration.

[Equation 15](#) calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where  $F_{SW}$  is the switching frequency,  $V_{OUT\_ripple}$  is the maximum allowable output voltage ripple, and  $I_{ripple}$  is the inductor ripple current. In this case, the maximum output voltage ripple is 20 mV. Under this requirement, [Equation 15](#) yields 168.75  $\mu$ F.

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{I_{ripple}}{V_{OUT\_ripple}} \quad (15)$$

[Equation 16](#) calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. [Equation 16](#) indicates the ESR should be less than 7.41 m $\Omega$ .

$$R_{ESR} < \frac{V_{OUT\_ripple}}{I_{ripple}} \quad (16)$$

For this specific design, taking into consideration the stringent requirements for space applications, two output capacitors of 330  $\mu$ F ( $C_{OUT} = 660$   $\mu$ F) with ESR = 6 m $\Omega$  each have been selected.

#### 8.2.4.4 Slow Start Capacitor Selection

The slow start capacitor  $C_{SS}$ , determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS50601A-SP reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. The soft start capacitor value can be calculated using [Equation 5](#). The example circuit has the soft start time set to an arbitrary value of about 4 ms which requires a 10-nF capacitor. In TPS50601A-SP,  $I_{SS}$  is 2- $\mu$ A typical, and  $V_{REF}$  is 0.804 V.

#### 8.2.4.5 Undervoltage Lockout (UVLO) Set Point

The UVLO can be adjusted using the external voltage divider network formed by  $R_1$  and  $R_2$ .  $R_1$  is connected between  $V_{IN}$  and the EN pin of the TPS50601A-SP and  $R_2$  is connected between EN and GND. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above selected voltage (UVLO start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below (UVLO stop or disable) voltage. [Equation 2](#) and [Equation 3](#) can be used to calculate the values for the upper and lower resistor values. For the stop voltages specified in [Table 1](#), the nearest standard resistor value for  $R_1$  is 10 k $\Omega$  and for  $R_2$  is 3.4 k $\Omega$ .

#### 8.2.4.6 Output Voltage Feedback Resistor Selection

The resistor divider network  $R_{TOP}$  and  $R_{BOTTOM}$  is used to set the output voltage. For the example design, 10 k $\Omega$  was selected for  $R_{TOP}$ . Using [Equation 1](#),  $R_{BOTTOM}$  is calculated as 4.77 k $\Omega$ . A 4.64-k $\Omega$  resistor was used for this design.

#### 8.2.4.7 Compensation Component Selection

There are several industry techniques used to compensate DC-DC regulators. For this design, type 2B compensation is used as shown in the [Small Signal Model for Frequency Compensation](#) section.



First, the modulator pole,  $f_{pmod}$ , and the  $R_{ESR}$  zero,  $f_{zmod}$  must be calculated using [Equation 17](#) and [Equation 18](#). Use [Equation 19](#) and [Equation 20](#) to estimate a starting point for the closed loop crossover frequency  $f_{co}$ , then the required compensation components may be derived. For this design example,  $f_{pmod}$  is 0.58 kHz and  $f_{zmod}$  is 80.36 kHz. [Equation 19](#) is the geometric mean of the modulator pole and the ESR zero and [Equation 20](#) is the geometric mean of the modulator pole and one half the switching frequency. Use a frequency near the lower of these two values as the intended crossover frequency  $f_{co}$ . In this case [Equation 19](#) yields 6.82 kHz and [Equation 20](#) yields 12.03 kHz. A frequency of 10 kHz is chosen as the intended crossover frequency.

$$f_{pmod} = \frac{I_{OUT}}{2\pi \times V_{OUT} \times C_{OUT}} \quad (17)$$

$$f_{zmod} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \quad (18)$$

$$f_{co} = \sqrt{f_{pmod} \times f_{zmod}} \quad (19)$$

$$f_{co} = \sqrt{f_{pmod} \times \frac{f_{SW}}{2}} \quad (20)$$

Now the compensation components can be calculated using [Equation 10](#) and [Equation 11](#). The standard values for  $R_3$  and  $C_1$  are 4.02 k $\Omega$  and 68 nF, respectively.

### 8.2.5 Application Curve

The evaluation module for the TPS50602-SP was used to capture a load step response of the device. The testing conditions were:

- $V_{IN} = P_{VIN} = 5\text{ V}$
- $V_{OUT} = 2.5\text{ V}$
- Load step = 0 A to 5 A
- Switching frequency = 500 kHz

## 9 Power Supply Recommendations

The TPS50602-SP is designed to operate from an input voltage supply range between 3 V and 7 V. This supply voltage must be well regulated and proper local bypass capacitors should be used for proper electrical performance from  $P_{VIN}$  to GND and from  $V_{IN}$  to GND. Due to stringent requirements for space applications, typically additional input bypass capacitors are used. The TPS50602-SP Evaluation Module uses 6, 22- $\mu\text{F}$  ceramic capacitors in addition to 3, 150- $\mu\text{F}$  tantalum capacitors from  $P_{VIN}$  to GND and a 4.7  $\mu\text{F}$  and a 0.1  $\mu\text{F}$  from  $V_{IN}$  to GND.

## 10 Layout

### 10.1 Layout Guidelines

Layout is a critical portion of good power supply design. Standard good practices should be applied. Some basic guidelines follow:

- The top layer contains the main power traces for  $P_{VIN}$ ,  $V_{IN}$ ,  $V_{OUT}$ , and PHASE. Also on the top layer are connections for the remaining pins of the TPS50602-SP and a large top side area filled with ground.
- The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor and the output filter capacitor.
- Thermal pad can be electrically floating or connected externally. If electrically connected externally then it must be connected to GND. Customer should evaluate their system performance when thermal pad is electrically isolated and thermally conductive.
- Preferred approach is that GND pin should be tied directly to the power pad under the IC and the PGND.
- The  $P_{VIN}$  and  $V_{IN}$  pins should be bypassed to ground with ceramic capacitors placed as close as possible to the pins.
- Since the PH connection is the switching node, the output inductor should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The RT, REFCAP and COMP pins are sensitive to noise so the respective components should be located as close as possible to the IC and routed with minimal lengths of trace.
- The feedback voltage signal  $V_{SENSE}$  should be routed away from the switching node.

## 10.2 Layout Example

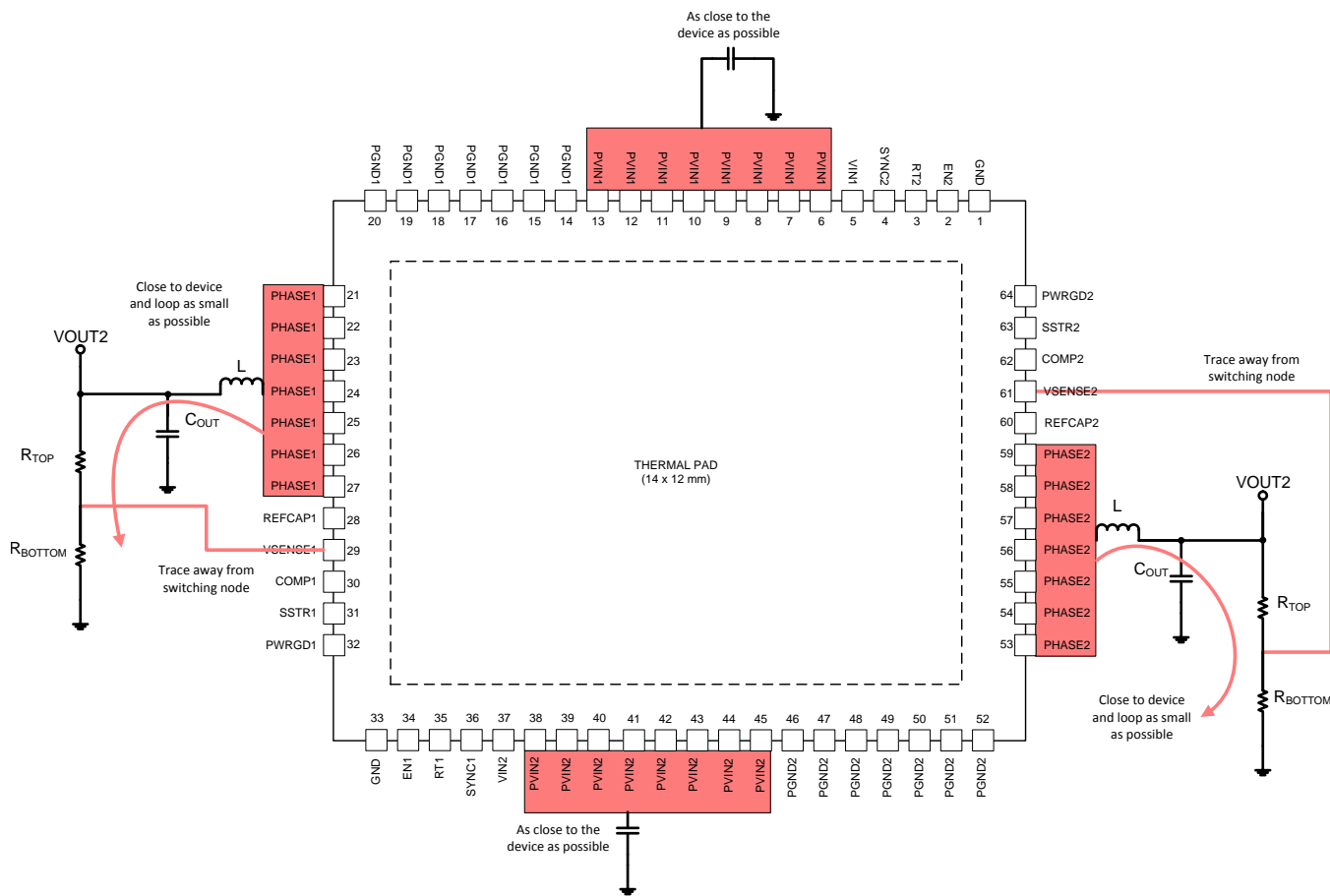


Figure 17. PCB Layout Example

ADVANCE INFORMATION

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

*TPS50602EVM-CVAL Evaluation Module*, [SLVUB66](#)

### 11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 12.1 Device Nomenclature

**RHA** Radiation hardness assurance for space systems

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|-------------------------|----------------------|--------------|-------------------------|---------|
| PTPS50602HFG/EM  | ACTIVE        | CFP          | HFG             | 64   | 1           | TBD             | Call TI                 | Call TI              | 25 to 25     |                         | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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