ECE1117

Multi-Function BC-Link™/SMBus Companion Device

Product Features

- Microchip BC-Link™ Slave Interface to Host EC
  - 3-pin point-to-point communication link to Embedded Controller
- Optional SMBus Slave Interface to Host EC
  - BC-Link/SMBus protocol autodetect
  - Strap pin selects between two slave addresses at POR
  - Dynamically programmed slave address after POR
- Keyboard Scan Matrix
  - Up to 19x8 Keyboard Scan Matrix
- LED Output Pins
  - 7 LED Output Pins
    - 4 with 20mA current sink
    - 3 with 4mA current sink
  - Multiple Clock Rates
  - Breathe capability
  - Open Drain
  - 5V tolerant
  - All can be synchronized
- General Purpose I/O Pins
  - 16 General Purpose I/O Pins
  - All are BC Bus addressable I/O Pins
  - All are Maskable Hardware Wake-Event Capable
  - All are Programmable Open-Drain/Push-Pull Outputs
- Two PS/2 Ports
- One Power Plane
  - Low Standby Current in Sleep Mode
- 3.3 Volt Operation
- Package
  - 48-pin QFN, 7x7mm body, 0.5mm pitch
  - 48-pin SQFN, 7x7mm body, 0.5mm pitch

Description

The ECE1117 is a 48-pin 3.3V multi-function companion device. The ECE1117 communicates with an upstream host via BC-Link or SMBus.

The ECE1117 is typically mounted in the keyboard assembly. By mounting the ECE1117 onto the keyboard assembly, the keyboard signals as well as the touchpad/point stick PS/2 signals and the backlight PWMs are routed from the keyboard to the motherboard over a single BC-Link or SMBus connection.

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1.0   GENERAL DESCRIPTION

The ECE1117 is a 48-pin 3.3V multi-function companion device. The ECE1117 communicates with the upstream host via BC-Link or SMBus.

The typical usage model is to locate the ECE1117 in the keyboard assembly. By mounting the ECE1117 onto the keyboard assembly, the keyboard signals as well as the touchpad/point stick PS/2 signals and the backlight PWMs are routed from the keyboard to the motherboard over a single BC-Link connection. In all other notebook designs without BC companion device, the keyboard matrix signals, PS/2 and LEDs are routed to the motherboard via a wide ribbon extension for the keyboard switch circuit.

1.1   Block Diagram

FIGURE 1-1:   ECE1117 BLOCK DIAGRAM
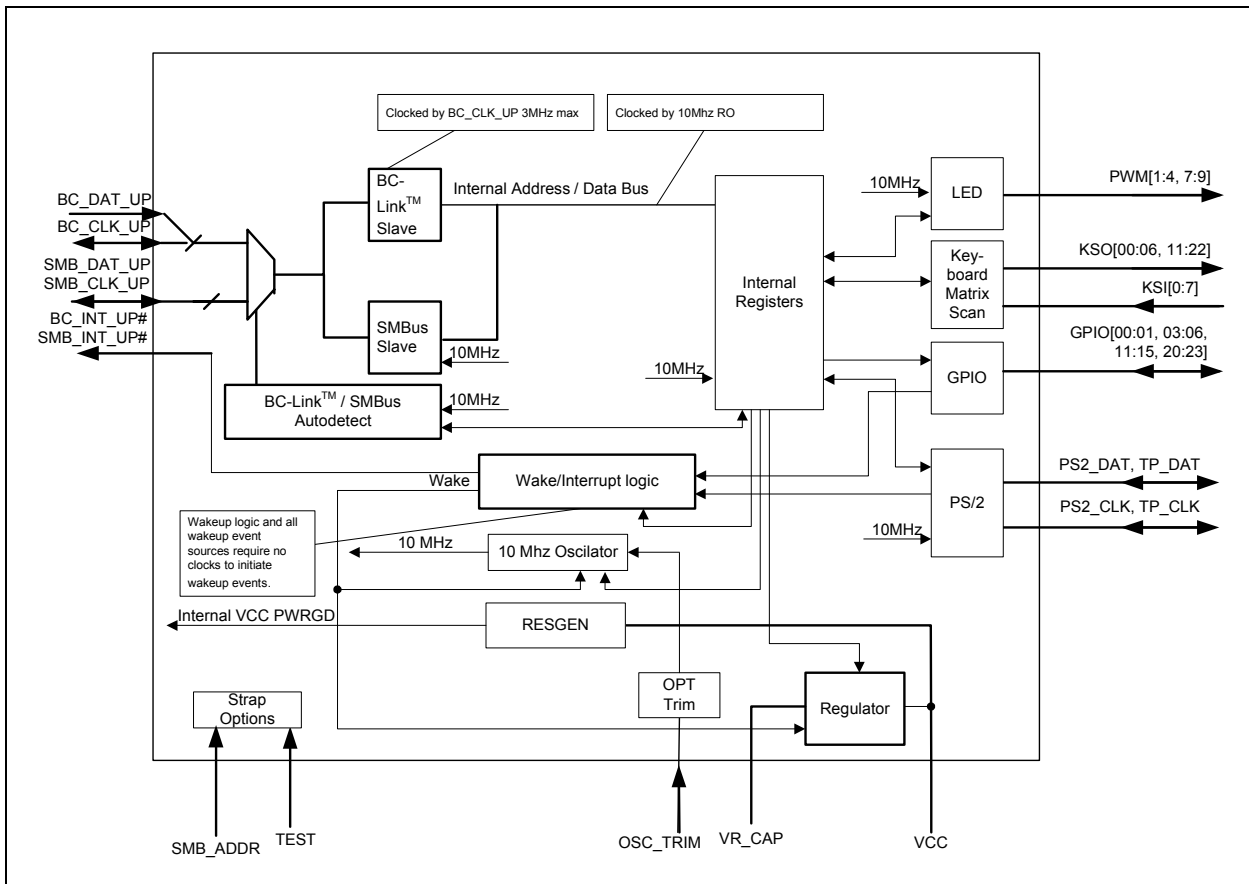
The ECE1117 has a single Power Source VCC and a single digital ground VSS. There are two power domains VCC and VCC_1.8.

See Section 3.0, " Power, Clocks and Resets," on page 22 for additional details about clocks and power.

2.0   PIN CONFIGURATION AND SIGNAL DESCRIPTION

2.1   Package Pin Configuration

FIGURE 2-1:   ECE1117 PACKAGE CONFIGURATION
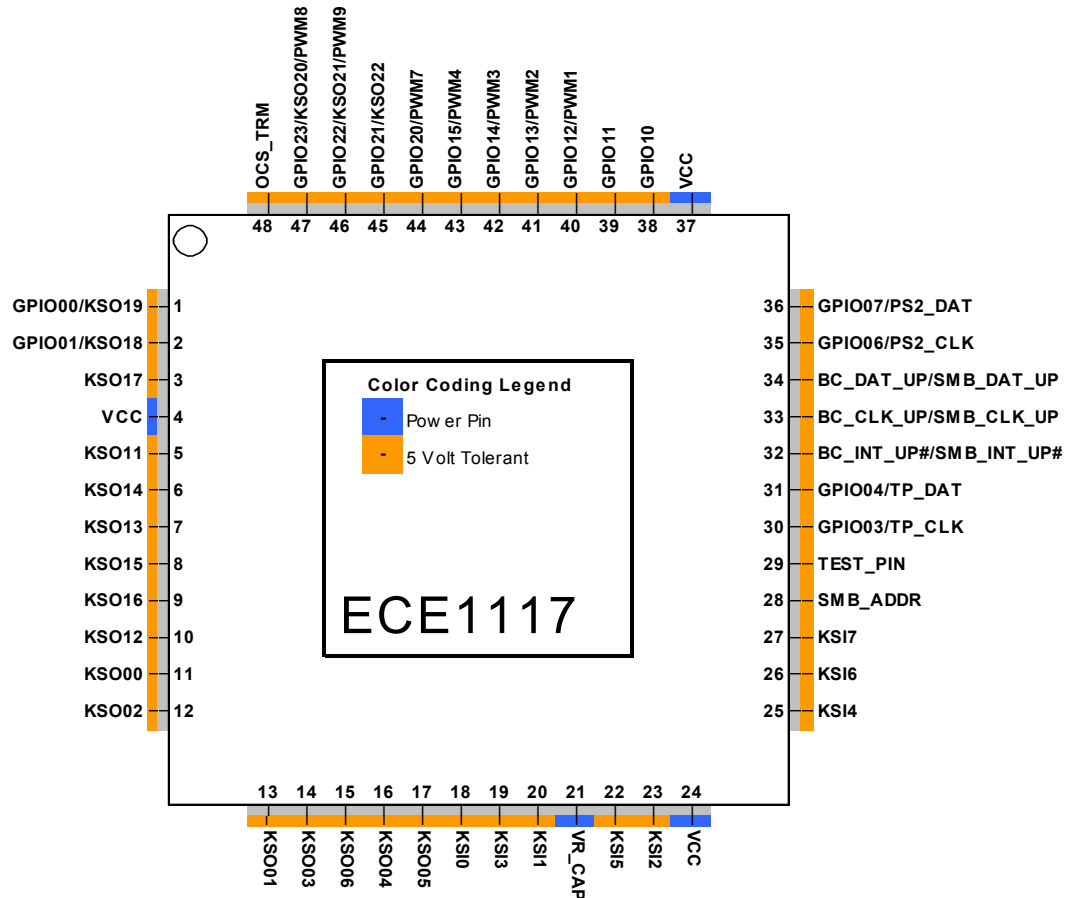
TABLE 2-1:   ECE1117 PIN CONFIGURATION

Pin Number	Pin Name	Pin No	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	GPIO00/KSO19	13	KSO01	25	KSI4	37	VCC
2	GPIO01/KSO18	14	KSO03	26	KSI6	38	GPIO10
3	KSO17	15	KSO06	27	KSI7	39	GPIO11
4	VCC	16	KSO04	28	SMB_ADDR	40	GPIO12/PWM1
5	KSO11	17	KSO05	29	TEST_PIN	41	GPIO13/PWM2
6	KSO14	18	KSI0	30	GPIO03/TP_CLK	42	GPIO14/PWM3
7	KSO13	19	KSI3	31	GPIO04/TP_DAT	43	GPIO15/PWM4
8	KSO15	20	KSI1	32	BC_INT_UP#/SMB_INT_UP#	44	GPIO20/PWM7
9	KSO16	21	VR_CAP	33	BC_CLK_UP/SMB_CLK_UP	45	GPIO21/KSO22
10	KSO12	22	KSI5	34	BC_DAT_UP/SMB_DAT_UP	46	GPIO22/KSO21/PWM9
11	KSO00	23	KSI2	35	GPIO06/PS2_CLK	47	GPIO23/KSO20/PWM8
12	KSO02	24	VCC	36	GPIO07/PS2_DAT	48	OCS_TRM

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2.2   Signal Pin Function Description

2.2.1   BC-LINK™ INTERFACE

TABLE 2-2:   BC-LINK™ INTERFACE

BC-Link Interface			(3 Pins)
Pin Number	Signal Name	Description	Notes
34	BC_DAT_UP	BC-Link Upstream Data	
33	BC_CLK_UP	BC-Link Upstream Clock	
32	BC_INT_UP#	BC-Link Upstream Interrupt	

2.2.2   SMBUS INTERFACE

TABLE 2-3:   SMBUS INTERFACE

SMBus Interface			(4 Pins)
Pin Number	Signal Name	Description	Notes
34	SMB_DAT_UP	SMBus Upstream Data	Note 7
33	SMB_CLK_UP	SMBus Upstream Clock	Note 7
32	SMB_INT_UP#	SMBus Upstream Interrupt	
28	SMB_ADDR	SMBus Address selection pin	

2.2.3   GPIO INTERFACE

TABLE 2-4:   GPIO INTERFACE

GPIO Interface			(16 Pins)
Pin Number	Signal Name	Description	Notes
1	GPIO00	GPIO Interface	
2	GPIO01	GPIO Interface	
30	GPIO03	GPIO Interface	Note 3
31	GPIO04	GPIO Interface	Note 3
35	GPIO06	GPIO Interface	Note 3
36	GPIO07	GPIO Interface	Note 3
38	GPIO10	GPIO Interface	
39	GPIO11	GPIO Interface	
40	GPIO12	GPIO Interface	Note 2
41	GPIO13	GPIO Interface	Note 2
42	GPIO14	GPIO Interface	Note 2
43	GPIO15	GPIO Interface	Note 2
44	GPIO20	GPIO Interface	
45	GPIO21	GPIO Interface	
46	GPIO22	GPIO Interface	
47	GPIO23	GPIO Interface	

2.2.4 KEYBOARD SCAN INTERFACE

TABLE 2-5: KEYBOARD SCAN INTERFACE

Keyboard Scan Interface			(27 Pins)
Pin Number	Signal Name	Description	Notes
18	KSI0		Note 3Note 9
20	KSI1		Note 9
23	KSI2		Note 9
19	KSI3		Note 9
25	KSI4	Keyboard Matrix Scan Inputs	Note 9
22	KSI5		Note 9
26	KSI6		Note 9
27	KSI7		Note 9
11	KSO00		Note 10
13	KSO01		Note 10
12	KSO02		Note 10
14	KSO03		Note 10
16	KSO04		Note 10
17	KSO05		Note 10
15	KSO06		Note 10
5	KSO11		Note 10
10	KSO12		Note 10
7	KSO13	Keyboard Matrix Scan Outputs	Note 10
6	KSO14		Note 10
8	KSO15		Note 10
9	KSO16		Note 10
3	KSO17		Note 10
2	KSO18		Note 11
1	KSO19		Note 11
47	KSO20		Note 11
46	KSO21		Note 11
45	KSO22		Note 11

2.2.5 PS/2 INTERFACE

TABLE 2-6: PS/2 INTERFACE

PS/2 Interface			(4 Pins)
Pin Number	Signal Name	Description	Notes
35	PS2_CLK	PS2 Clock	Note 3Note 12
36	PS2_DAT	PS2 Data	Note 3Note 12
30	TP_CLK	Touch Pad Clock	Note 3Note 12
31	TP_DAT	Touch Pad Data	Note 3Note 12

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2.2.6   LED INTERFACE

TABLE 2-7:   LED INTERFACE

PWM Interface			(7 Pins)
Pin Number	**Signal Name**	**Description**	**Notes**
40	PWM1		Note 2
41	PWM2		Note 2
42	PWM3	LED Interface	Note 2
43	PWM4		Note 2
44	PWM7		
47	PWM8		
46	PWM9		

2.2.7   TEST INTERFACE

TABLE 2-8:   TEST INTERFACE

Test Interface			(3 Pins)
Pin Number	**Signal Name**	**Description**	**Notes**
29	TEST_PIN	Test Pin	Note 5
48	OCS_TRM	Oscillator Trim	Note 6
28	SMB_ADDR	SMBus Address selection pin	

2.2.8   POWER INTERFACE

TABLE 2-9:   POWER INTERFACE

Power Interface			(4 Pins)
Pin Number	**Signal Name**	**Description**	**Notes**
4, 24, 37	VCC	3.3 Volt Power Supply	
Center Pad	VSS	Power Supply Ground	Note 8
21	VR_CAP	Internal Voltage Regulator Output	Note 4

2.3   Pin Signal Function Multiplexing

The following Multiplexing Tables document the Programmable signal pin functions per pin, as well as, programmable buffer type and signal power.

Each Pin, which has a GPIO, has an associated and corresponding GPIO Configuration Register which controls Pin Signal Function Multiplexing, as well as, programmable buffer type, programmable internal pullup & programmable pull-down.

Each pin without a GPIO either provides power or has a single pin signal function; All exceptions to have an explicit note in the multiplexing tables below.

> **Note:** See GPIO Configuration Register on page 48 for register definition and Register Summary Table 1 of 6 on page 35 specific pin defaults Pullup/Pulldown, Open Drain/Pushpull configurations. Also see General Rules for GPIO Configuration Register described in Section 2.3, "Pin Signal Function Multiplexing," on page 8 and Section 2.3.1, "Exceptions to the GPIO Configuration Register Rules," on page 9.

PROGRAMMER'S NOTE: The programmer must insure that all settings in the GPIO Configuration Register are programmed to provide the desired pin behavior.

Detailed Buffer type parameters are provided for the buffer types in the Section 11.2, "DC Electrical Characteristics," on page 69. See Section 2.4, "Notes for the Tables in this Chapter," on page 17 for notes that are referenced in the Pin Multiplexing tables.

2.3.1   EXCEPTIONS TO THE GPIO CONFIGURATION REGISTER RULES

The only exception to the GPIO Configuration Register usage rules is the Keyboard Scan Interface (See Table 2-5 on page 7). Each Keyboard Scan Interface pin utilizes a unrelated GPIO Configuration Register bit to control its pullup. The rest of the bits in the GPIO Configuration Register controls its associated and corresponding GPIO pin.

Each Keyboard Scan Interface pin has a note used throughout this chapter. See Table 2.4, "Notes for the Tables in this Chapter," on page 17.

PROGRAMMER'S NOTE:

- All writes to GPIO01 Configuration Register at BC address 0Bh should keep bit[7] cleared to '0'.
- Do not write to the GPIO Configuration Register for GPIO[02,05,16,17]. These GPIO's do not exist in the part; they default to and should remain inputs, pullup/pulldown disabled.

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TABLE 2-10:   MULTIPLEXING TABLE (1 OF 7)

Pin Number	MUX	Signal	Buffer Type	Signal Power Well	Notes
1	Default: 0	GPIO00	I/O/OD-8 mA	VCC	
1	1	KSO19	O/OD-8 mA	VCC	Note 11
1	2	Reserved	Reserved	Reserved	
1	3	Reserved	Reserved	Reserved	
2	Default: 0	GPIO01	I/O/OD-8 mA	VCC	
2	1	KSO18	O/OD-8 mA	VCC	Note 11
2	2	Reserved	Reserved	Reserved	
2	3	Reserved	Reserved	Reserved	
3	Default: 0	KSO17	OD-8 mA	VCC	Note 10
3	1	Reserved	Reserved	Reserved	
3	2	Reserved	Reserved	Reserved	
3	3	Reserved	Reserved	Reserved	
4		VCC	PWR	PWR	
4					
4					
4					
5	Default: 0	KSO11	OD-8 mA	VCC	Note 10
5	1	Reserved	Reserved	Reserved	
5	2	Reserved	Reserved	Reserved	
5	3	Reserved	Reserved	Reserved	
6	Default: 0	KSO14	OD-8 mA	VCC	Note 10
6	1	Reserved	Reserved	Reserved	
6	2	Reserved	Reserved	Reserved	
6	3	Reserved	Reserved	Reserved	

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TABLE 2-11: MULTIPLEXING TABLE (2 OF 7)

Pin Number	MUX	Signal	Buffer Type	Signal Power Well	Notes
7	Default: 0	KSO13	OD-8 mA	VCC	Note 10
7	1	Reserved	Reserved	Reserved	
7	2	Reserved	Reserved	Reserved	
7	3	Reserved	Reserved	Reserved	
8	Default: 0	KSO15	OD-8 mA	VCC	Note 10
8	1	Reserved	Reserved	Reserved	
8	2	Reserved	Reserved	Reserved	
8	3	Reserved	Reserved	Reserved	
9	Default: 0	KSO16	OD-8 mA	VCC	Note 10
9	1	Reserved	Reserved	VCC	
9	2	Reserved	Reserved	Reserved	
9	3	Reserved	Reserved	Reserved	
10	Default: 0	KSO12	OD-8 mA	VCC	Note 10
10	1	Reserved	Reserved	Reserved	
10	2	Reserved	Reserved	Reserved	
10	3	Reserved	Reserved	Reserved	
11	Default: 0	KSO00	OD-8 mA	VCC	Note 10
11	1	Reserved	Reserved	Reserved	
11	2	Reserved	Reserved	Reserved	
11	3	Reserved	Reserved	Reserved	
12	Default: 0	KSO02	OD-8 mA	VCC	Note 10
12	1	Reserved	Reserved	Reserved	
12	2	Reserved	Reserved	Reserved	
12	3	Reserved	Reserved	Reserved	
13	Default: 0	KSO01	OD-8 mA	VCC	Note 10
13	1	Reserved	Reserved	Reserved	
13	2	Reserved	Reserved	Reserved	
13	3	Reserved	Reserved	Reserved	
14	Default: 0	KSO03	OD-8 mA	VCC	Note 10
14	1	Reserved	Reserved	Reserved	
14	2	Reserved	Reserved	Reserved	
14	3	Reserved	Reserved	Reserved	

TABLE 2-12:   MULTIPLEXING TABLE (3 OF 7)

Pin Number	MUX	Signal	Buffer Type	Signal Power Well	Notes
15	Default: 0	KSO06	OD-8 mA	VCC	Note 10
15	1	Reserved	Reserved	Reserved	
15	2	Reserved	Reserved	Reserved	
15	3	Reserved	Reserved	Reserved	
16	Default: 0	KSO04	OD-8 mA	VCC	Note 10
16	1	Reserved	Reserved	Reserved	
16	2	Reserved	Reserved	Reserved	
16	3	Reserved	Reserved	Reserved	
17	Default: 0	KSO05	OD-8 mA	VCC	Note 10
17	1	Reserved	Reserved	Reserved	
17	2	Reserved	Reserved	Reserved	
17	3	Reserved	Reserved	Reserved	
18	Default: 0	KSI0	I	VCC	Note 3 Note 9
18	1	Reserved	Reserved	Reserved	
18	2	Reserved	Reserved	Reserved	
18	3	Reserved	Reserved	Reserved	
19	Default: 0	KSI3	I	VCC	Note 9
19	1	Reserved	Reserved	Reserved	
19	2	Reserved	Reserved	Reserved	
19	3	Reserved	Reserved	Reserved	
20	Default: 0	KSI1	I	VCC	Note 9
20	1	Reserved	Reserved	Reserved	
20	2	Reserved	Reserved	Reserved	
20	3	Reserved	Reserved	Reserved	

TABLE 2-13:   MULTIPLEXING TABLE (4 OF 7)

Pin Number	MUX	Signal	Buffer Type	Signal Power Well	Notes
21		VR_CAP	PWR	PWR	Note 4
21					
21					
21					
22	Default: 0	KSI5	I	VCC	Note 9
22	1	Reserved	Reserved	Reserved	
22	2	Reserved	Reserved	Reserved	
22	3	Reserved	Reserved	Reserved	
23	Default: 0	KSI2	I	VCC	Note 9
23	1	Reserved	Reserved	Reserved	
23	2	Reserved	Reserved	Reserved	
23	3	Reserved	Reserved	Reserved	
24		VCC	PWR	PWR	
24					
24					
24					
25	Default: 0	KSI4	I	VCC	Note 9
25	1	Reserved	Reserved	Reserved	
25	2	Reserved	Reserved	Reserved	
25	3	Reserved	Reserved	Reserved	
26	Default: 0	KSI6	I	VCC	Note 9
26	1	Reserved	Reserved	Reserved	
26	2	Reserved	Reserved	Reserved	
26	3	Reserved	Reserved	Reserved	
27	Default: 0	KSI7	I	VCC	Note 9
27	1	Reserved	Reserved	Reserved	
27	2	Reserved	Reserved	Reserved	
27	3	Reserved	Reserved	Reserved	
28	Default: 0	SMB_ADDR	I	VCC	
28	1	Reserved	Reserved	VCC	
28	2	Reserved	Reserved	Reserved	
28	3	Reserved	Reserved	Reserved	

TABLE 2-14:   MULTIPLEXING TABLE (5 OF 7)

Pin Number	MUX	Signal	Buffer Type	Signal Power Well	Notes
29	Default: 0	TEST_PIN	I	VCC	Note 5
29	1	Reserved	Reserved	Reserved	
29	2	Reserved	Reserved	Reserved	
29	3	Reserved	Reserved	Reserved	
30	Default: 0	GPIO03	I/O/OD-16 mA	VCC	Note 3
30	1	Reserved	I/O-16 mA	VCC	
30	2	Reserved	I	VCC	
30	3	TP_CLK	I/OD-16 mA	VCC	Note 3 Note 12
31	Default: 0	GPIO04	I/O/OD-16 mA	VCC	Note 3
31	1	Reserved	I/O-16 mA	VCC	
31	2	Reserved	I	VCC	
31	3	TP_DAT	I/OD-16 mA	VCC	Note 3 Note 12
32	Default: 0	BC_INT_UP#	O-16 mA	VCC	
32	1	SMB_INT_UP#	OD-16 mA	VCC	
32	2	Reserved	Reserved	Reserved	
32	3	Reserved	Reserved	Reserved	
33	Default: 0	BC_CLK_UP	I	VCC	
33	1	SMB_CLK_UP	I/OD-16 mA	VCC	Note 7
33	2	Reserved	Reserved	Reserved	
33	3	Reserved	Reserved	Reserved	
34	Default: 0	BC_DAT_UP	IO-16 mA	VCC	
34	1	SMB_DAT_UP	I/OD-16 mA	VCC	Note 7
34	2	Reserved	Reserved	Reserved	
34	3	Reserved	Reserved	Reserved	

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TABLE 2-15:   MULTIPLEXING TABLE (6 OF 7)

Pin Number	MUX	Signal	Buffer Type	Signal Power Well	Notes
35	Default: 0	GPIO06	I/O/OD-16 mA	VCC	Note 3
35	1	Reserved	I/O-16 mA	VCC	
35	2	Reserved	I	VCC	
35	3	PS2_CLK	I/OD-16 mA	VCC	Note 3 Note 12
36	Default: 0	GPIO07	I/O/OD-16 mA	VCC	Note 3
36	1	Reserved	I/O-16 mA	VCC	
36	2	Reserved	I	VCC	
36	3	PS2_DAT	I/OD-16 mA	VCC	Note 3 Note 12
37		VCC	PWR	PWR	
37					
37					
37					
38	Default: 0	GPIO10	I/O/OD-16 mA	VCC	
38	1	Reserved	Reserved	Reserved	
38	2	Reserved	Reserved	Reserved	
38	3	Reserved	Reserved	Reserved	
39	Default: 0	GPIO11	I/O/OD-8 mA	VCC	
39	1	Reserved	Reserved	Reserved	
39	2	Reserved	Reserved	Reserved	
39	3	Reserved	Reserved	Reserved	
40	Default: 0	GPIO12	I/O/OD-12/20 mA	VCC	Note 2
40	1	PWM1	O/OD-12/20 mA	VCC	Note 2
40	2	Reserved	Reserved	Reserved	
40	3	Reserved	Reserved	Reserved	
41	Default: 0	GPIO13	I/O/OD-12/20 mA	VCC	Note 2
41	1	PWM2	O/OD-12/20 mA	VCC	Note 2
41	2	Reserved	Reserved	Reserved	
41	3	Reserved	Reserved	Reserved	
42	Default: 0	GPIO14	I/O/OD-12/20 mA	VCC	Note 2
42	1	PWM3	O/OD-12/20 mA	VCC	Note 2
42	2	Reserved	Reserved	Reserved	
42	3	Reserved	Reserved	Reserved	

TABLE 2-16:   MULTIPLEXING TABLE (7 OF 7)

Pin Number	MUX	Signal	Buffer Type	Signal Power Well	Notes
43	Default: 0	GPIO15	I/O/OD-12/20 mA	VCC	Note 2
43	1	PWM4	O/OD-12/20 mA	VCC	Note 2
43	2	Reserved	I	VCC	
43	3	Reserved	I	VCC	
44	Default: 0	GPIO20	I/O/OD-8 mA	VCC	
44	1	PWM7	O/OD-8 mA	VCC	
44	2	Reserved	Reserved	Reserved	
44	3	Reserved	Reserved	Reserved	
45	Default: 0	GPIO21	I/O/OD-8 mA	VCC	
45	1	KSO22	O/OD-8 mA	VCC	Note 11
45	2	Reserved	Reserved	VCC	
45	3	Reserved	Reserved	Reserved	
46	Default: 0	GPIO22	I/O/OD-8 mA	VCC	
46	1	KSO21	O/OD-8 mA	VCC	Note 11
46	2	PWM9	O/OD-8 mA	VCC	
46	3	Reserved	Reserved	Reserved	
47	Default: 0	GPIO23	I/O/OD-8 mA	VCC	
47	1	KSO20	O/OD-8 mA	VCC	Note 11
47	2	PWM8	O/OD-8 mA	VCC	
47	3	Reserved	Reserved	Reserved	
48	Default: 0	OCS_TRM	special	VCC	Note 6
48	1	Reserved	Reserved	Reserved	
48	2	Reserved	Reserved	Reserved	
48	3	Reserved	Reserved	Reserved	

2.4   Notes for the Tables in this Chapter

TABLE 2-17:   NOTES FOR THE TABLES IN THIS CHAPTER

Note 1	Buffer modes are described per signal function. On multiplexed pins buffer modes are separated by a slash "/"; e.g., a pin with two multiplexed functions where the primary function is an input and the secondary function is an 8mA bi-directional driver is represented as "I/IO-8". Buffer modes in parentheses represent multiple buffer modes for a single pin function. The number following the "-" represents the balanced output sink/source capability of the buffer in milliamps.
Note 2	This pin can sink 20ma when selected as an open drain buffer. This pin can source or sink 12ma when selected as a push-pull buffer. This pin has an internal pullup and pulldown impedance characteristics defined in the DC Electrical Characteristics section labed as following parameters: "Pull Down Impedance for I/O/OD 12/20mA buffer type (Used only where noted)" "Pull UP Impedance for I/O/OD 12/20mA buffer type (Used only where noted)" Although the Buffer Strength on this pin is available for all signal pin functions. It was specifically incorporated for the PWM signal pin function.
Note 3	This pin has an programmable internal pullup with impedance of 5.0 ± 50% KOHMS. This pullup is controlled by the pin's GPIO Configuration Register. Although the internal programmable pullup on this pin is available for all signal pin functions, it was specifically incorporated for the PS/2 signal pin function. Suitability for other purposes should be evaluated by the system designer.
Note 4	Capacitor Connection for Internal Voltage Regulator (4.7uF ±20%, ESR 2 Ohms, max.). A series resistor is required on VR_CAP. See PCB Layout Guide for the recommended value.
Note 5	This pin has a week internal pull-down which disables test function. It may be left unconnected in the system. In an environment that has the potential for noise, like a cabled daughter-board, it is suggested that this pin be pulled to GND through a 1K resistor. In an environment less noisy, it can be left unconnected. It is also recommended that this pin go to a test point so ICT can pull it high for XNOR test mode.
Note 6	Connect this pin to VSS in the system.
Note 7	This pin is connected to the internal SMB Slave and the SMB-Switch.
Note 8	The VSS pad is the exposed center pad on the bottom of the QFN and SQFN packages.

Note 9	The internal pullup for the KSI[7:0] pins are all enabled by GPIO00 Configuration Register-bit[7]. Bit[6] continues to control selection between KSO19 and GPIO00 pin signal function. The BC address for this register is 0Ah.
	Bit[7] definition is as follows:
	    '0' (default) = internal pullup resistor is enabled.
	    '1' = internal pullup is disabled
	The GPIO00 Configuration Register-bit[7] has the opposite sense of all other pullup bit definitions.

Note 10	The internal pullup for the KSO[17:11, 6:0] pins are all enabled by GPIO10 Configuration Register-bit[7]. The BC address for this register is 12h.
	Bit[7] definition is as follows:
	    '0' (default) = internal pullup is disabled
	    '1' = internal pullup resistor is enabled.
	The GPIO10 Configuration Register-bit[7] has the same sense of all other Pullup bit definitions.

Note 11	The KSO[22:18] signal pin functions are multiplexed with GPIO's and obey the general rules for use of GPIO Configuration Registers. Specifically, their pullup are controlled by their associated and conrresponding GPIO Configuration Register.
Note 12	The pullup resister must always be powered by the same source as the PS/2 device signals. The internal pullup may be used (see Note 3) or an external pullup resister. The PS/2 Wake Interface is only active when the PS/2 signals are active.

2.5   Strapping Options

2.5.1   SMB_ADDR STRAPPING OPTION

The SMB_ADDR pin selects the POR SMBus slave address of the ECE1117.The SMB_ADDR pin affects the SMBus Slave Address Register on page 44 and the pin and register together can dynamically change the SMBus address.

2.6   TEST_PIN strapping option

The TEST_PIN pin selects entry into the XNOR Chain Test Mode on page 18.

2.6.1   RESGEN INDICATION ON TEST_PIN PIN

The TEST_PIN pin provides an indication that the VCCGD signal transitioned from '0' to '1'. (See FIGURE 3-2: Power-Up Timing on page 23.) The TEST_PIN pin has an internal weak pull-down which is always enabled. The TEST_PIN buffer is driven as an open drain output during the t_{DLY2} in FIGURE 3-2: Power-Up Timing on page 23. After the VCCGD transitions to '1', the TEST_PIN buffer is tri-stated. The TEST_PIN input is examined after nDLY_RST transitioned to a '1'. for all the following tests:

To observe the RESGEN Indication on TEST_PIN pin, a strong external pullup should be connected. Observing the transition to high indicates the RESGEN has come out of reset. Timing on the pin is not ensured.

2.7   XNOR Chain Test Mode

An XNOR Chain test structure is in to the ECE1117 to allow users to confirm that all pins are in contact with the Circuit assembly (Figure 2-2).

The XNOR Chain test structure must be activated to perform these tests. When the XNOR Chain is activated, the ECE1117 pin functions are disconnected from the device pins, which all become input pins except for one output pin at the end of XNOR Chain.

The tests that are performed when the XNOR Chain test structure is activated require the board-level test hardware to control the device pins and observe the results at the XNOR Chain output pin.

2.7.1   PINS IN XNOR CHAIN STRUCTURE

All pins are inputs into the XNOR Chain with the exception of the following pins:

- TEST_PIN
- SMB_ADDR
- BC_INT_UP#/SMB_INT_UP# (this is the XNOR Chain output)
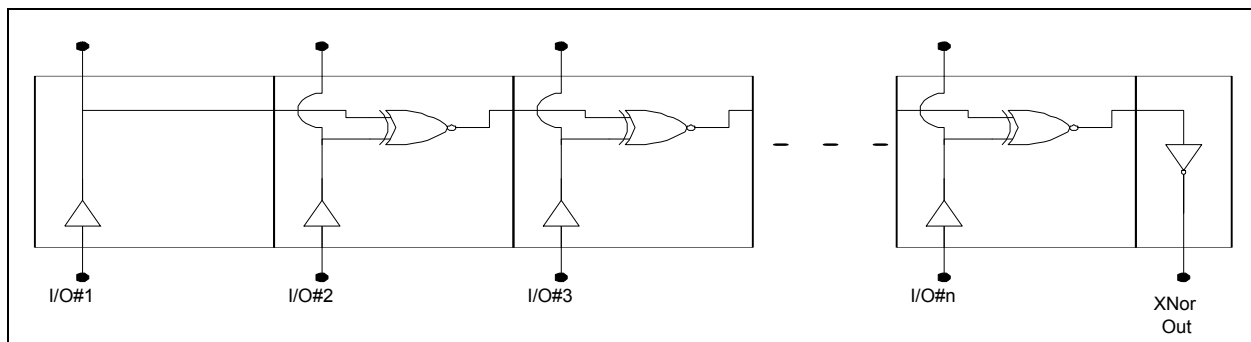- OSC_TRIM

2.7.2   ENTERING AND EXITING THE XNOR CHAIN

The XNOR Chain test is entered by setting TEST_PIN to 1 while SMB_ADDR is 0.

When activated, the test mode allows one single input pin, when switched, to toggle the BC_INT_UP#/SMB_INT_UP# output.

The XNOR Chain is exited by setting TEST_PIN to 0, independent of the value of SMB_ADDR.

FIGURE 2-2:   XNOR CHAIN TEST STRUCTURE

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2.8   Package Outline Drawings

FIGURE 2-3:   48-PIN QFN PACKAGE, 7 X 7MM BODY, 0.5MM PITCH

REVISION HISTORY

REVISION	DESCRIPTION	DATE	RELEASED BY
A	INITIAL RELEASE	7/16/04	S.KILIEV
B	DELETE THE "PRELIMINARY" SIGN	11/23/04	S.KILIEV
C	3-D VIEW ADDED. D2/E2 WAS 1.25-5.80 NOW - SEE TABLE. L(MAX) WAS 0.75 NOW IS 0.50	7/14/05	S.KILIEV
D	PCB FOOTPRINT AND EMC4001 IN D2/E2 TABLE ADDED	2/23/06	S.KILIEV
E	NEW EXPOSED PAD ADDED FOR EMC4002 DEVICE	4/24/07	S.KILIEV
F	NEW EXPOSED PAD ADDED FOR OS81110 DEVICE	5/17/07	S.KILIEV
G	ADDED PAGE 2of2. UPDATED APP NOTES. D2/E2 TOLERANCE FROM ±0.15 TO ±0.10 mm	2/3/09	S.KILIEV

COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.70	0.85	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A2	-	-	0.90	-	MOLD CAP THICKNESS
D/E	6.85	7.00	7.15	-	X/Y BODY SIZE
D1/E1	6.55	6.75	6.95	-	X/Y MOLD CAP SIZE
D2/E2	4.00	4.10	4.20	-	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	-	TERMINAL WIDTH
K	0.95	-	-	2	CENTER PAD TO PIN CLEARANCE
e		0.50 BSC		-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging

PACKAGE DATA
48 QFN-4104, 7x7mm BODY, 0.5mm PITCH, 4.1x4.1mm EXPOSED PAD, 0.4mm LEAD LENGTH
Package Outline Drawing (POD)

DWG NUMBER	48QFN-4104-7x7B
STD COMPLIANCE	JEDEC: MO-220
SCALE	1:1
SHEET	1 OF 2
REV	G

TITLE

DRAWN — 6/15/04
CHECKED — 7/14/04
APPROVED S.KILIEV 7/16/04

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL   ANGULAR
X.X   ±0.1   ±1°
X.XX   ±0.05
X.XXX ±0.025
INTERPRET DIM AND TOL PER ASME Y14.5M – 1994

MATERIAL

FINISH

PRINT WITH "SCALE TO FIT"
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

BOTTOM VIEW

TOP VIEW

SIDE VIEW

3-D VIEWS

FIGURE 2-3: 48-PIN QFN PACKAGE, 7 X 7MM BODY, 0.5MM PITCH (CONTINUED)

REVISION HISTORY

REV	DESCRIPTION	DATE	RELEASED BY
G	ADDED PAGE 2of2, UPDATED APP NOTES AND D2/E2 TOLERANCE FROM ±0.15 TO ±0.10 mm	2/3/09	S.K.ILIEV

LAND PATTERN DIMENSIONS

SYMBOL	MIN	NOM	MAX
GD/GE	6.00	-	6.10
GDs/GEs	6.05	-	-
D2'/E2'	-	4.10	-
Pad: X	-	0.28	0.28
Stencil: Xs	-	0.23	0.25
Pad: Y	-	0.69	0.69
Stencil: Ys	-	0.62	0.64
e		0.50	

SMT APPLICATION NOTES

1. THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY.
2. THE LAND PATTERN CORRESPONDING TO THE PACKAGE EXPOSED PAD (IN THE CENTER) CAN BE LARGER, AND WITH DIFFERENT SHAPE THAN THE EXPOSED PAD ON THE PACKAGE. HOWEVER, THE SOLDERABLE AREA, AS DEFINED BY THE SOLDER MASK (SMD), OR NON-SOLDER MASK DEFINED (NSMD), SHOULD BE AS SHOWN FOR THE BEST THERMAL & ELECTRICAL PERFORMANCE.
3. MAXIMUM THERMAL AND ELECTRICAL PERFORMANCE IS ACHIEVED WHEN AN ARRAY OF SOLID VIAS IS INCORPORATED IN THE CENTER LAND PATTERN. (See Options 1 & 2)
4. THE VIAS SHOULD BE AT 0.8 to 1.2MM PITCH WITH 0.30 TO 0.40MM DIAMETER, AND 1 OZ COPPER VIA BARREL PLATING.
5. NON SOLDER MASK DEFINED (NSMD) PAD DESIGN IS RECOMMENDED FOR PERIMETER LANDS.
6. A LASER-CUT STAINLESS STEEL STENCIL IS RECOMMENDED WITH ELECTRO POLISHED TRAPEZOIDAL WALLS. THE RECOMMENDED STENCIL THICKNESS IS 0.125 mm FOR PITCHES 0.4 and 0.5 mm.
7. RECOMMENDED STENCIL AREA & ASPECT RATIOS ARE 0.66 & 1.5 (MIN) RESPECTIVELY.
8. RECOMMENDED STENCIL APERTURES ARE AS SHOWN.
9. IT IS RECOMMENDED TO USE "NO-CLEAN", TYPE 3 SOLDER PASTE.
10. THE REFLOW PROFILE DEPENDS ON THE EXACT SOLDER PASTE USED AND THE GIVEN BOARD DETAILS, SUCH AS GEOMETRY, COMPONENTS ETC.

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL ANGULAR
X.X ±0.1 ±1°
X.XX ±0.05
X.XXX ±0.025
INTERPRET DIM AND TOL PER ASME Y14.5M - 1994

	NAME	DATE
DRAWN	-	2/3/09
CHECKED	-	2/3/09
APPROVED	S.K.ILIEV	2/3/09

MATERIAL -
FINISH -
PRINT WITH "SCALE TO FIT"
DO NOT SCALE DRAWING

TITLE PACKAGE DATA
48 QFN-4104, 7x7mm BODY, 0.5mm PITCH, 4.1x4.1mm EXPOSED PAD, 0.4mm LEAD LENGTH
Application Notes

DWG # 48QFN-4104-7x7B	REV G
STD COMPLIANCE -	SHEET
SCALE 1:1	2 OF 2

PCB LAND PATTERN

STENCIL

SEE DETAIL "A" FOR STENCIL PERIMETER PAD

SEE DETAIL "A" FOR PERIMETER PAD AND SOLDER MASK

SEE DETAIL "B" FOR CENTER PAD STENCIL OPENINGS

SEE DETAIL "B" FOR CENTER PAD DESIGN (EXPOSED SOLDERABLE COPPER AREA)

DETAIL "A"
STENCIL OPENING - PERIMETER LANDS

SOLDER MASK
CLEARANCE B/N PAD & SM 0.060 - 0.075
0.025 (MIN)
0.5
0.075 (MIN)
FULL RADIUS IS OPTIONAL
0.1mm (MIN)

DETAIL "B"
THERMAL VIAS and STENCIL OPENING - CENTER PAD

OPTION 1 (NON-PLUGGED THERMAL VIAS)
Thermal Vias: Ø0.30mm, 5x5 Matrix @ 0.90mm Pitch
Stencil Openings: Ø0.55-0.65mm 4x4 Matrix

OPTION 3 (PLUGGED THERMAL VIAS)
Thermal Vias: Ø0.30mm, 5x5 Matrix @ 0.90mm Pitch
Stencil Openings: 0.82x0.82mm (MAX) 4x4 Matrix
0.2+0.3mm

FIGURE 2-4: 48-PIN SQFN PACKAGE, 7 X 7MM BODY, 0.5MM PITCH

REVISION HISTORY

REVISION	DESCRIPTION	DATE	RELEASED BY
A	INITIAL RELEASE	1/17/2012	HC
B	A(min) from 0.70 to 0.80. A(nom) from 0.85 to 0.90. Added K(nom)	6/18/2012	SKI

3-D VIEWS

COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.90	1.00	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
D/E	6.90	7.00	7.10	-	X/Y BODY SIZE
D2/E2	4.00	4.10	4.20	4	X/Y EXPOSED PAD SIZE
L	0.30	0.40	0.50	-	TERMINAL LENGTH
b	0.18	0.25	0.30	2, 4	TERMINAL WIDTH
K	0.95	1.05	-	-	CENTER PAD TO PIN CLEARANCE
ccc	-	-	0.08	4	COPLANARITY
e		0.50 BSC		-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.
4. COPLANARITY ZONE APPLIES TO EXPOSED PAD AND TERMINALS.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS AND TOLERANCES ARE:
DECIMAL
X.X ±0.1
X.XX ±0.05
X.XXX ±0.025
INTERPRET DIM AND TOL PER ASME Y14.5M - 1994

MATERIAL -
FINISH -

THIRD ANGLE PROJECTION

Note: For the most current package drawings, see the Microchip Packaging Specification at http://www.microchip.com/packaging

PRINT WITH "SCALE TO FIT" DO NOT SCALE DRAWING

TITLE PACKAGE OUTLINE
48 SQFN, 7x7mm BODY, 0.5mm PITCH, 4.1x4.1mm EXPOSED PAD, 0.4mm LEAD LENGTH

	NAME	DATE
DRAWN	-	1/17/12
CHECKED	-	1/17/12
APPROVED	H. CABALLERO	1/17/12

DWG NUMBER 48SQFN-4104-7x7B   REV B

SCALE 1:1   STD COMPLIANCE JEDEC: MO-220   SHEET 1 OF 1

TOP VIEW

BOTTOM VIEW

TERMINAL #1 IDENTIFIER AREA (D/2 X E/2)
EXPOSED PAD
48 X L
TERMINAL #1 IDENTIFIER AREA (D/2 X E 1/2)

SIDE VIEW

PCB LAND PATTERN

LAND PATTERN DIMENSIONS

SYMBOL	MIN	NOM	MAX
GD/GE	6.00		6.10
D2'/E2'		4.10	
X		0.28	0.28
Y		0.70	
e		0.50	

FULL RADIUS IS OPTIONAL

THE USER MAY MODIFY THE PCB LAND PATTERN DIMENSIONS BASED ON THEIR EXPERIENCE AND/OR PROCESS CAPABILITY

ECE1117

3.0   POWER, CLOCKS AND RESETS

3.1   General Description

The Power, Clocks and Resets chapter includes descriptions of the ECE1117 Clocks Sources and Power and Resets Interfaces. The Power and Resets includes a description the internal reset and descriptions of an internal 1.8V Regulator.

The Power Configuration, Clock Generator and Reset circuits have the following features:

Clocks Sources

• Three Asynchronous Clock Sources: 10MHz Clock, BC_CLK, SMB_CLK and two independent PS2_CLK clock inputs.
• 10MHz Clock Ring Oscillator frequency accuracy is 10MHz ± 5%.

Power and Resets

• Power-Up Sequence Definition.
• 1.8V Regulator.
• VCC Reset Signaling (VCCGD, nSYS_RST, nDLY_RST).

3.2   Clocks Sources

3.2.1   10MHZ CLOCK

The source of the 10MHz Clock is a Ring Oscillator. This 10 MHz Ring Oscillator frequency accuracy is 10Mhz ± 5%. The 10MHz Clock distribution is disabled during the SYSTEM LIGHT SLEEP and the Ring Oscillator is disabled during SYSTEM DEEP SLEEP. At VCC POR the 10MHz Clock distribution is enabled. See Section 4.0, "Power Management Interface," on page 26.

3.2.2   BC_CLK

The BC_CLK_UP is an independent clock input to the BC-Link Slave.

3.2.3   SMB_CLK

The SMB_CLK_UP is an independent clock input to the SMB Slave.

3.2.4   PS2_CLK

Two independent clocks drive the PS/2 protocol: TP_CLK and PS2_CLK. Each PS2_CLK input drives a separate PS/2 block.

3.3   Power and Resets

The Power and Reset Logic includes the following blocks:

• 1.8VDC-50ma Regulator
• Power-on-Reset (POR)
• POR Control Register

TABLE 3-1:   POWER AND RESETS SIGNAL LIST

SIGNAL NAME	DIRECTION	DESCRIPTION
10MHz Clock	Input	Ring Oscillator Clock
REG_SUSPEND	Input	Places Regulator into a low power state
VCCGD	Output	Asynchronous 1.8 VDC good signal
nSYS_RST	Output	Synchronous 1.8 VDC good signal
nDLY_RST	Output	Delayed synchronous 1.8 VDC good signal
VCC	Power Input	3.3 Volt power
VCC_1.8	Power Output	1.8 Volt power

FIGURE 3-1: **POWER AND RESETS BLOCK DIAGRAM**
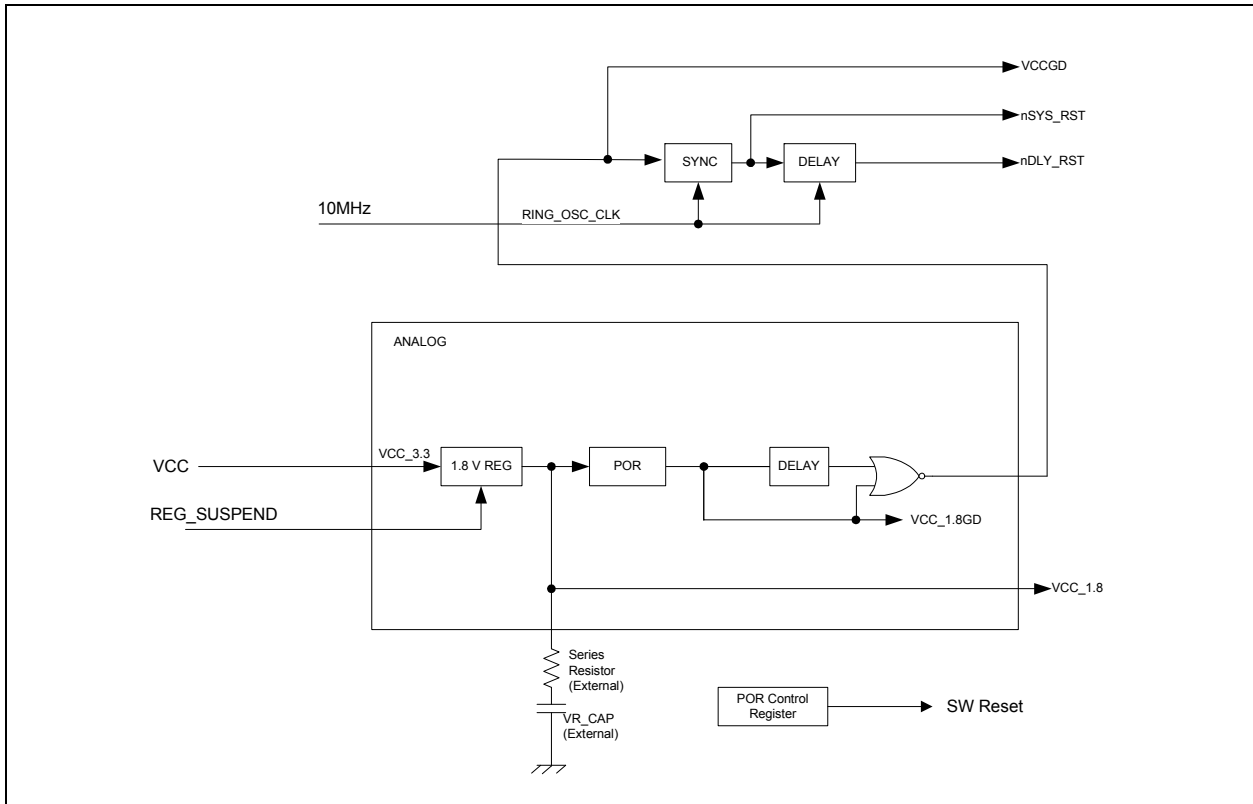
FIGURE 3-2: **POWER-UP TIMING**
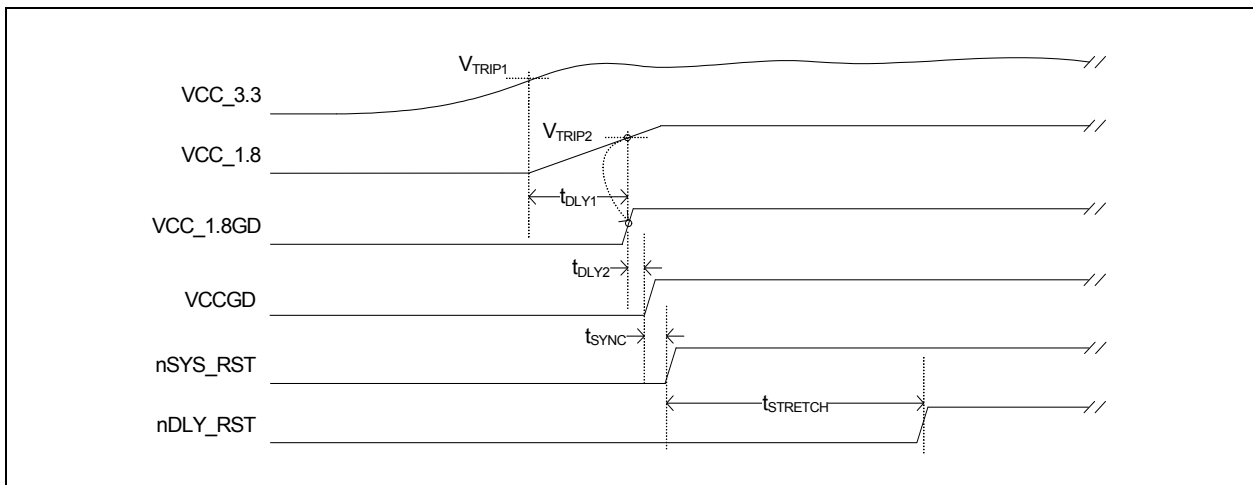
TABLE 3-2: POWER-UP TIMING

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Voltage Trip Level (VCC_3.3)	V_{TRIP1}		2.4		V	
Voltage Trip Level (VCC_1.8)	V_{TRIP2}	0.9	1.2	1.4	V	
VCC_1.8GD Delay Time	t_{DLY1}		70		us	
VCCGD Delay Time	t_{DLY2}		200		ns	
nSYS_RST Delay Time	t_{SYNC}	2	–	3	10 MHz Ring Oscillator Clocks	Note 3-1
nDLY_RST Delay Time	$t_{STRETCH}$	0.5	1	2	ms	Note 3-1

Note 3-1 This interval is determined using a Fixed Clock Domain from the 10 MHz Ring Oscillator.

FIGURE 3-3: POWER-DOWN TIMING
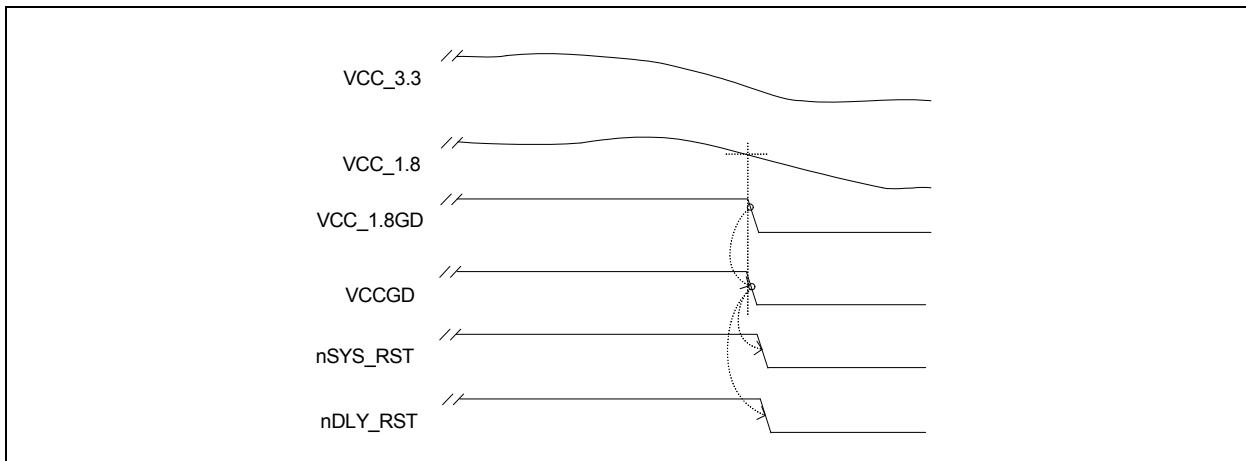
3.3.1 POR CONTROL REGISTER

BUS OFFSET	D0h					8-bit	SIZE	
POWER	VCC					00h	nDLY_RST DEFAULT	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	TEST	POR	TEST					

TEST

All writes to this register must clear these bits to '0', otherwise undesirable result may occur.

POR

After a powerup sequence, two writes to this register are required: to set this bit to a '1' and then immediately clear this bit to a '0'. This bit provides a reset to internal circuitry.

> 0 normal operation
> 1 circuity reset

PROGRAMMER'S NOTE: After a powerup sequence, two writes to the POR Control Register on page 24 are required to set and then clear the POR bit.

3.3.2   1.8V REGULATOR

The 1.8V Regulator generates the ECE1117 core power well.   As illustrated in FIGURE 3-1: Power and Resets Block Diagram on page 23, the input to the 1.8V Regulator is VCC, the output is VCC_1.8 (see also Table 3-1).

3.3.2.1   VREG Suspend

To conserve power, the output of the internal 1.8 V Regulator (VREG) can be placed in suspend mode as defined in the System Deepest Sleep State as defined in Table 4-2, "Low Power Sleep States," on page 27.   When the VREG is placed in suspend, the current the VREG consumes is reduced.

4.0 POWER MANAGEMENT INTERFACE

4.1 General Description

The Power Management Interface chapter includes descriptions of the ECE1117 Power Management States, Wake-up Interface, and Interrupt Interface.

4.2 Power Management States

Table 4-2 on page 27 describes the four power management states in the ECE1117.

The FULL POWER State is default on VCC POR.

Writes to the Power Management Register on page 28 places the ECE1117-Power Management Interface into the PREPARING SYSTEM SLEEP State.

When clocks are no longer required in the ECE1117, then the ECE1117-Power Management Interface transitions from PREPARING SYSTEM SLEEP to either SYSTEM LIGHT SLEEP or SYSTEM DEEP SLEEP.

Any enabled wake event causes the ECE1117-Power Management Interface to transition for either SYSTEM LIGHT SLEEP or SYSTEM DEEP SLEEP to the FULL POWER state.

FIGURE 4-1: POWER MANAGEMENT TRANSITION TIMING
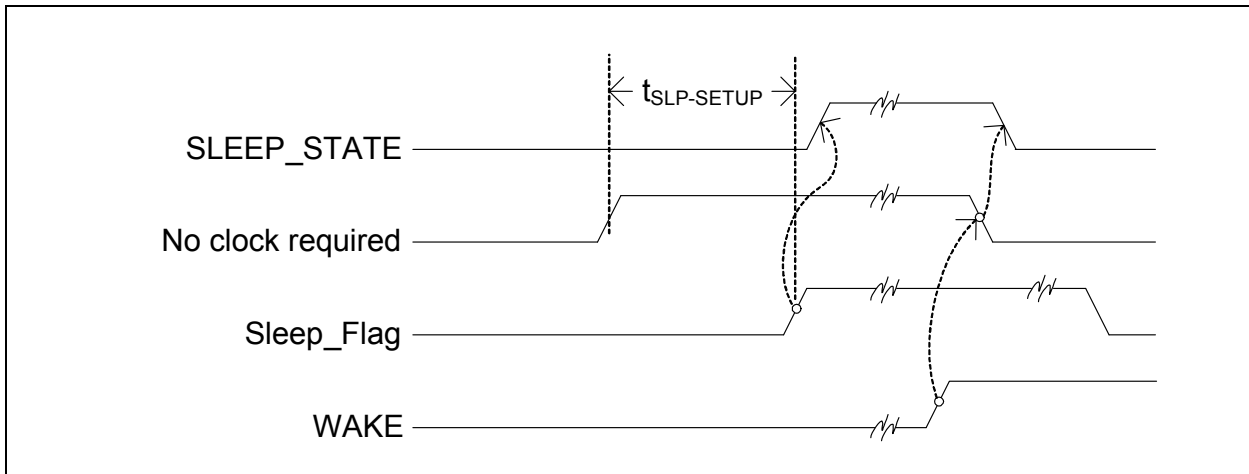
TABLE 4-1: POWER MANAGEMENT INTERFACE TIMING PARAMETERS

PARAMETERS	SYMBOL	MIN	TYP	MAX	UNITS
System Sleep Setup Time	$t_{SLP-SETUP}$	1	–	–	10MHz Clock

TABLE 4-2:   LOW POWER SLEEP STATES

POWER STATES	CLOCK REQUIRED STATUS (SEE Section 4.2.1)	Power Management Register			DESCRIPTION
		10MHZ_-Suspend_EN	VREG_Sus-pend_EN	SLEEP_REQUEST	
FULL POWER	X	X	X	0	The system is running and no pending request for entry into a low power state
	X	0	X	1	The SLEEP_REQUEST bit is set to '1' but the 10MHZ_Suspend_EN bit is cleared to '0'; therefore, the system is running and no pending request for entry into a low power state.
PREPARING SYSTEM SLEEP	Some blocks require a clock.	1	X	1	Both the SLEEP_REQUEST bit and but the 10MHZ_Suspend_EN bit are set to '1'; therefore, a request for entry into a low power state is pending. However, some blocks still require clocks; therefore, the system is running.
SYSTEM LIGHT SLEEP	No blocks require a clock.	1	0	1	Both the SLEEP_REQUEST bit and the 10MHZ_Suspend_EN bit are set to '1'and no blocks require clocks; therefore, the 10MHz Clock Distribution is disabled.
SYSTEM DEEP SLEEP	No blocks require a clock.	1	1	1	The SLEEP_REQUEST bit and both the 10MHZ_Suspend_EN bit and the VREG_Suspend_EN are set to '1'and no blocks require clocks; therefore, 10MHz Clock Distribution is disabled, the 10Mhz Ring Oscillator is turned off and the Voltage Regulator is placed in suspend.

4.2.1   10MHZ CLOCK REQUIREMENTS FOR BLOCKS

The following blocks require clocks derived from the 10MHz Clock and therefore generate a clock required output to the Sleep logic:

• BC-Link/SMBus Autodetect - This block always requires the 10MHz Clock when enabled

• SMBus Slave - This block always requires the 10MHz Clock when enabled -See Section 4.2.1.2 on page 28.

• PS/2 block (x2) - This block always requires the 10MHz Clock when enabled

• LED (x7) -This block always requires the 10MHz Clock when enabled

> **Note 4-1**   The ECE1117 can enter sleep while a LED is configured to fully off or fully on.

• BC-Link transaction Decode - See Section 4.2.1.1 on page 27.

The following blocks use the 10MHz Clock but depend on wake logic or register access and therefore do not need to generate clock required output to the sleep logic:

• GPIO

• Interrupt

• Wake-up events are generated without clocks. For interrupts which are also wake-up events, the interrupt event (edge) is held until 10MHz Clocks is available to clock the value into the interrupt source register.

4.2.1.1   BC-Link™ transaction Decode - Auto-Sleep Mode

The BC-Link Slave does not require the 10MHz Clock to run the BC-Link protocol for BC-Link Switch. However, when an internal addresses is decoded, a narrow window of 10MHz Clocks is required to complete each BC-Link transaction. This 10MHz Clock window of clocks is required only if the destination of the transaction is internal.

The Auto-Sleep mode is controlled by the AUTO_SLEEP bit in the Power Management Register on page 28. Auto-Sleep mode is disabled by default. When disabled an additional BC-Link transaction is required to write to the Power Management Register in order to re-enter a Low Power ECE1117-Power Management Interface sleep state.

4.2.1.2 SMBUS transaction Decode - Auto-Sleep Mode

The SMBUS Slave requires the 10MHz Clock to run the SMBus protocol transfer through the SMBus Switch. In order to decode an internal addresses, the internal SMBus Slave requires a narrow window of 10MHz Clocks to complete each transaction. This 10MHz Clock window of clocks is required for all transactions of internal destination.

The Auto-Sleep mode is controlled by the AUTO_SLEEP bit in the Power Management Register on page 28. Auto-Sleep mode is disabled by default. When disabled an additional SMBus transaction is required to write to the Power Management Register in order to re-enter a Low Power ECE1117-Power Management Interface sleep state.

4.2.2 POWER MANAGEMENT REGISTER

TABLE 4-3:   POWER MANAGEMENT REGISTER

BUS OFFSET	F1h						8-bit	**SIZE**
POWER	VCC						00h	nDLY_RST **DEFAULT**
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved				AUTO_S LEEP	VREG_ Suspend _EN	10MHZ_S uspend_E N	SLEEP_R EQUEST

SLEEP_REQUEST

Writing a '1' to this bit requests entry into the ECE1117 low power mode. Writing a '0' to this bit rescinds the request to enter low power mode.

This bit defaults to '0' and is autonomously cleared to '0' when a Wake Event occurs during low power mode except when the AUTO_SLEEP bit is set to '1' and a BC-Link or SMBus transaction causes a special wake-up event.

See AUTO_SLEEP bit in this register, Section 4.2.1.1, "BC-Link™ transaction Decode - Auto-Sleep Mode," on page 27, and Section 4.2.1.2, "SMBUS transaction Decode - Auto-Sleep Mode," on page 28.

10MHZ_Suspend_EN

When this bit is set to '1' a pending sleep request will either disable the 10MHz clock distribution or both disable the 10MHz clock distribution and disable the 10MHz Ring Oscillator depending other bits in the Power Management Register. See Table 4-2, "Low Power Sleep States," on page 27.

When this bit is cleared to '0', the system will stay in Full Power state in Table 4-2.

VREG_Suspend_EN

When this bit is set to '1' a pending sleep request will suspend the VREG depending other bits in the Power Management Register. See Table 4-2, "Low Power Sleep States," on page 27 and Section 3.3.2.1, "VREG Suspend," on page 25.

When this bit is set to '0' the VREG is capable of outputting the maximum current.

AUTO_SLEEP

When the AUTO_SLEEP bit is set to '1', a BC-Link or SMBus transaction causes a special wake-up event which allows a narrow window of 10MHz Clocks to complete the transaction. Then the ECE1117-Power Management Interface will autonomously re-enter sleep. The SLEEP_REQUEST will not change state.

When the AUTO_SLEEP bit is cleared to '0', the BC-Link or SMBus transactions causes a normal wake-up the event which leaves the 10MHz Clock running and autonomously clears the SLEEP_REQUEST to '0'.

4.3 Wake-up Interface

Wake-up events are interrupts event which are generated with the 10MHz Clock Distribution off. Table 4-4 and FIGURE 4-2: Wakeup/Interrupt Routing on page 31. Figure 3-1 The "Any Wake-up" event output is routed to wake input illustrated in FIGURE 4-1: Power Management Transition Timing on page 26. See Section 4.2, "Power Management States," on page 26.

TABLE 4-4:   WAKE EVENT SOURCES

EVENT SOURCE	INTERRUPT STATUS REGISTER (ADDRESS)	INTERRUPT MASK REGISTER (ADDRESS)	(GROUPING REGISTER) WAKE CONTROL BIT	NOTES
BC_CLK_UP/SMB_DAT_UP	None	None	Bit[0]	Note 4-2
GPIO[07:00]	32h	37h	Bit[2]	
GPIO[17:10]	32h	38h	Bit[2]	
GPIO[27:20]	33h	39h	Bit[2]	
PS/2_WAKE	F7h	F8h	Bit[4]	Note 4-2
TP/2_WAKE	F7h	F8h	Bit[5]	
KSI	42h	43h	Bit[3]	

Note 4-2   The BC_CLK_UP/SMB_DAT_UP active low detection is always an enabled wakeup event. and has no Interrupt Status Register or Interrupt Mask Register.

Note 4-3   In order for edge detection to work on any pin with an associated GPIO Configuration Register, the pin must be selected for input and the desired edges configured, as described in Table 7-4, "Direction, Level/Edge, Output Type Bit Definition," on page 48, in the GPIO configuration register.

The Wakeup event routing is illustrated in Figure 4-2. Generally the routing uses the following conventions with all exceptions specified in the notes in Table 4-4.

1.   All wakeup event sources are listed in Figure 4-2 and Table 4-4. All asynchronous wakeup event source states are maintained until clocks are restored and the associated interrupt source register bit is set.

2.   Each wakeup event undergoes the following bit-wise operations and the result forwarded to the Wake-up Control Register:

```
// first---
//each individual event masked.
Masked_Event = asynchrounous_wakeup_event & Interrupt_mask_bit

//Second---
//the masked events output from each mask register is logically
//OR'ed into a Group_Event.

//Therefore if any unmasked event is a '1', the group event output
is a '1'.

//Note The '|' bit wise operator has the following effect:
// result and bit = Bit[7] or bit[6] or ...or bit[0].
Group_Event = |Masked_Event[7:0]
```

3. The Grouping Register for wakeup events is Wake-up Control Register on page 32. The Wake-up Control Register bits are R/W and the wakeup events undergo the following bit-wise operations and the result forwarded to the wake input illustrated in FIGURE 4-1: Power Management Transition Timing on page 26:

```
// first---
// Group Event masked by Wake-up Control Register bit
Group_Result = Group_Event & Wake-up_Control_Register_bit

//Second---
//all masked Group_Results are logically OR'ed

//Therefore if any unmasked event is a '1', the group event output
is a '1'.

//Note The '|' bit wise operator has the following effect:
// resultand bit = Bit[7] or bit[6] or ...or bit[0].
Any_wakeup = |Group_Result[7:0]
```

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FIGURE 4-2: **WAKEUP/INTERRUPT ROUTING**
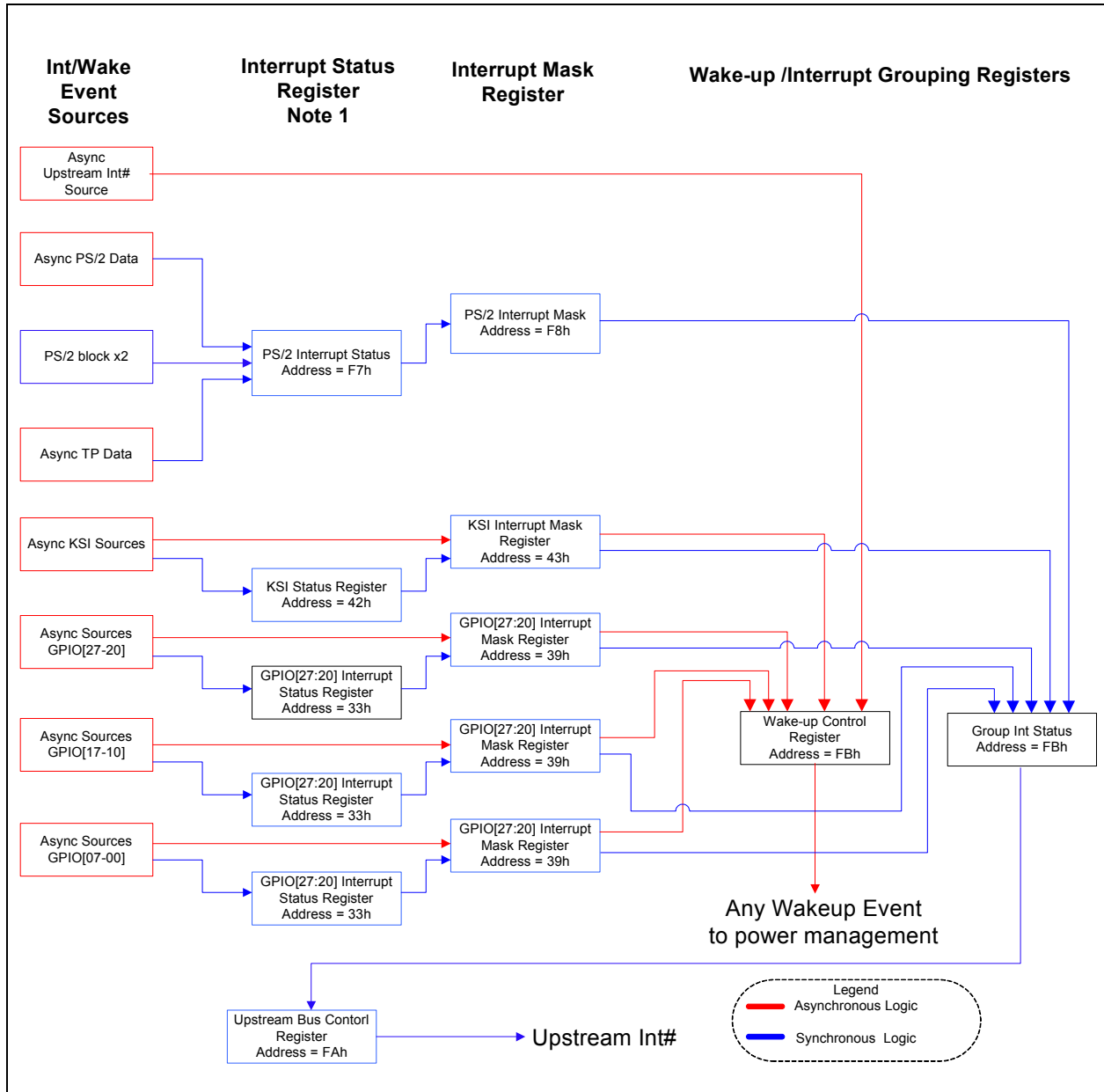
4.3.1   WAKE-UP CONTROL REGISTER

The Wake-up Control Register masks wakeup events.

TABLE 4-5:   WAKE-UP CONTROL REGISTER

BUS OFFSET	FBh					8-bit	**SIZE**	
POWER	VCC					00h	nDLY_RST **DEFAULT**	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	Test	Reserved	TP	PS/2	Keyscan	GPIO	Reserved	Upstream Data

TEST

Writes to this register should clear this bit to '0'.

TP

When this bit is cleared to '0', the TP START bit detection is not a Wakeup Event. When this bit is set to '1', a TP START bit detection is a wakeup event.

For edge detection on any TP pin the direction and edge configuration must be set in the GPIO Configuration registers for the GPIO pins that correspond to the TP pins.

> **Note:** If the TP bit is 1 and TP interrupts are not enabled, an edge on the TP pins may cause the internal Oscillator to start without an interrupt informing the Master device that the Oscillator is operating.

PS/2

When this bit is cleared to '0', the PS/2 START bit detection is not a Wakeup Event. When this bit is set to '1', a PS/2 START bit detection is wakeup event.

For edge detection on any PS/2 pin the direction and edge configuration must be set in the GPIO Configuration registers for the GPIO pins that correspond to the PS/2 pins.

> **Note:** If the PS/2 bit is 1 and PS/2 interrupts are not enabled, an edge on the PS/2 pins may cause the internal Oscillator to start without an interrupt informing the Master device that the Oscillator is operating.

GPIO

When this bit is cleared to '0', GPIO Interrupts are masked from generating a wakeup event. When this bit is set to '1', GPIO Interrupts are enabled to generating a wakeup event.

In order for edge detection to work on any GPIO pin the pin must be selected for input and the desired edges configured, as described in Table 7-4, "Direction, Level/Edge, Output Type Bit Definition," on page 48, in the GPIO configuration register.

Keyscan

When this bit is cleared to '0', KSI interface Interrupt is masked from generating a wakeup event. When this bit is set to '1', KSI interface Interrupt is enabled to generating a wakeup event.

For edge detection on any Keyscan pin the direction and edge configuration must be set in the GPIO Configuration registers for the GPIO pins that correspond to each Keyscan pin.

Upstream Data

When this bit is cleared to '0', BUS_DAT signal (BC_DAT_UP or SMB_DAT_UP) is masked from generating a wakeup event. When this bit is set to '1', BUS_DAT signal (BC_DAT_UP or SMB_DAT_UP) is enabled to generating a wakeup event.

4.4 Interrupt Interface

Table 4-6 and FIGURE 4-2: Wakeup/Interrupt Routing on page 31 describe the Interrupt routing.

TABLE 4-6: INTERRUPT EVENT SOURCES

EVENT SOURCE	WAKE CAPABLE	INTERRUPT STATUS REGISTER (ADDRESS)	INT MASK REG (ADDRESS)	GROUP INTERRUPT STATUS REGISTER	NOTES
GPIO[07:00]	YES	32h	37h	Bit[0]	
GPIO[17:10]	YES	32h	38h	Bit[1]	
GPIO[27:20]	YES	33h	39h	Bit[2]	
Reserved	-	-	-	Bit[3]	
Reserved	-	-	-	Bit[4]	
PS/2	NO	F7h	F8h	Bit[5]	
TP	NO	F7h	F8h	Bit[5]	
PS/2_WAKE	YES	F7h	F8h	Bit[5]	
TP/2_WAKE	YES	F7h	F8h	Bit[5]	
KSI	YES	42h	43h	Bit[6]	
Reserved	-	-	-	Bit[7]	

Note 4-4 In order for edge detection to work on any pin with an associated GPIO Configuration Register, the pin must be selected for input and the desired edges configured, as described in Table 7-4, "Direction, Level/Edge, Output Type Bit Definition," on page 48, in the GPIO configuration register.

The interrupt event routing is illustrated in Figure 4-2. Generally the routing uses the following conventions with all exceptions specified in the notes in Table 4-5.

1. Interrupt event sources are listed in Figure 4-2 & Table 4-5. During a wakeup event, all asynchronous wakeup event source states are maintained until clocks are restored and the associated interrupt source register bit is set.

2. The interrupt status register bits are R/WC and the interrupt mask register bits are R/W. All interrupts/wakeup events undergo the following bit-wise operations and the result forwarded to the Wake-up /Interrupt Grouping Registers:

```
//First---
// individual Masked_Event
Masked_Event = Interrupt_status_bit & Interrupt_mask_bit

//Second---
//the masked events output from each mask register is logically
OR'ed //into a Group_Event.

//Therefore if any unmasked event is a '1', the group event output
is //a '1'.

//Note The '|' bit wise operator has the following effect:
// resultand bit = Bit[7] or bit[6] or ...or bit[0].

Group_Event_bit = | Masked_Event[7:0]
```

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3. The Grouping Register for interrupt events is Group Interrupt Status Register on page 34. The Group Interrupt Status Register bits are read-only and the wakeup events undergo the following bit-wise operations:

```
//all masked Group_Results are logically OR'ed and then inverted.

//Therefore if any unmasked event is a '1', the group event output
is //a '1'.

//Note The '|' bit wise operator has the following effect:
// resultand bit = Bit[7] or bit[6] or ...or bit[0].
```

Int# = ! |Group_Result_bit[7:0]

4. The ARA bit in the Upstream Bus Control Register on page 43 must be set to assert upstream interrupts for both BC-Link and SMBus protocols. For the SMBus protocol the result is forwarded to the Upstream Bus Control Register for the SMBus Alert Response (see Section 6.5.10, "SMBus Alert Response Address," on page 45).

4.5   Group Interrupt Status Register

TABLE 4-7:   GROUP INTERRUPT STATUS REGISTER

BUS OFFSET	F9h					8-bit	**SIZE**	
POWER	VCC					00h	nDLY_RST **DEFAULT**	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R	R	R	R	R	R	R	R
BIT NAME	Reserved	Key-scan	PS/2	Reserved		GRP2	GRP1	GRP0

Keyscan

When this bit is cleared to '0', no Keyscan interrupt is asserted. When this bit is set to '1', the Keyscan interrupt is asserted

PS/2

When this bit is cleared to '0', no PS/2 interrupts are asserted. When this bit is set to'1',at least one of PS/2 interrupt is asserted.

Bit2 Grp2

When this bit is cleared to '0', no interrupts are asserted in GPIO Group2. When this bit is set to '1', at least one of the GPIO23-GPIO20 interrupt is asserted

Bit1 Grp1

When this bit is cleared to '0', no interrupts are asserted in GPIO Group1. When this bit is set to '1', at least one of the GPIO17-GPIO10 interrupt is asserted.

Bit0 Grp3

When this bit is cleared to '0', no interrupts are asserted in GPIO Group0. When this bit is set to '1', at least one of the GPIO07-GPIO00 interrupt is asserted.

5.0   MEMORY MAP

PROGRAMMER'S NOTE: After a powerup sequence, two writes to the POR Control Register on page 24 are required to set and then clear the POR bit.

> **Note:**   Some Test registers are read/write registers. Modifying these registers may have unwanted results.

TABLE 5-1:   REGISTER SUMMARY TABLE 1 OF 6

Address (Hex)	Name	nDLY_RST Default
00h	GPIO[7:0] Input Register	00h
01h	GPIO[17:10] Input Register	00h
02h	GPIO[27:20] Input Register	00h
03h	Reserved	
04h	Reserved	
05h	GPIO[7:0] Output Register	00h
06h	GPIO[17:10] Output Register	00h
07h	GPIO[27:20] Output Register	00h
08h	Reserved	
09h	Reserved	
0Ah	GPIO[00] Configuration Register	00h
0Bh	GPIO[01] Configuration Register	00h
0Ch	TEST	00h
0Dh	GPIO[03] Configuration Register	01h
0Eh	GPIO[04] Configuration Register	01h
0Fh	TEST	00h
10h	GPIO[06] Configuration Register	01h
11h	GPIO[07] Configuration Register	01h
12h	GPIO[10] Configuration Register	00h
13h	GPIO[11] Configuration Register	00h
14h	GPIO[12] Configuration Register	00h
15h	GPIO[13] Configuration Register	00h
16h	GPIO[14] Configuration Register	00h
17h	GPIO[15] Configuration Register	00h
18h	TEST	00h
19h	TEST	00h
1Ah	GPIO[20] Configuration Register	00h
1Bh	GPIO[21] Configuration Register	00h
1Ch	GPIO[22] Configuration Register	00h
1Dh	GPIO[23] Configuration Register	00h
1Eh	Reserved	
1Fh	Reserved	
20h-31h	Reserved	
32h	GPIO[7:0] Interrupt Status Register	00h
33h	GPIO[17:10] Interrupt Status Register	00h
34h	GPIO[27:20] Interrupt Status Register	00h
35h	Reserved	
36h	Reserved	
37h	GPIO[7:0] Interrupt Mask Register	00h
38h	GPIO[17:10] Interrupt Mask Register	00h
39h	GPIO[27:20] Interrupt Mask Register	00h
3Ah-3Fh	Reserved	

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TABLE 5-2: REGISTER SUMMARY TABLE 2 OF 6

Address (Hex)	Name	nDLY_RST Default
40h	KSO Select	40h
41h	KSI Input	00h
42h	KSI Status	00h
43h	KSI Interrupt Mask	00h
44h-4Fh	Reserved	
50h	PS/2 Transmit Buffer	00h
50h	PS/2 Receive Buffer	FFh
51h	PS/2 Control	00h
52h	PS/2 Status	10h
53h	Reserved	00h
54h	TP Transmit Buffer	00h
54h	TP Receive Buffer	FFh
55h	TP Control	00h
56h	TP Status	10h
57h	Reserved	00h
58h	TEST	02h
59h	TEST	58h
5Ah	TEST	0Fh
5Bh	TEST	A0h
5Ch	TEST	C3h
5Dh	TEST	50h
5Eh	TEST	04h
5Fh	Reserved	00h

TABLE 5-3:   REGISTER SUMMARY TABLE 3 OF 6

Address (Hex)	Name	nDLY_RST Default
60h	LED[1]__Control Register	00h
61h	LED[1]__Reserved	00h
62h	LED[1]__Reserved	00h
63h	LED[1]__Reserved	00h
64h	LED[1]__LED_DutyCycle Register	00h
65h	LED[1]__Reserved	00h
66h	LED[1]__LED_Prescale_LSB Register	00h
67h	LED[1]__LED_Prescale_MSB Register	00h
68h	LED[2]__Control Register	00h
69h	LED[2]__Reserved	00h
6Ah	LED[2]__Reserved	00h
6Bh	LED[2]__Reserved	00h
6Ch	LED[2]__LED_DutyCycle Register	00h
6Dh	LED[2]__Reserved	00h
6Eh	LED[2]__LED_Prescale_LSB Register	00h
6Fh	LED[2]__LED_Prescale_MSB Register	00h
70h	LED[3]__Control Register	00h
71h	LED[3]__Reserved	00h
72h	LED[3]__Reserved	00h
73h	LED[3]__Reserved	00h
74h	LED[3]__LED_DutyCycle Register	00h
75h	LED[3]__Reserved	00h
76h	LED[3]__LED_Prescale_LSB Register	00h
77h	LED[3]__LED_Prescale_MSB Register	00h
78h	LED[4]__Control Register	00h
79h	LED[4]__Reserved	00h
7Ah	LED[4]__Reserved	00h
7Bh	LED[4]__Reserved	00h
7Ch	LED[4]__LED_DutyCycle Register	00h
7Dh	LED[4]__Reserved	00h
7Eh	LED[4]__LED_Prescale_LSB Register	00h
7Fh	LED[4]__LED_Prescale_MSB Register	00h

TABLE 5-4:   REGISTER SUMMARY TABLE 4 OF 6

Address (Hex)	Name	nDLY_ RST Default
80h	TEST	00h
81h	TEST	00h
82h	TEST	00h
83h	TEST	00h
84h	TEST	00h
85h	TEST	00h
86h	TEST	00h
87h	TEST	00h
88h	TEST	00h
89h	TEST	00h
8Ah	TEST	00h
8Bh	TEST	00h
8Ch	TEST	00h
8Dh	TEST	00h
8Eh	TEST	00h
8Fh	TEST	00h
90h	LED[7]__Control Register	00h
91h	LED[7]__Reserved	00h
92h	LED[7]__Reserved	00h
93h	LED[7]__Reserved	00h
94h	LED[7]__LED_DutyCycle Register	00h
95h	LED[7]__Reserved	00h
96h	LED[7]__LED_Prescale_LSB Register	00h
97h	LED[7]__LED_Prescale_MSB Register	00h
98h	LED[8]__Control Register	00h
99h	LED[8]__Reserved	00h
9Ah	LED[8]__Reserved	00h
9Bh	LED[8]__Reserved	00h
9Ch	LED[8]__LED_DutyCycle Register	00h
9Dh	LED[8]__Reserved	00h
9Eh	LED[8]__LED_Prescale_LSB Register	00h
9Fh	LED[8]__LED_Prescale_MSB Register	00h
A0h	LED[9]__Control Register	00h
A1h	LED[9]__Reserved	00h
A2h	LED[9]__Reserved	00h
A3h	LED[9]__Reserved	00h
A4h	LED[9]__LED_DutyCycle Register	00h
A5h	LED[9]__Reserved	00h
A6h	LED[9]__LED_Prescale_LSB Register	00h
A7h	LED[9]__LED_Prescale_MSB Register	00h
A8h-BFh	Reserved	

TABLE 5-5:   REGISTER SUMMARY TABLE 5 OF 6

Address (Hex)	Name	nDLY_ RST Default
C0h-CFh	Reserved	
D0h	POR_CNTL	00h
D1h	TEST	00h
D2h	TEST	00h
D3H-DFh	Reserved	00h

TABLE 5-6:   REGISTER SUMMARY TABLE 6 OF 6

Address (Hex)	Name	nDLY_ RST Default
E0h-EEh	Reserved	
EFh	TEST	00h
F0h	SMBus Switch Control Reg	00h
F1h	Power Management Control Reg	00h
F2h	Reserved	00h
F3h	SMBus Slave Address Register	B8h or B9h
F4h	TEST	00h
F5h	SOFT_RST	00h
F6h	TEST	00h
F7h	PS/2 Interrupt Status	00h
F8h	PS/2 Interrupt Mask	00h
F9h	Group Interrupt	00h
FAh	Upstream Bus Contorl Register	00h
FBh	Wakeup Control	00h
FCh	Device ID	43h
FDh	Device Revision Number	Rev. B = 01h Rev. C = 05h
FEh	Vendor ID (LSB)	55h
FFh	Vendor ID (MSB)	10h

5.1   Miscellaneous Registers

5.1.1   DEVICE ID REGISTER

TABLE 5-7:   DEVICE ID REGISTER

BUS OFFSET	FCh				8-bit	SIZE		
POWER	VCC				43h	nDLY_RST DEFAULT		
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R	R	R	R	R	R	R	R
BIT NAME	43h							

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TABLE 5-8:   DEVICE REVISION REGISTER

BUS OFFSET	FDh					8-bit	**SIZE**	
POWER	VCC					Rev. B = 01h Rev. C = 05h (Note 5-1)	nDLY_RST **DEFAULT**	
BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BC-LINK™ TYPE	R	R	R	R	R	R	R	R
BIT NAME	Current Revision Number							

Note 5-1   This register is hardwired. See Anomaly Sheet for current revision level.

TABLE 5-9:   VENDOR ID (LSB) REGISTER

BUS OFFSET	FEh					8-bit	**SIZE**	
POWER	VCC					55h	nDLY_RST **DEFAULT**	
BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BC-LINK™ TYPE	R	R	R	R	R	R	R	R
BIT NAME	55h							

TABLE 5-10:   VENDOR ID (MSB) REGISTER

BUS OFFSET	FFh					8-bit	**SIZE**	
POWER	VCC					10h	nDLY_RST **DEFAULT**	
BIT	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BC-LINK™ TYPE	R	R	R	R	R	R	R	R
BIT NAME	10h							

5.1.2 RESET REGISTER

TABLE 5-11: RESET REGISTER

BUS OFFSET	F5h					8-bit	SIZE	
POWER	VCC					00h	nDLY_RST **DEFAULT**	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R	R	R	R	R	R	R	W
BIT NAME	Reserved							Force_ POR

Force_POR

Writing this bit with a 1 will force a nDLY_RST. All registers and state machines in the device will be reset to their default power-on values. Writing a 0 to this bit has no effect.

The Force_POR bit does not affect the **Interface Selection** setting of the Upstream Bus Control Register on page 43. Whichever bus interface is in effect at the time Force_POR is set (BC-Link or SMBus) will remain in effect after the POR.

6.0   UPSTREAM INTERFACES

6.1   General Description

Communication between upstream components and the ECE1117 is accomplished via SMBus or the BC-Link protocols using the same pins.

The ECE1117 has one Upstream Port and an internal slave device. The SMBus / BC-Link™ Autodetect Circuit determines which protocol is used.

6.2   BC-Link™

The BC-Link™ can connect an upstream BC-Link Master with the ECE1117 internal BC-Link Slave. (See Figure 6-1.)

FIGURE 6-1:   **BC-LINK™ BLOCK DIAGRAM**
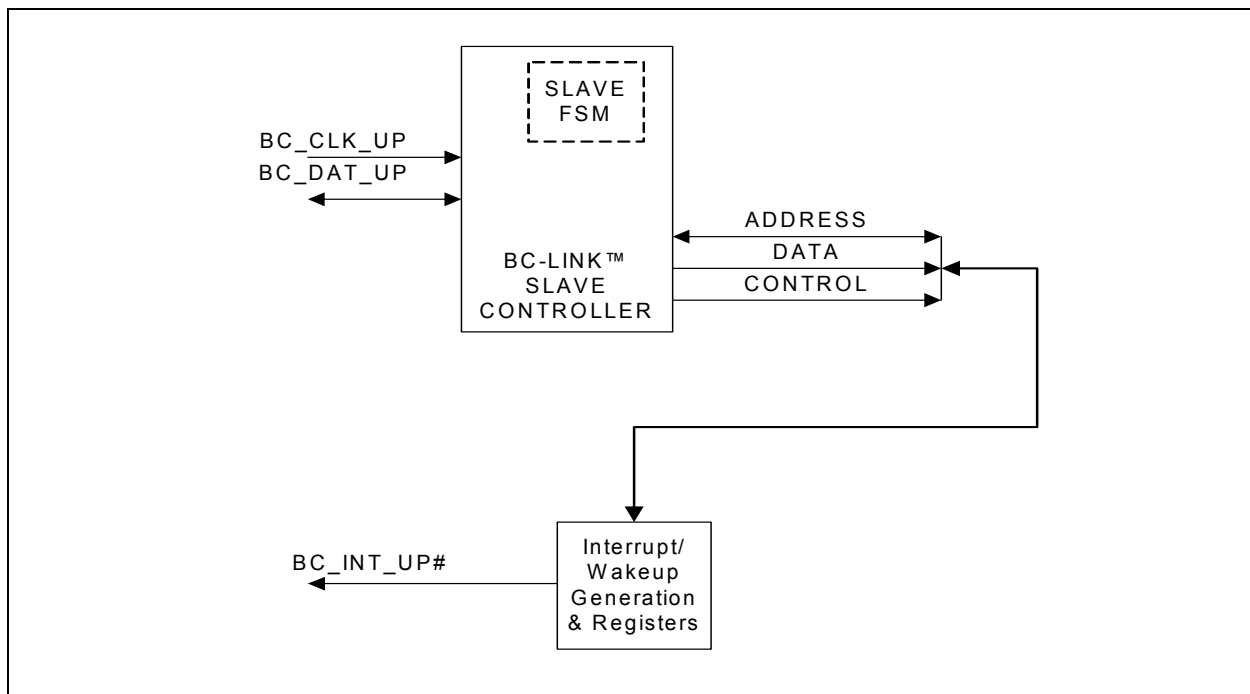
> **Note:**   Figure 6-1 is for illustration purposes only and is not intended to suggest specific implementation details.

• All Upstream transactions with address range 0E0h through 0EFh are absorbed by the ECE1117 internal BC Slave.

6.3   SMBus

The SMBus can connect the ECE1117 internal SMBus Slave with an upstream SMBus segment. The upstream SMBus segment must have at least one SMBus master.

Note 6-1   Each SMB Bus Segment data and clock requires a separate pullup.

6.4 SMBus / BC-Link™ Autodetect Circuit

6.4.1 OVERVIEW

The SMBus / BC-Link™ Autodetect Circuit determines the protocol traffic on the Upstream Port by detecting difference in start conditions. At Power On Reset or after the timeout timer expires, the Autodetect circuit waits for detection of the idle condition (both clk and data pins high). From an idle condition, the device will sample the data line on the first falling edge of the clock. If it is low, a SMBus interface is selected; if it is high, a BC-Link interface is selected.

To safeguard against glitches selecting the wrong bus protocol and locking the system, the ECE1117 uses time-outs that resets the Autodetect circuit. After detecting the transfer via the selected protocol, a timeout timer is started. If the timer expires, the Autodetect circuit is reset. For SMBus, the timeout timer is 50 ms. For BC-Link, the timeout timer is 50 µs.

6.4.2 UPSTREAM BUS CONTROL REGISTER

APPLICATION NOTE: The first access to the ECE1117 must be a write to the Upstream Bus Control Register to configure the Interface Selection field to the desired interface type (10b or 11b). This is required so that Oscillator control works properly and so that the bus type does not inadvertently switch during use.

TABLE 6-1:   UPSTREAM BUS CONTROL REGISTER

BUS OFFSET	FAh						8-bit	SIZE
POWER	VCC						00h	nDLY_RST DEFAULT
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R	R	R	R/W	R	R	R/W	R/W
BIT NAME	Reserved			ARA	Reserved		Interface Selection	

ARA

> **Note 6-2**   The ARA bit in the Upstream Bus Control Register on page 43 must be set to assert upstream interrupts for both BC-Link and SMBus protocols.

When the SMBus interface is selected, this bit can be written to a '1' to activate the SMBus slave ARA functionality. This bit must be a '1' to assert the SMB_INT_UP# signal pin function.

When the SMBus interface is selected, after the ECE1117 asserts an interrupt on the SMB_INT_UP# pin to the SMBus Master, The SMBus Master can initiate an Alert Response Address Read Byte command. When the ECE1117 wins arbitration of the ARA Read Byte command the ARA bit is autonomously cleared to '0' and the ECE1117 SMB_INT_UP# pin is deasserted. No additional interrupts will be asserted on the SMB_INT_UP until the ARA bit is set to'1'.

When the SMBus slave ARA functionality is not required, the programmer clears the ARA bit to '0'.

Interface Selection

> 0Xb Autodetect Mode (default)
> 10b BC-Link interface enabled
> 11b SMBus interface enabled

6.5 SMBus Slave Interface

The host processor communicates with the ECE1117device through a series of read/write registers via the SMBus interface. SMBus is a serial communication protocol between a computer host and its peripheral devices.

The SMBus data rate is 10KHz minimum to 400 KHz maximum.

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6.5.1 CLOCKING

The SMBus Slave interface is driven by an 10MHz Clock. See Section 4.0, "Power Management Interface," on page 26.

6.5.2 SLAVE ADDRESS

Upon power up, the ECE1117 selects the SMB slave address based on the SMB_ADDR strapping option on page 18. The device will latch the address during the first valid SMBus transaction in which the first five bits of the targeted address match those of the ECE1117 address. This feature eliminates the possibility of a glitch on the SMBus interfering with address selection.

The SMB address can be changed using a SMBus Write Byte Command to the SMBus Slave Address Register. The ECE1117 will respond to the new slave address during the next SMBus transaction.

TABLE 6-2:   SMBUS SLAVE ADDRESS OPTIONS

SMB_ADDR PIN	BOARD IMPLEMENTATION	SMBUS ADDRESS [7:1]
0	Address Select Pulled to ground through a 10kΩ resistor	0111 000b
1	Address Select pulled to VCC through a 10kΩ resistor	0111 001b

6.5.2.1 SMBus Slave Address Register

Writes to this register will change the slave address after the present transaction completes. The ECE1117 will respond to the new slave address during the next SMBus transaction.

Reads of this register indicate the current slave address.

TABLE 6-3:   SMBUS SLAVE ADDRESS REGISTER

BUS OFFSET	F3h					8-bit	SIZE	
POWER	VCC			SMB_ADDR ='0' ->1 0111 000b SMB_ADDR ='1' ->1 0111 001b			nDLY_RST DEFAULT	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	DFLT	SMB_SLAVE_ADDR[7:1]						

DFLT

This bit selects between default value selected by the SMB_ADDR strapping option on page 18 and a programmed value written into this register.

- 0 Programmed value
- 1 Default

Note 6-3   Should the value of the SMB_ADDR pin change, the default address will change following Table 6-2.

APPLICATION NOTE: Dynamically changing the state of the SMB_ADDR pin is not recommended.

SMB_SLAVE_ADDR[7:1]

Writes to this register with the DFLT bit cleared to '0' sets the slave address to the value written in the SMB_SLAVE_ADDR[7:1] field.

Writes to this register with the DFLT bit set to '1' sets the slave address to default value selected by the SMB_ADDR strapping option on page 18 and the SMB_SLAVE_ADDR[7:1] field is ignored.

Reads of this register provide the current Slave address that the ECE1117 in the SMB_SLAVE_ADDR[7:1] field.

6.5.3 SLAVE BUS INTERFACE

The ECE1117 device SMBus implementation is a subset of the SMBus interface to the host. The device is a *slave-only* SMBus device. The implementation in the device is a subset of SMBus since it only supports four protocols.

The Write Byte, Read Byte, Send Byte, and Receive Byte protocols are the only valid SMBus protocols for the device. This part responds to other protocols as described in the Invalid Protocol Section. Reference the System Management Bus Specification, Rev 2.0.

The SMBus interface is used to read and write the registers in the device. The register set is shown in Register Address Table.

6.5.4 WRITE BYTE

The Write Byte protocol is used to write data to the registers. The data will only be written if the protocol shown in Table 3.29 is performed correctly. Only one byte is transferred at time for a Write Byte protocol.

TABLE 6-4: SMBUS WRITE BYTE PROTOCOL

Field	Start	Slave Addr	Wr	Ack	Reg. Addr	Ack	Reg. Data	Ack	Stop
Bits	1	7	1	1	8	1	8	1	1

6.5.5 READ BYTE

The Read Byte protocol is used to read data from the registers. The data will only be read if the protocol shown in Table 3.30 is performed correctly. Only one byte is transferred at time for a Read Byte protocol.

TABLE 6-5: SMBUS READ BYTE PROTOCOL

Field:	Start	Slave Addr	Wr	Ack	Reg. Addr	Ack	Start	Slave Addr	Rd	Ack	Reg. Data	Nack	Stop
Bits:	1	7	1	1	8	1	1	7	1	1	8	1	1

6.5.6 SEND BYTE

The Send Byte protocol is used to set the Internal Address Register to the correct register in the ECE1117. No data is transferred for a Send Byte protocol.The send byte protocol is shown in Table 3.31.

TABLE 6-6: SMBUS SEND BYTE PROTOCOL

Field:	Start	Slave Addr	Wr	Ack	Reg. Addr	Ack	Stop
Bits:	1	7	1	1	8	1	1

6.5.7 RECEIVE BYTE

The Receive Byte protocol is used to read data from the registers when the register address is known to be at the desired address (using the Internal Address Register). Only one byte is transferred at time for a Receive Byte protocol.

TABLE 6-7: SMBUS RECEIVE BYTE PROTOCOL

Field:	Start	Slave Addr	Rd	Ack	Reg. Data	Nack	Stop
Bits:	1	7	1	1	8	1	1

> **Note:** Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or stop condition.

6.5.8 STRETCHING THE SCLK SIGNAL

The ECE1117 supports stretching of the SCLK by other devices on the SMBus.

6.5.9 SMBUS TIMING

The SMBus Slave Interface complies with the SMBus AC Timing Specification. See the SMBus timing diagram shown in Section 12.3, "SMBus Timing," on page 74.

6.5.10 SMBUS ALERT RESPONSE ADDRESS

This device responds to protocols with the SMBus Alert Response Address of 0001_100 if the ARA bit in the Upstream Bus Control Register is set. See Upstream Bus Control Register on page 43.

6.5.11   SMBUS TIME-OUT

The ECE1117 includes an SMBus time-out feature. Following a 30 ms period of inactivity on the SMBus, the device times-out and resets the SMBus interface.

6.6   BC-Link™ Interface

The BC-Link is a proprietary bus that allows communication between a Master device and a Companion device. The Master device uses this serial bus to read and write registers located on the Companion device.

The bus comprises three signals, BC_CLK, BC_DAT and BC_INT#. The Master device always provides the clock, BC_CLK, and the Companion device is the source for an independent asynchronous interrupt signal, BC_INT#.

The ECE1117 supports BC-Link speeds up to 3 MHz.

7.0 GENERAL PURPOSE INPUT OUTPUTS

7.1 GPIO Registers

PROGRAMMER'S NOTE: Do not write to the GPIO Configuration Register for GPIO[02,05,16,17]. These GPIO's do not exist in the part; they default to and should remain inputs, pullup/pulldown disabled.

7.1.1 GPIO INPUT REGISTER

TABLE 7-1: GPIO INPUT REGISTER

BUS OFFSET	See Table 5-1, "Register Summary Table 1 of 6," on page 35					8-bit	**SIZE**	
POWER	VCC					N/A	nDLY_RST DEFAULT	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R	R	R	R	R	R	R	R
BIT NAME	GPIOx7	GPIOx6	GPIOx5	GPIOx4	GPIOx3	GPIOx2	GPIOx1	GPIOx0

7.1.2 GPIO OUTPUT REGISTER

TABLE 7-2: GPIO OUTPUT REGISTER

BUS OFFSET	See Table 5-1, "Register Summary Table 1 of 6," on page 35					8-bit	**SIZE**	
POWER	VCC					00h	nDLY_RST DEFAULT	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	GPIOx7	GPIOx6	GPIOx5	GPIOx4	GPIOx3	GPIOx2	GPIOx1	GPIOx0

7.1.3 GPIO CONFIGURATION REGISTER

> **Note:** See General Rules for GPIO Configuration Register described in Section 2.3, "Pin Signal Function Multiplexing," on page 8 and Section 2.3.1, "Exceptions to the GPIO Configuration Register Rules," on page 9.

TABLE 7-3: GPIO CONFIGURATION REGISTER

BUS OFFSET	See Table 5-1, "Register Summary Table 1 of 6," on page 35			8-bit			SIZE	
POWER	VCC			See Memory Map on page 35			nDLY_RST DEFAULT	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
BIT NAME	Mux_Position		DIR	TYPE		POL	PD	PU

Mux_Position

Pin Signal Function Multiplexing select. This field determines which signal is selected on the pin based on the multiplexing position. The Mux_Position value can be looked up in the "MUX" column in the tables in Section 2.3, "Pin Signal Function Multiplexing," on page 8.

DIR, TYPE

The level/edge and output type are controlled by these fields. The effects are defined in Table 7-4, "Direction, Level/Edge, Output Type Bit Definition":

TABLE 7-4: DIRECTION, LEVEL/EDGE, OUTPUT TYPE BIT DEFINITION

DIRECTION BIT 5	TYPE BIT 4	TYPE BIT 3	SELECTED FUNCTION
0	0	0	Input, Level Sensitive Low
0	0	1	Input, Rising Edge Triggered
0	1	0	Input, Falling Edge Triggered
0	1	1	Input, Both Edge Triggered
1	0	x	Output, Push-Pull
1	1	x	Output, Open Drain

Note 7-1 In order to enable a Wakeup Event from a Low Power Mode for any GPIO pin, the GPIO Configuration Register for that GPIO must be configured for Input. To enable a Wakeup Event a Low Power Mode for any pin that is an alternate Signal Pin Function, the GPIO Configuration Register must still be configured for input. This applies to the wakeup sources in Table 4-4, "Wake Event Sources," on page 29. Signals that require specific edge detection also require the edge detection to be configured. PS/2 pin functions should be configured for edge triggering (TYPE field 01, 10 or 11). See Section 4.0, "Power Management Interface," on page 26.

POL

When the **POL** bit is set to '1' the signal output is inverted when routed to its pin and the interrupt level sense is inverted when a level-sensitive interrupt is selected by the **DIR, TYPE** fields. POL does not effect any output when the Mux_Position Field is not '00'. The state of the pin is always reported without inversion in the GPIO Input Register, independent of the value of **POL** or Mux_Position.

PD

When this bit is 1, an internal pull-down resistor is enabled. When this bit is 0, the pull-down is disabled.

PU

When this bit is 1, an internal pullup resistor is enabled. When this bit is 0, the pullup is disabled.

7.1.4 GPIO INTERRUPT STATUS REGISTER

TABLE 7-5: GPIO INTERRUPT STATUS REGISTER

BUS OFFSET	**See** Table 5-1, "Register Summary Table 1 of 6," on page 35					8-bit	**SIZE**	
POWER	VCC					00h	**nDLY_RST DEFAULT**	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC
BIT NAME	GPIOX7	GPIOX6	GPIOX5	GPIOX4	GPIOX3	GPIOX2	GPIOX1	GPIOX0

A bit in a GPIOX Interrupt Status Register is set to 1 when the DIRECTION field for that bit in the corresponding GPIOX*n* Configuration Register is set for Input and the bit in the corresponding GPIOX Input Register matches the conditions defined by the TYPE field in the GPIOX Configuration Register. For example, if the TYPE field for GPIO X*n* is set for Level Sensitive Low, then bit *n* in the GPIOX Interrupt Status Register is set to 1 when bit *n* in the GPIOX Input Register is 0. If the TYPE field specifies edge triggering, then the Status Register bit is set when the Input Register bit transitions with the specified edge.

Writing a bit in a GPIOX Interrupt Status Register clears that bit. Writing a bit with a 0 has no effect.

7.1.5 GPIO INTERRUPT MASK REGISTER

TABLE 7-6: GPIO INTERRUPT MASK REGISTER

BUS OFFSET	**See** Table 5-1, "Register Summary Table 1 of 6," on page 35					8-bit	**SIZE**	
POWER	VCC					00h	**nDLY_RST DEFAULT**	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	GPIOX7 0 No Int 1 Int	GPIOX6 0 No Int 1 Int	GPIOX5 0 No Int 1 Int	GPIOX4 0 No Int 1 Int	GPIOX3 0 No Int 1 Int	GPIOX2 0 No Int 1 Int	GPIOX1 0 No Int 1 Int	GPIOX0 0 No Int 1 Int

An interrupt is signaled on either BC_INT_UP# or SMB_INT_UP# when a GPIOX bit in a GPIO Interrupt Status Register is 1 and the corresponding GPIOX bit in the GPIO Interrupt Mask Register is also 1.

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8.0   LED

8.1   General Description

The LED can control three external LEDs. Each LED can be individually set to be full on, full off, or oscillate. Oscillation can in turn be configured to "blink", where the LED output switches between full on and full off at a fixed frequency, or to "breathe", where the brightness of the LED increases and decreases at a fixed rate.

The periodic behavior of the LEDs is driven by the 32.895KHz clock derived from the 10MHz Clock.

The Blink Mode equations are shown in Figure 8-1 and Breathing Mode LED Equations are shown in Figure 8-2.

FIGURE 8-1:   BLINK MODE EQUATIONS

$$\text{BLINK PERIOD} = \frac{32895}{(\text{LED\_PRESCALE[11:0]} + 1)} \times \frac{1}{2^8} \text{ Hz}$$

$$\text{"H" width} = \frac{\text{LED\_DUTYCYCLE[7:0]}}{\text{BLINK PERIOD}} \times \frac{1}{256} \text{ Sec}$$

$$\text{"L" width} = \frac{(256 - \text{LED\_DUTYCYCLE[7:0]})}{\text{BLINK PERIOD}} \times \frac{1}{256}$$

$$\text{Breathing Oscillation TIme} = \frac{2x\ (255 - \text{"Min" LED\_DUTYCYCLE[7:0]})}{\text{BLINK PERIOD}} \text{ Sec}$$

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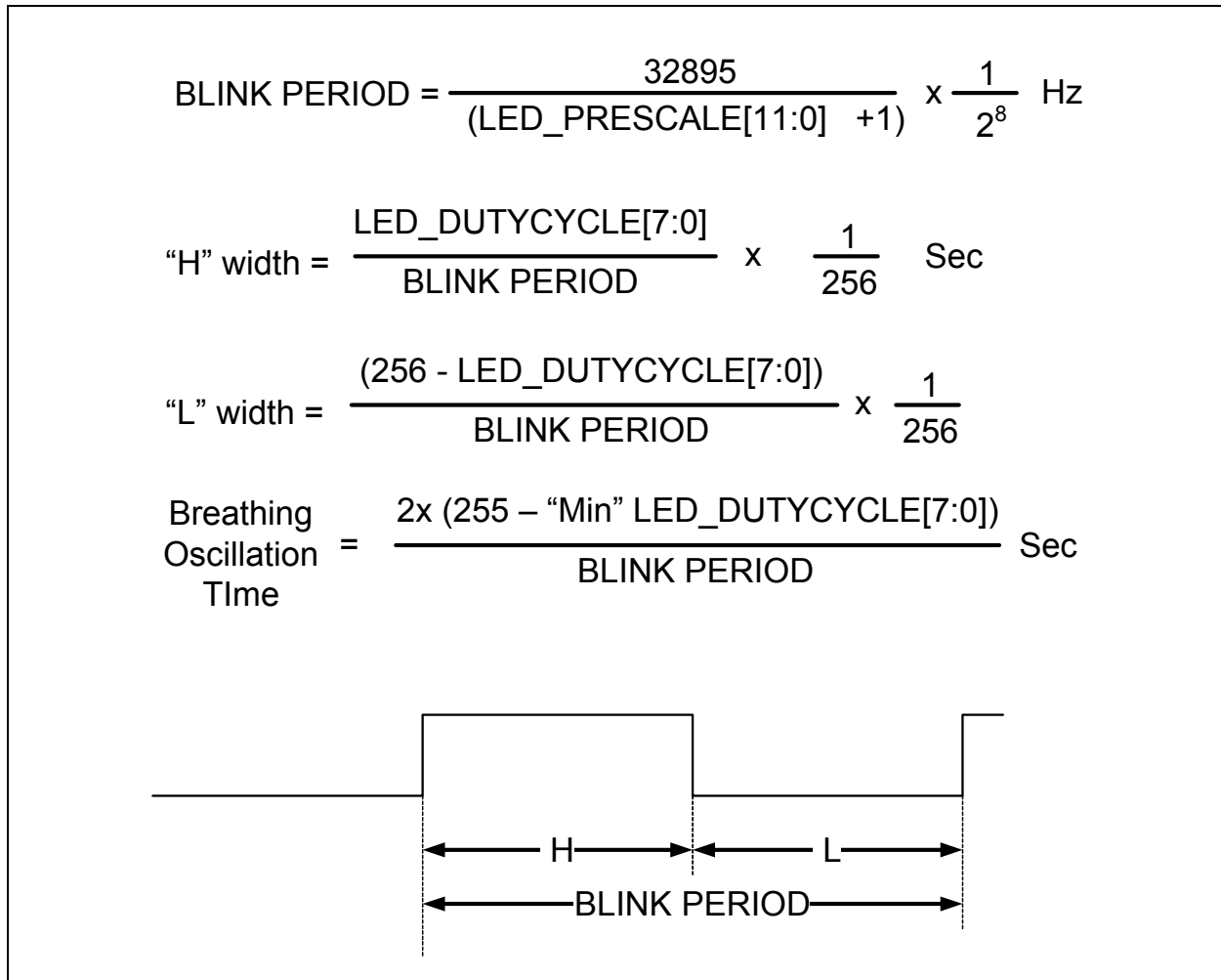
FIGURE 8-2: **BREATHING MODE LED EQUATIONS**

$$\text{BLINK PERIOD} = \frac{32895}{(\text{LED\_PRESCALE[11:0]} + 1)} \times \frac{1}{2^8} \text{ Hz}$$

$$\text{"H" width} = \frac{\text{LED\_DUTYCYCLE[7:0]}}{\text{BLINK PERIOD}} \times \frac{1}{256} \text{ Sec}$$

$$\text{"L" width} = \frac{(256 - \text{LED\_DUTYCYCLE[7:0]})}{\text{BLINK PERIOD}} \times \frac{1}{256} \text{ Sec}$$

ECE1117
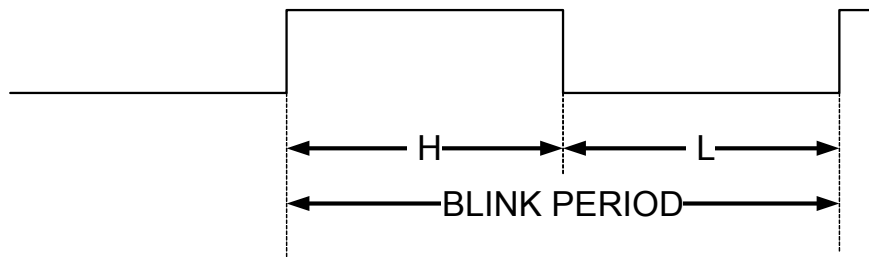
8.2 LED Block Diagram

FIGURE 8-3: **LED BLOCK DIAGRAM**
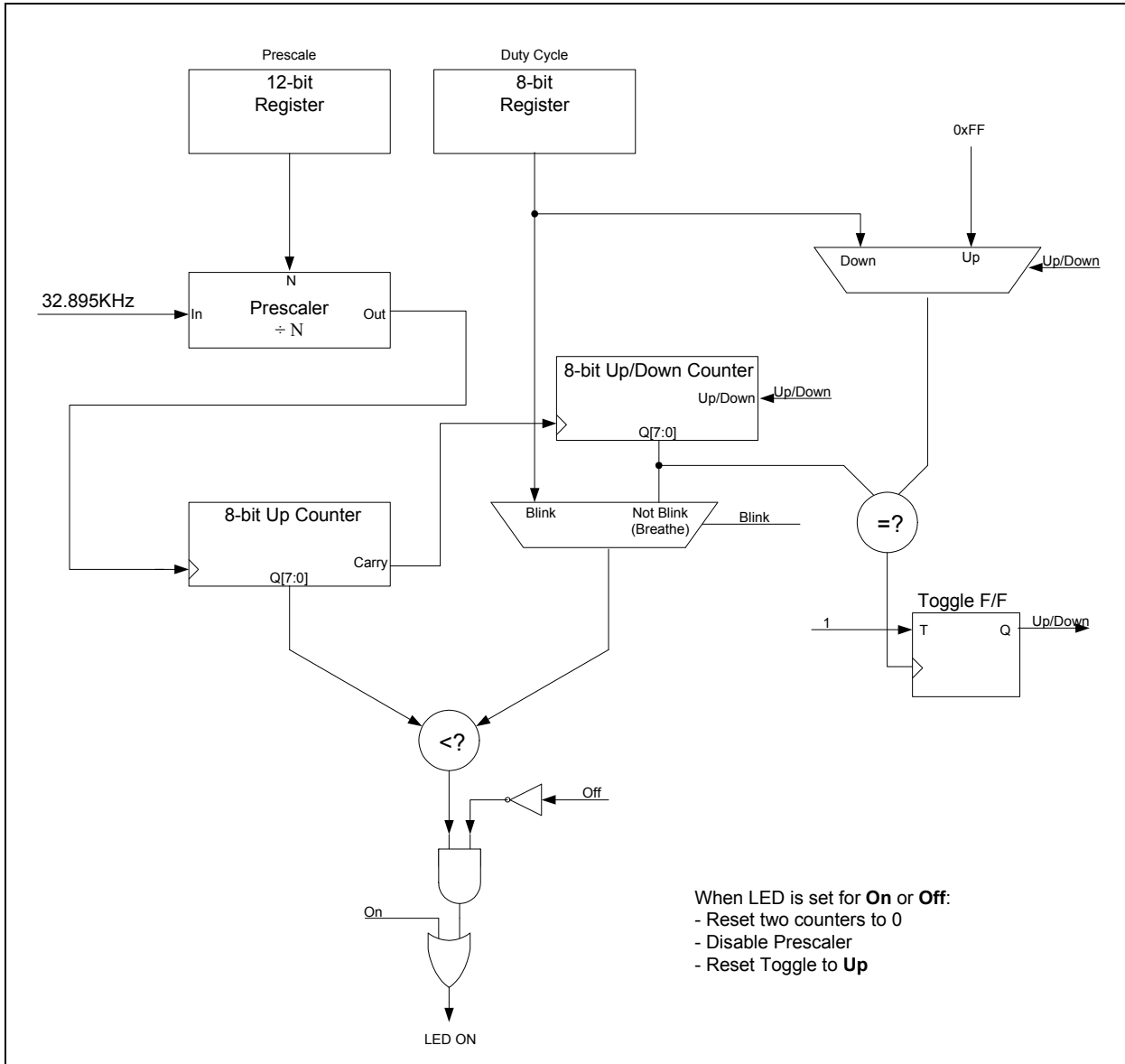
8.3 Block Diagram Signal List

TABLE 8-1: **LED SIGNAL LIST**

SIGNAL NAME	DIRECTION	DESCRIPTION
32.895KHz	INPUT	10MHz Clock/**304**
Blink	Internal	Control signal from LED Control Register
Up/Down	Internal	Control signal generated by 8-bit Up/Down counter
LED ON	OUTPUT	LED outputs
SYNC_in	INPUT	SYNC INPUT indicates all LED

8.4   LED Blinking and Breathing

Blinking and breathing is controlled by two registers for each LED. The first register controls the clock prescaler that sets the oscillation period. An 8-bit counter clocked on the pre-scaled 32.895KHz clock defines a blink period with 256 phases. In "blink" mode, the second register determines the duty cycle of the LED blink. In "breathe" mode, the second register determines the minimum duty cycle of the LED.

When the prescale is 0, the blink period will use the 32.895KHz clock (with 30.4μs phases). For $N>0$, the 32.895KHz clock will be divided by $N+1$. For examples of settings of the prescale and duty cycle registers, see Table 8-2, "LED Control Configuration Examples". The maximum blink period is 31.87 seconds.

When an LED is configured to be fully off or fully on, the prescalar and other counters in the LED circuitry are shut down in order to save power.

Note 8-1   The ECE1117 can enter sleep while a LED is configured to fully off or fully on.

8.4.1   BLINKING

When configured for blinking, the LED will be on for all phases of the prescaled period that are less than the duty cycle and off for all phases that are greater than the duty cycle. An LED with a duty cycle value of 0h will be fully off, while an LED with a duty cycle value of FFh will be fully on.

8.4.2   BREATHING

When configured for breathing, the duty cycle of the LED blink will continuously increase and decrease between full on (a duty cycle of FFh) and a minimum duty cycle set by the duty cycle register. After each blink period the duty cycle will increase by 1, until the duty cycle saturates at FFh. Once the duty cycle saturates, it is reduced by 1 after each blink period, until it reaches a minimum duty cycle set by the duty cycle register. Once the minimum duty cycle is reached, the duty cycle will start increasing again. If the frequency of the LED blink period is sufficiently fast (for example, greater than 30Hz), the LED will not appear to blink but will instead appear dimmer or brighter, depending on the duty cycle.

The overall duration of the breathing oscillation is a factor of the blink period and the minimum duty cycle. The total time will be 2 X (*BLINK_PERIOD* X (*FFh - MIN_DUTY_CYCLE*)).

TABLE 8-2:   LED CONTROL CONFIGURATION EXAMPLES

PRESCALE	DUTY CYCLE	BLINK PERIOD	BLINK	BREATHE
000h	00h	128Hz	full off	full off to full on 4s oscillation cycle
001h	40h	64Hz	3.9ms on, 11.6ms off	quarter on to full on 6s oscillation cycle
003h	80h	32Hz	15.5ms on, 15.5ms off	half on to full on 8s oscillation cycle
07Fh	20h	1Hz	125ms on, 0.875s off	blink to 1s on 7m 26s oscillation cycle
0BFh	16h	0.66Hz	125ms on, 1.375s off	blink to 1.5s on 11m 39s oscillation period
0FFh	10	0.5Hz	125ms on, 1.875s off	blink to 2s on 15m 56s oscillation period
180h	0Bh	0.33Hz	125ms on, 2.875s off	blink to 3s on 24m 24s oscillation period
1FFh	40h	0.25Hz	1s on, 3s off	1s/3s on/off to 4s on 12m 48s oscillation cycle

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8.5 LED Registers

There are three instances of the LED block implemented in the ECE1117 enumerated as [1:9]. Each instance of the LED has its Base Address as indicated in Table 8-3, " LED Base Address Table".

TABLE 8-3: LED BASE ADDRESS TABLE

LED INSTANCE	AHB BASE ADDRESS
LED[1]	60h
LED[2]	60h + 8h = 68h
LED[3]	68h + 8h = 70h
LED[4]	70h + 8h = 78h
LED[7]	88h + 8h = 90h
LED[8]	90h + 8h = 98h
LED[9]	98h + 8h = A0h

Table 8-4 is a register summary for one instance of the LED block.

TABLE 8-4: LED REGISTER SUMMARY

REGISTER NAME	OFFSET	TYPE
LED Control Register	00h	R/W
LED DutyCycle Register	04h	R/W
LED Prescale_LSB Register	06h	R/W
LED Prescale_MSB Register	07h	R/W

Note: It may take up to 30μs for a change to a LED register to take effect.

8.5.1 LED CONTROL REGISTER

The LED Control Register is used to control the behavior of each of the three output LEDs.

TABLE 8-5: LED CONTROL REGISTER

BUS OFFSET	0h					8-bit	**EC SIZE**	
POWER	VCC					0000_0000h	nDLY_RST **DEFAULT**	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	Reserved					Synch	Control	

Control

This bit controls the behavior of LED:

0= LED is always off

1= LED blinks, at a rate controlled by the LED Rate Registers

2= LED breathes, at a rate controlled by the LED Rate Registers

3= LED is always on

Note 8-2 The LED Rate Registers consist of the following three eight bit registers: LED DutyCycle Register, LED Prescale_MSB Register & LED Prescale_LSB Register.

Synch

When this bit is 1, all counters for all LEDs are reset to their initial values. When this bit is 0 in the LED Control Register for all LEDs, then all counters for LEDs that are configured to blink or breathe will increment or decrement, as required.

APPLICATION NOTE: To synchronize blinking or breathing, The Synch bit should be set for at least one LED, the LED Control Register and the LED Rate Registers for each LED should be set to their required values, then the Synch bits should all be cleared. If the LED Rate Registerss are set for the same blink period, they will all be synchronized.

8.5.2 LED RATE REGISTERS

The LED Rate Registers are used to configure the blinking and breathing rate of each of the LEDs.

* The LED Rate Registers consist of the following three eight bit registers: LED DutyCycle Register, LED Prescale_MSB Register & LED Prescale_LSB Register.

8.5.2.1 LED DutyCycle Register

TABLE 8-6: LED DUTYCYCLE REGISTER

BUS OFFSET	4h						8-bit	EC SIZE
POWER	VCC						00h	nDLY_RST DEFAULT
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	LED_DutyCycle							

LED_DutyCycle[7:0]

The field determines the duty cycle of the LED blink pattern. A value of 0 means full off, a value of FFh means full on.

8.5.2.2 LED Prescale Registers

LED_Prescale[11:0]

LED_Prescale[11:0] field is divided between two eight bit registers: LED Prescale_MSB Register & LED Prescale_LSB Register. If this field is 0, the 32.895KHz clock will be used to determine the blink period of LED: If this field is greater than 0, then the 32.895KHz clock will be divided by LED_Prescale[11:0]+1

TABLE 8-7: LED PRESCALE_LSB REGISTER

BUS OFFSET	6h						8-bit	EC SIZE
POWER	VCC						00h	nDLY_RST DEFAULT
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	LED_Prescale[7:0]							

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TABLE 8-8:   LED PRESCALE_MSB REGISTER

BUS OFFSET	7h					8-bit	**EC SIZE**	
POWER	VCC					00h	nDLY_RST **DEFAULT**	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R	R	R	R	R/W	R/W	R/W	R/W
BIT NAME	LED_Prescale[11:8]							

9.0 KEYSCAN

9.1 General Description

> **Note:** See GPIO Configuration Register on page 48 for register definition and Register Summary Table 1 of 6 on page 35 specific pin defaults Pullup/Pulldown, Open Drain/Pushpull configurations. Also see General Rules for GPIO Configuration Register described in Section 2.3, "Pin Signal Function Multiplexing," on page 8 and Section 2.3.1, "Exceptions to the GPIO Configuration Register Rules," on page 9.

9.1.1 KEYBOARD SCAN REGISTERS

9.1.1.1 KSO Select

TABLE 9-1: KSO SELECT REGISTER

BUS OFFSET	40h						8-bit	SIZE
POWER	VCC						40h	nDLY_RST DEFAULT
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	KSO INVERT	KSEN	KSO ALL	KSO Driver Select[4:0]				

Bit[7] KSO INVERT

KSO INVERT = 1 inverts KSO[22:0]. When KSO INVERT = 0 KSO[22:00] operate normally See Table 9-3, "Keyboard Scan Out Control Summary," on page 58.

Bit[6] KSEN

KSEN = 1 disables keyboard scan and drives. KSEN = 0 enables keyboard scan.

Bit[5] KSO ALL

KSO ALL = 1, drives all KSO lines according to KSO INVERT bit. See Table 3.9, "Keyboard Scan Out Control summary," on page 23.

Bits[4:0] KSO Driver Select

KSO Driver Select controls the corresponding KSO line (00000b = KSO[0] etc.) according to KSO INVERT. See Table 9-2, "KSO Select Decode".

TABLE 9-2: KSO SELECT DECODE

KSO SELECT [4:0]	KSO SELECTED
00h	KSO00
01h	KSO01
02h	KSO02

TABLE 9-2: **KSO SELECT DECODE (CONTINUED)**

KSO SELECT [4:0]	KSO SELECTED
03h	KSO03
04h	KSO04
05h	KSO05
06h	KSO06
07h	N/A
08h	N/A
09h	N/A
0Ah	N/A
0Bh	KSO11
0Ch	KSO12
0Dh	KSO13
0Eh	KSO14
0Fh	KSO15
10h	KSO16
11h	KSO17
12h	KSO18
13h	KSO19
14h	KSO20
15h	KSO21
16h	KSO22
17h - 1Fh	Reserved

TABLE 9-3: **KEYBOARD SCAN OUT CONTROL SUMMARY**

D7 KSO INVERT	D6 KSEN	D5 KSO ALL	D[5:0] KSO DRIVERS ADDRESS	DESCRIPTION
X	1	x	x	Keyboard Scan disabled KSO[22:00] driven high.
0	0	0	10110b-00000b	KSO[Drive Selected] asserted low. All others de-asserted high
1	0	0	10110b-00000b	KSO[Drive Selected] de-asserted high. All others asserted low
0	0	0	11111b-10111b	ALL KSO's de-asserted high
1	0	-	11111b-10111b	All KSO's asserted low

TABLE 9-3: KEYBOARD SCAN OUT CONTROL SUMMARY (CONTINUED)

D7 KSO INVERT	D6 KSEN	D5 KSO ALL	D[5:0] KSO DRIVERS ADDRESS	DESCRIPTION
0	0	1	x	KSO[22:0] driven low
1	0	1	x	KSO[22:00] driven high

9.1.1.2　　KSI Input

TABLE 9-4: KSI INPUT REGISTER

BUS OFFSET	41h					8-bit	**SIZE**
POWER	VCC					00h	nDLY_RST **DEFAULT**
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R	R	R	R	R	R	R	R
BIT NAME	KS7	KS6	KS5	KS4	KS3	KS2	KS1	KS0

9.1.1.3　　KSI Status

TABLE 9-5: KSI STATUS REGISTER

BUS OFFSET	42h					8-bit	**SIZE**
POWER	VCC					00h	nDLY_RST **DEFAULT**
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC	R/WC
BIT NAME	Status of KI7	Status of KSI6	Status of KSI5	Status of KSI4	Status of KSI3	Status of KSI2	Status of KSI1	Status of KSI0

Note 9-1 The status bit is set by a falling edge of the KS input.

Note 9-2 Writing a 1 to a bit will clear that bit to 0.

Operation:

KSI interrupt is generated when one of the KSI signals transitions from High to Low (Edge Triggered). This interrupt will not be signalled again until all KSI signals are brought high and one then transitions low.

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9.1.1.4   KSI Mask

TABLE 9-6:   KSI INTERRUPT MASK REGISTER

BUS OFFSET	43h						8-bit	SIZE
POWER	VCC						00h	nDLY_RST DEFAULT
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT NAME	KSI7 1= Inten 0= No Int	KSI6 1= Inten 0= No Int	KSI5 1= Inten 0= No Int	KSI4 1= Inten 0= No Int	KSI3 1= Inten 0= No Int	KSI2 1= Inten 0= No Int	KSI1 1= Inten 0= No Int	KSI0 1= Inten 0= No Int

10.0   PS/2 INTERFACE

The PS/2 Device Interface has two independent Hardware Driven PS/2 ports. Each PS/2 serial channels use a synchronous serial protocol to communicate with an auxiliary device. Each PS/2 channel has Clock and Data signal lines. The signal lines are bi-directional and employ open drain outputs capable of sinking 16mA. A pullup resistor, typically 10K, is connected to both lines. This allows either the ECE1117 PS/2 logic or the auxiliary device to drive the lines. Regardless of the drive source, the auxiliary device always provides the clock for transmit and receive operations. The serial packet is made up of eleven bits, listed in the order they appear on the data line: start bit, eight data bits (least significant bit first), odd parity, and stop bit. Each bit cell is from $60\mu S$ to $100\mu S$ long.

10.1   Block Diagram

FIGURE 10-1:   PORT PS/2 BLOCK DIAGRAM
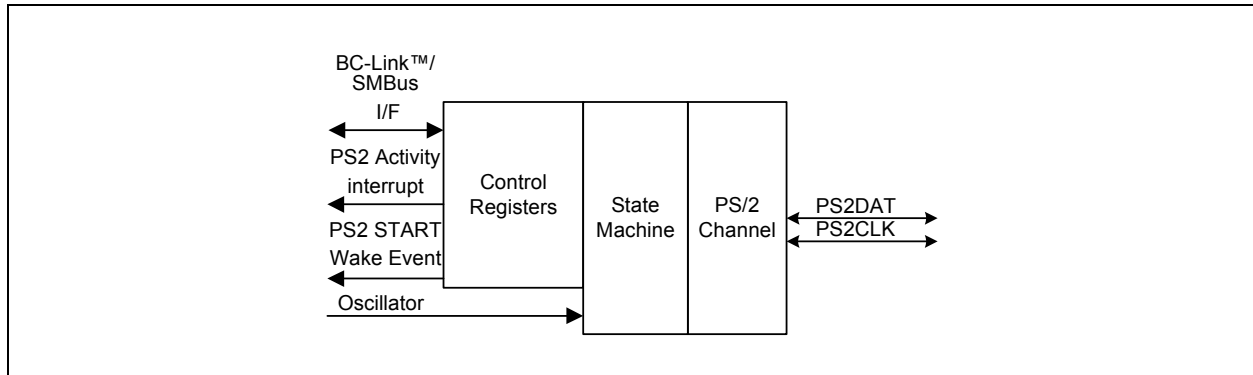
10.1.1   PS/2 PORT PHYSICAL LAYER BYTE TRANSMISSION PROTOCOL

The PS/2 physical layer transfers a byte of data via an eleven bit serial stream as shown in Table 10-1. A logic 1 is sent at an active high level. Data sent from a Keyboard or mouse device to the host is read on the falling edge of the clock signal. The Keyboard or mouse device always generates the signal. The Host may inhibit communication by pulling the Clock line low. The Clock line must be continuously high for at least 50 microseconds before the Keyboard or mouse device can begin to transmit its data. See Table 10-2, "PS/2 Port Physical Layer Bus States".

TABLE 10-1:   PS/2 PORT PHYSICAL LAYER BYTE TRANSMISSION PROTOCOL

BIT	FUNCTION
1	Start bit (always 0)
2	Data bit 0 (least significant bit)
3	Data bit 1
4	Data bit 2
5	Data bit 3
6	Data bit 4
7	Data bit 5
8	Data bit 6
9	Data bit 7 (most significant bit)
10	Parity bit (odd / even or no parity)
11	Stop Bit (1, 0 or ignored)

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FIGURE 10-2: **PS/2 PORT PHYSICAL LAYER BYTE TRANSMISSION PROTOCOL**
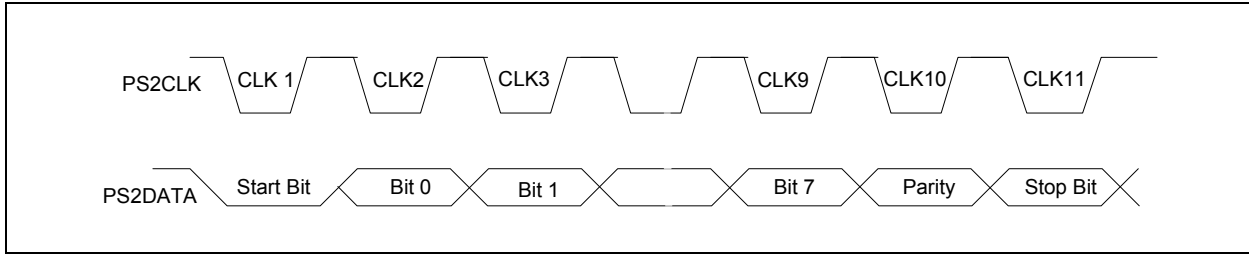
TABLE 10-2: **PS/2 PORT PHYSICAL LAYER BUS STATES**

DATA	CLOCK	STATE
high	high	Idle
high	low	Communication Inhibited
low	low	Request to Send

10.2   Interrupts

Each of the two PS/2 Channels has both a PS/2 activity interrupt event and a START Bit detection Wake-up event. The activity interrupt event is routed to the PS/2 Interrupt Status. The START Bit detection wakeup event is routed to the Wake-up Control Register.

APPLICATION NOTE: The GPIO Configuration registers for the pins that correspond to the PS/2 and the TP ports should be programmed to Input, Falling Edge Triggered, non-inverted polarity detection in order to enable PS/2 or TP START Bit detection wakeup events.

10.2.1   PS/2 INTERRUPT STATUS

TABLE 10-3:   PS/2 INTERRUPT STATUS

BUS OFFSET	F7h					8-bit	SIZE	
POWER	VCC					00h	nDLY_RST DEFAULT	
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R	R	R/WC	R/WC	R/WC	R/WC	R	R
BIT NAME	Reserved	Reserved	TP WAKE	PS/2 WAKE	TP	PS/2	Reserved	Reserved

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Bit5 TP WAKE

This bit is set to 1 if there is a TP Wake-up event, which occurs when there is TP activity and the TP bit is set in the Wake-up Control Register register. It is cleared when written with a 1. See Section 4.0, "Power Management Interface," on page 26 and Section 4.3, "Wake-up Interface," on page 29.

> Note 10-1   In order for edge detection to work on any pin with an associated GPIO Configuration Register, the pin must be selected for input and the desired edges configured, as described in Table 7-4, "Direction, Level/Edge, Output Type Bit Definition," on page 48, in the GPIO configuration register.

Bit4 PS/2 WAKE

This bit is set to 1 if there is a PS/2 Wake-up event, which occurs when there is PS/2 activity and the PS/2 bit is set in the Wake-up Control Register register. It is cleared when written with a 1. See Section 4.0, "Power Management Interface," on page 26, Section 4.3, "Wake-up Interface," on page 29, and Note 10-1.

Bit5 TP

This bit is set to 1 if an interrupt is signaled (as defined by Note 10-6, Note 10-5 and Note 10-4) in the TP Status Register. It is cleared when written with a 1.

Bit4 PS/2

This bit is set to 1 if an interrupt is signaled (as defined by Note 10-6, Note 10-5 and Note 10-4) in the PS/2 Status Register. It is cleared when written with a 1.

10.2.2   PS/2 INTERRUPT MASK

TABLE 10-4:   PS/2 INTERRUPT MASK

BUS OFFSET	F8h						8-bit	SIZE
POWER	VCC						00h	nDLY_RST DEFAULT
BIT	D7	D6	D5	D4	D3	D2	D1	D0
BC-LINK™ TYPE	R	R	R/W	R/W	R/W	R/W	R	R
BIT NAME	Reserved	Reserved	TP WAKE	PS/2 WAKE	TP	PS/2	Reserved	Reserved

Bit5 TP WAKE

The interrupt signal (BC_INT# in BC-LINK mode or SMB_INT# in SMBus mode) is asserted when this bit is 1 and Bit5 TP WAKE in the PS/2 Interrupt Status is 1.

Bit4 PS/2 WAKE

The interrupt signal (BC_INT# in BC-LINK mode or SMB_INT# in SMBus mode) is asserted when this bit is 1 and Bit4 PS/2 WAKE in the PS/2 Interrupt Status is 1.

Bit3 TP

The interrupt signal (BC_INT# in BC-LINK mode or SMB_INT# in SMBus mode) is asserted when this bit is 1 and Bit3 TP in the PS/2 Interrupt Status is 1.

Bit2 PS/2

The interrupt signal (BC_INT# in BC-LINK mode or SMB_INT# in SMBus mode) is asserted when this bit is 1 and Bit2 PS/2 in the PS/2 Interrupt Status is 1.

10.3 Block Registers

PS/2 TX/RX

The byte written to this register, when PS/2_T/R, PS/2_EN, and XMIT_IDLE are set, is transmitted automatically by the PS/2 channel control logic. If any of these three bits (PS/2_T/R, PS/2_EN, and XMIT_IDLE) are not set, then writes to this register are ignored. On successful completion of this transmission or upon a Transmit Time-out condition, the PS/2_T/R bit is automatically cleared and the XMIT_IDLE bit is automatically set. The PS/2_T/R bit must be written to a '1' before initiating another transmission to the remote device.

10.3.1 TRANSMIT BUFFER

TABLE 10-5: TRANSMIT BUFFER REGISTER

BU OFFSET	PS/2: 50h TP: 54h					8-bit	**SIZE**	
POWER	VCC					00h	nDLY_RST **DEFAULT**	
BYTE0 BIT	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	W							
BIT NAME	Transmit Data PS/2							

Even if PS/2_T/R, PS/2_EN, and XMIT_IDLE are all set, writing the Transmit Register will not kick off a transmission if RDATA_RDY is set. The automatic PS/2 logic forces data to be read from the Receive Register before allowing a transmission.

An interrupt is generated on the low to high transition of XMIT_IDLE.

All bits of this register are write only.

10.3.2 RECEIVE BUFFER

When PS/2_EN=1 and PS/2_T/R=0, the PS/2 Channel is configured to automatically receive data on that channel (both the CLK and DATA lines will float waiting for the peripheral to initiate a reception by sending a start bit followed by the data bits). After a successful reception, data is placed in this register and the RDATA_RDY bit is set and the CLK line is forced low by the PS/2 channel logic. RDATA_RDY is cleared and the CLK line is released to hi-z following a read of this register. This automatically holds off further receive transfers until the Master has had a chance to get the data.

TABLE 10-6: RECEIVE BUFFER REGISTER

BUS OFFSET	PS/2: 50h TP: 54h					8-bit	SIZE	
POWER	VCC					FFh	nDLY_RST DEFAULT	
BYTE0 BIT	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R							
BIT NAME	Receive Data							

The Receive Register is initialized to FFh after a read or after a Time-out has occurred.

The channel can be enabled to automatically transmit data (PS/2_EN=1) by setting PS/2_T/R while RDATA_RDY is set, however a transmission can not be kicked off until the data has been read from the Receive Register.

An interrupt is generated on the low to high transition of RDATA_RDY.

If a receive time-out (REC_TIMEOUT=1) or a transmit time-out (XMIT_TIMEOUT=1) occurs the channel is busied (CLK held low) for 300us (Hold Time) to ensure that the peripheral aborts. Writing to the Transmit Register will be allowed, however the data written will not be transmitted until the Hold Time expires.

All bits in this register are read only.

Note 10-2   In receive mode the RX_BUSY bit for a particular channel is set in the PS/2 Status Register.

10.3.3   CONTROL

TABLE 10-7: CONTROL REGISTER

BUS OFFSET	PS/2: 51h TP: 55h					8-bit	SIZE	
POWER	VCC					00h	nDLY_RST DEFAULT	
BYTE0 BIT	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R	R	R/W		R/W		R/W	R/W
BIT NAME	Reserved	Reserved	STOP		PARITY		PS/2_ EN	PS/2_ T/R

STOP

These bits are used to set the level of the stop bit expected by the PS/2 channel state machine. These bits are therefore only valid when PS/2_EN is set.

00=Receiver expects an active high stop bit.

01=Receiver expects an active low stop bit.

10=Receiver ignores the level of the Stop bit (11th bit is not interpreted as a stop bit).

11=Reserved.

PARITY

These bits are used to set the parity expected by the PS/2 channel state machine. These bits are therefore only valid when PS/2_EN is set.

00=Receiver expects Odd Parity (default).

01=Receiver expects Even Parity.

10=Receiver ignores level of the parity bit (10th bit is not interpreted as a parity bit).

11=Reserved

This register should be read to determine the status of Bits[1:0] prior to clearing by writing a 1 to that bit.

PS/2_EN

PS/2 Channel ENable (default = 0). When PS/2_EN is set, the PS/2 State machine is enabled allowing the channel to perform automatic reception or transmission depending on the bit value of PS/2_T/R. When PS/2_EN is cleared, the channel's automatic PS/2 state machine is disabled and the PW/2 channel's CLK pin driven low and DATA pin not driven.

Note:	If the PS/2_EN bit is cleared prior to the leading edge (falling edge) of the 10th (parity bit) clock edge the receive data is discarded (RDATA_RDY remains low). If the PS/2_EN bit is cleared following the leading edge of the 10th clock signal, then the receive data is saved in the Receive Register (RDATA_RDY goes high) assuming no parity error.

PS/2_T/R

PS/2 Channel Transmit/Receive (default = 0). Configures the PS/2 logic for automatic transmission when set or reception when cleared. This bit is only valid when PS/2_EN is set.

When set the PS/2 channel is enabled to transmit data. To properly initiate a transmit operation, this bit must be set prior to writing to the Transmit Register. Writes to the Transmit Register are blocked when this bit is cleared. Upon setting the PS/2_T/R bit, the channel will drive its CLK line low and then float the DATA line and hold this state until a write occurs to the Transmit Register or until the PS/2_T/R bit is cleared. Writing to the Transmit Register initiates the transmit operation. ECE1117 drives the data line low and, within 80ns, floats the clock line (externally pulled high by the pullup resistor) to signal to the external PS/2 device that data is now available. The PS/2_T/R bit is cleared on the 11th clock edge of the transmission or if a Transmit Time-out error condition occurs.

Note:	If the PS/2_T/R bit is set while the channel is actively receiving data prior to the leading edge of the 10th (parity bit) clock edge, the receive data is discarded. If this bit is not set prior to the 10th clock signal, then the receive data is saved in the Receive Register.

When the PS/2_T/R bit is cleared, the PS/2 channel is enabled to receive data. Upon clearing this bit, if RDATA_RDY is also cleared, the channel's CLK and DATA will float waiting for the external PS/2 device to signal the start of a transmission. If the PS/2_T/R bit is set while RDATA_RDY is set, then the channel's DATA line will float but its CLK line will be held low, holding off the peripheral, until the Receive Register is read.

10.3.4   STATUS

TABLE 10-8:   STATUS REGISTER

BUS OFFSET	PS/2: 52h TP: 56h					8-bit	**SIZE**	
POWER	VCC					10h	nDLY_RST **DEFAULT**	
BYTE0 BIT	D7	D6	D5	D4	D3	D2	D1	D0
TYPE	R/WC	R	R/WC	R	R/WC	R/WC	R/WC	R
BIT NAME	XMIT_START_TIMEOUT	RX_BUSY A	XMIT_TIMEOUT	XMIT_IDLE	FE	PE	REC_TIMEOUT	RDAT_RDY

PROGRAMMER'S NOTE: This register should be read to determine the status of Bits[7,5,3,2,1] prior to clearing by writing a 1 to that bit.

XMIT_START_TIMEOUT

When the XMIT_START_TIMEOUT bit is set, a start bit was not received within 25 ms following the transmit start event. Writing a '1' to the bit clears the XMIT_START_TIMEOUT bit. The XMIT_START_TIMEOUT bit is a 'sticky' bit and is intended to uniquely indicate the status of the transmit start bit time-out condition. This bit affects no other logic. Note that the transmit start bit time-out condition is also indicated by the XMIT_TIMEOUT bit.

PROGRAMMER'S NOTE: Always check that a PS/2 channel is idle, i.e. the RX_BUSY bit is clear, before attempting to transmit on that channel. Receive data may be lost by setting a PS/2 channel to transmit while the RX_BUSY bit is set depending where in the message frame the transmit mode change occurs.

This bit is cleared when written with a 1.

RX_BUSY

When a RX_BUSY bit is set, the associated channel is actively receiving PS/2 data; when a RX_BUSY bit is clear, the channel is idle. See Note 10-2 on page 65.

   Note 10-3   The Busy bit is set upon detection of a Start bit.

XMIT_TIMEOUT

When the XMIT_TIMEOUT bit is set, the PS/2_T/R bit is held clear, the PS/2 channel's CLK line is pulled low for a minimum of 300us until the PS/2 Status register is read. The XMIT_TIMEOUT bit is set on one of three transmit conditions: when the transmitter bit time (time between falling edges) exceeds 300us, when the transmitter start bit is not received within 25ms from signaling a transmit start event or if the time from the first bit (start) to the 10th bit (parity) exceeds 2ms.

This bit is cleared when written with a 1.

XMIT_IDLE

Transmitter Idle: When low, the XMIT_IDLE bit is a status bit indicating that the PS/2 channel is actively transmitting data to the PS/2 peripheral device. Writing to the Transmit Register when the channel is ready to transmit will cause the XMIT_IDLE bit to clear and remain clear until one of the following conditions occur: the falling edge of the 11th CLK, XMIT_TIMEOUT is set; the PS/2_T/R bit is cleared or the PS/2_EN bit is cleared.

   Note 10-4   An interrupt is generated on the low-to-high transition of XMIT_IDLE.

FE

Framing Error: When receiving data, the stop bit is clocked in on the falling edge of the 11th CLK edge. If the channel is configured to expect either a high or low stop bit and the 11th bit is contrary to the expected stop polarity, then the FE and REC_TIMEOUT bits are set following the falling edge of the 11th CLK edge and an interrupt is generated.

This bit is cleared when written with a 1.

PE

Parity Error: When receiving data, the parity bit is clocked in on the falling edge of the 10th CLK edge. If the channel is configured to expect either even or odd parity and the 10th bit is contrary to the expected parity, then the PE and REC_TIMEOUT bits are set following the falling edge of the 10th CLK edge and an interrupt is generated.

This bit is cleared when written with a 1.

REC_TIMEOUT

Following assertion of the REC_TIMEOUT bit, the channel's CLK line is automatically pulled low for a minimum of 300us until the PS/2 status register is read. Under PS/2 automatic operation, PS/2_EN is set, this bit is set on one of three receive error conditions:

   - When the receiver bit time (time between falling edges) exceeds 300us.
   - If the time from the first bit (start) to the 10th bit (parity) exceeds 2ms.
   - On a receive parity error along with the Parity Error (PE) bit.
   - On a receive framing error due to an incorrect STOP bit along with the framing error (FE) bit.

This bit is cleared when written with a 1.

   Note 10-5   An Interrupt is generated on the low-to-high transition of the REC_TIMEOUT bit.

RDATA_RDY

Receive Data Ready: Under normal operating conditions, this bit is set following the falling edge of the 11th clock given successful reception of a data byte from the PS/2 peripheral (i.e., no parity, framing, or receive time-out errors) and indicates that the received data byte is available to be read from the Receive Register. This bit may also be set in the event that the PS/2_EN bit is cleared following the 10th CLK edge. Reading the Receive Register clears this bit.

> **Note 10-6**   An Interrupt is generated on the low-to-high transition of the RDATA_RDY bit.

11.0 OPERATIONAL DESCRIPTION

11.1 Maximum Ratings

Maximum V_{CC} ....+5V

Negative Voltage on any pin, with respect to Ground ....-0.3V

Operating Temperature Range ....0°C to +70°C

Storage Temperature Range.. -55° to +150°C

Lead Temperature Range .... Refer to JEDEC Spec. J-STD-020

Note 11-1 Stresses above those listed above and below could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

11.2 DC Electrical Characteristics

TABLE 11-1: DC ELECTRICAL CHARACTERISTICS $T_A = 0°C – 70°C$, $V_{CC} = +3.3$ V ± 10%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
IO8 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4		3.6	V	IOH = -4mA
IOD8 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
IO12/20 Type Buffer						Note 11-3
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4		3.6	V	IOH = 12mA
IOD12/20 Type Buffer						Note 11-3
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 20mA

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PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IO16 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16mA
High Output Level	V_{OH}	2.4		3.6	V	IOH = -8mA
IOD16 Type Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0		5.5	V	
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16mA
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4		3.6	V	IOH = -4mA
OD8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
O12/20 Type Buffer						Note 11-3
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4		3.6	V	IOH = -12mA
OD12/20 Type Buffer						Note 11-3
Low Output Level	V_{OL}			0.4	V	I_{OL} = 20mA
O16 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16mA
High Output Level	V_{OH}	2.4		3.6	V	IOH = -8mA
OD16 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 16mA
Leakage Current (ALL – except Buffers)						Note 11-2
Input High Current	$ILEAK_{IH}$			10	µA	V_{IN} = V_{CC}
Input Low Current	$ILEAK_{IL}$			-10	µA	V_{IN} = 0V
Pull Down Impedance 5 Volt Tolerant pins	PD	50	73	111	KOhms	See Note 11-4 and Note 11-5
Pull UP Impedance for 5 Volt Tolerant pins	PU	44	73	134	KOhms	See Note 11-4 and Note 11-5.
Pull Down Impedance for I/O/OD 12/20ma buffer type (Used only where noted)	PD	42	73	388	KOhms	See Note 11-4 and Note 11-5.
Pull UP Impedance for I/O/OD 12/20ma buffer type (Used only where noted)	PU	49	73	297	KOhms	See Note 11-4 and Note 11-5.

TABLE 11-1: **DC ELECTRICAL CHARACTERISTICS** $T_A = 0^{O}C - 70^{O}C$, V_{CC} = +3.3 V ± 10%

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
5 K Pull Down Impedance (Used only where noted)	PD	2.5	5	7.5	KOhms	See Note 11-4 and Note 11-5.
• Voltages are measured from the local ground potential, unless otherwise specified.						
• Typicals are at TA=25°C and represent most likely parametric norm.						
• The maximum allowable power dissipation at any temperature is PD = (TJmax - TA) / QJA.						
• Timing specifications are tested at the TTL logic levels, VIL=0.4V for a falling edge and VIH=2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.						
• All pins except power and ground are 5V tolerant and back drive protected						

Note 11-2 Leakage currents are measured with all pins in high impedance.

Note 11-3 This pin can sink 20ma when selected as an open drain buffer. This pin can source or sink 12ma when selected as a push-pull buffer. The internal pullup with an impedance of 5.0 ± 50% KOHMS. These pins have specific notes in Section 2.0, " Pin Configuration and Signal Description," on page 5. See Section 2.2.2, "SMBus Interface," on page 6 and Section 2.4, "Notes for the Tables in this Chapter," on page 17.

Note 11-4 See GPIO Configuration Register on page 48 for register definition and Register Summary Table 1 of 6 on page 35 specific pin defaults Pullup/Pulldown, Open Drain/Pushpull configurations. Also see General Rules for GPIO Configuration Register described in Section 2.3, "Pin Signal Function Multiplexing," on page 8 and Section 2.3.1, "Exceptions to the GPIO Configuration Register Rules," on page 9.

Note 11-5 Unless otherwise noted all internal pullups and pulldowns have their impedances characteristics defined in Table 11-1 as "Impedance for 5 Volt Tolerant pins". All exceptions have specific notes called out in Section 2.0, " Pin Configuration and Signal Description," on page 5. These notes are defined in Section 2.4, "Notes for the Tables in this Chapter," on page 17. and refer to the following pullup/pulldown impedances exceptions:

1. Pull Down Impedance for I/O/OD 12/20ma buffer type (Used only where noted)
2. Pull UP Impedance for I/O/OD 12/20ma buffer type (Used only where noted)
3. 5 K Pull Down Impedance (Used only where noted)

The Pullup impedance exceptions listed above are also have their impedances characteristics defined in Table 11-1.

11.3 Power Consumption

TABLE 11-2: **VCC SUPPLY CURRENT, REV. B**

PARAMETER	SYMBOL	MIN	TYP (3.3V, 25°V)	MAX (3.6V, 70°V)	UNITS	COMMENTS
VCC Supply at FULL POWER on page 27	I_{CC}		1.5	2.0	mA	See Note 11-6.
VCC Supply at SYSTEM LIGHT SLEEP on page 27	I_{CC}		1.0	1.5	mA	See Note 11-6.
VCC Supply at SYSTEM DEEP SLEEP on page 27	I_{CC}		0.5	1.0	mA	See Note 11-6.

Note 11-6 The Supply Current values are the results of characterization.

TABLE 11-3:   VCC SUPPLY CURRENT, REV. C

PARAMETER	SYMBOL	MIN	TYP (3.3V, 25°V)	MAX (3.6V, 70°V)	UNITS	COMMENTS
VCC Supply at FULL POWER on page 27	I$_{CC}$		1.5	2.0	mA	See Note 11-6.
VCC Supply at SYSTEM LIGHT SLEEP on page 27	I$_{CC}$		1.0	1.5	mA	See Note 11-6.
VCC Supply at SYSTEM DEEP SLEEP on page 27	I$_{CC}$		90	130	uA	See Note 11-6.

11.4   Capacitance Values for Pins

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 3.3V ±10%

TABLE 11-4:   CAPACITANCE VALUES FOR PINS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C$_{IN}$			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C$_{IN}$			10	pF	
Output Capacitance	C$_{OUT}$			20	pF	

Note 11-7   The input capacitance of a port is measured at the connector pins.

12.0 TIMING DIAGRAMS

12.1 VCC Power

FIGURE 12-1: VCC POWER
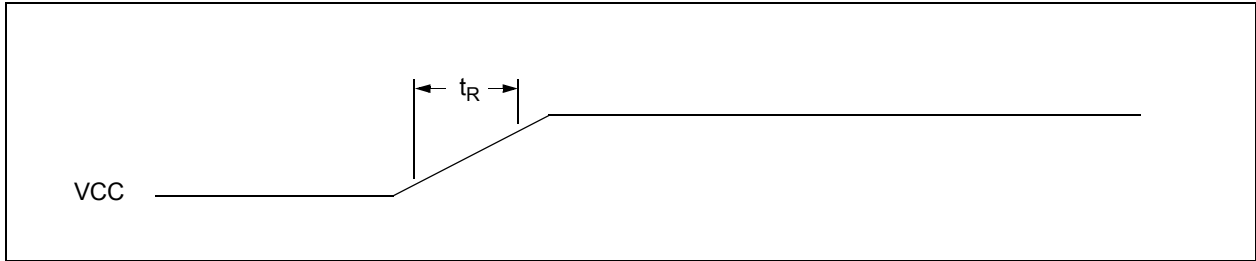
TABLE 12-1: VCC POWER PARAMETERS

SYMBOL	PARAMETER	LIMITS		UNITS	COMMENTS
		MIN	MAX		
t_R	VCC Rise time, 10% to 90%	0.150	30	msec	

12.2 BC-Link™ Timing

Refer to the LSBC Bus Specification.

FIGURE 12-2: BC-LINK™ TIMING

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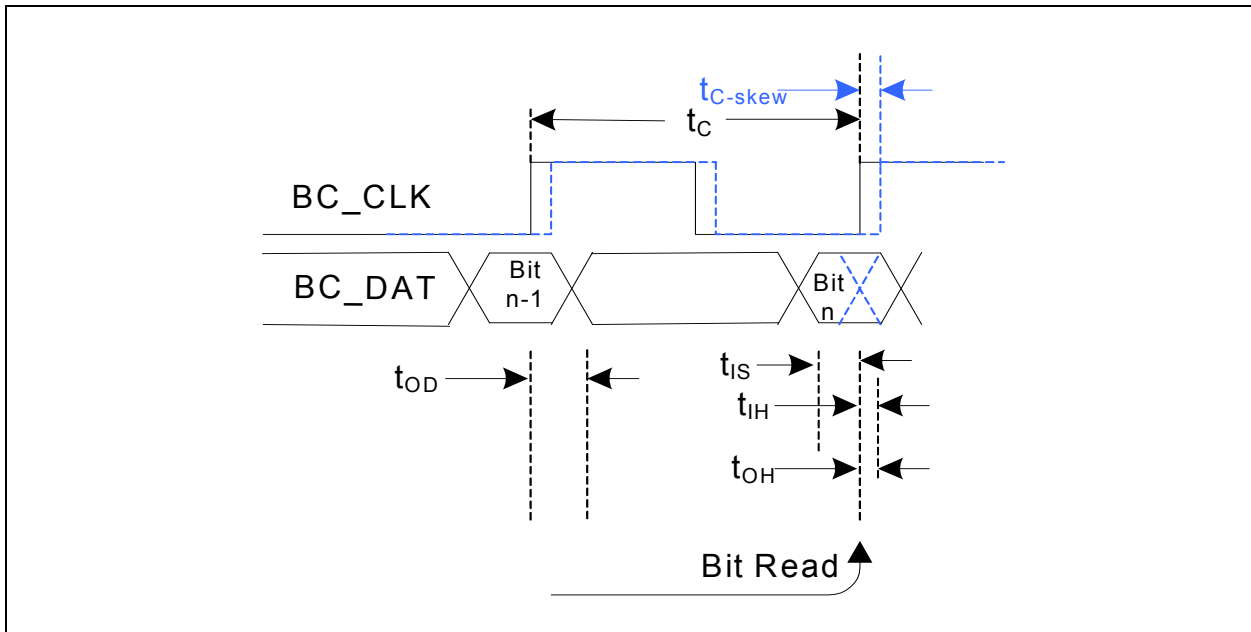
TABLE 12-2: BC-LINK™ UPSTREAM TIMING DIAGRAM PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_C	BC Clock Frequency		2.93	3.08	Mhz
	High Spec BC Clock Period	324.7	341.0		nsec
t_{OD}	BC-Link Upstream DATA output delay after rising edge of CLK.			20	nsec
t_{OH}	Upstream Data output hold time after falling edge of CLK	0			nsec
t_{IS}	BC-Link Upstream DATA input setup time before rising edge of CLK.	30			nsec
t_{IH}	BC-Link Upstream DATA input hold time after rising edge of CLK.	0			nsec
t_{C-Skew}	BC-Link Upstream DATA input allowed to be invalid before rising edge of CLK. (aka negative hold time)	5			nsec

12.3   SMBus Timing

FIGURE 12-3:   SMBUS TIMING
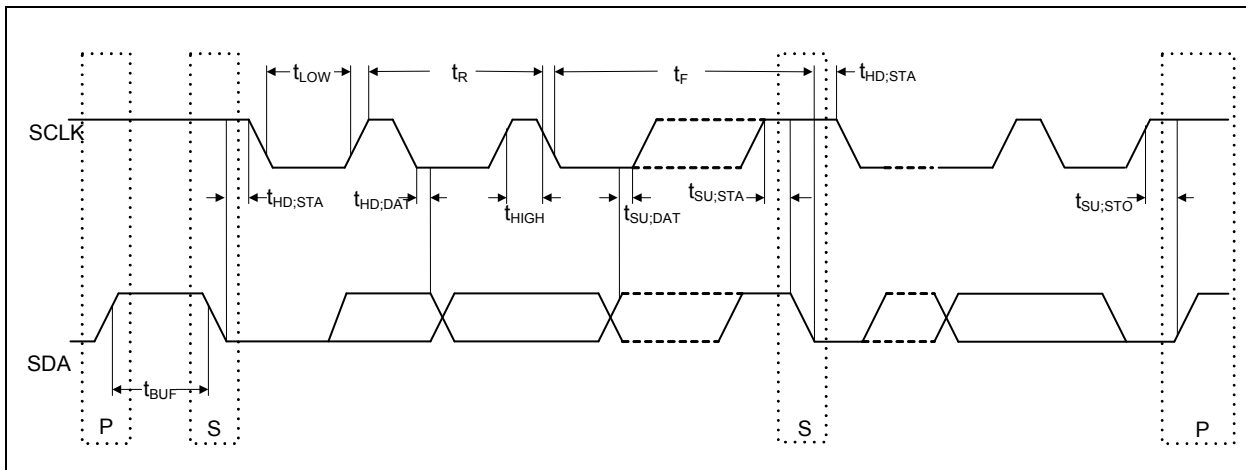
TABLE 12-3:   SMBUS TIMING PARAMETERS

SYMBOL	PARAMETER	LIMITS		UNITS	COMMENTS
		MIN	MAX		
Fsmb	SMB Operating Frequency	10	400	KHz	Note 12-1
Tsp	Spike Suppression		50	ns	Note 12-2
Tbuf	Bus free time between Stop and Start Condition	1.3		µs	
Thd:sta	Hold time after (Repeated) Start Condition. After this period, the first clock is generated.	0.6		µs	
Tsu:sta	Repeated Start Condition setup time	0.6		µs	
Tsu:sto	Stop Condition setup time	0.6		µs	
Thd:dat	Data hold time	0.3	0.9	µs	
Tsu:dat	Data setup time	100		ns	Note 12-3

TABLE 12-3:   SMBUS TIMING PARAMETERS (CONTINUED)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS	COMMENTS
Tlow	Clock low period	1.3		μs	
Thigh	Clock high period	0.6		μs	
Tf	Clock/Data Fall Time	$20+0.1C_b$	300	ns	
Tr	Clock/Data Rise Time	$20+0.1C_b$	300	ns	
C_b	Capacitive load for each bus line		400	pF	

Note 12-1   The max SMBus timing operating frequency exceeds that specified in the System Management Bus Specification, Rev 1.1, but corresponds to the maximum clock frequency for fast mode devices on the I^2C bus (see the I^2C Bus Specification).

Note 12-2   At 400kHz, the input filter suppresses spikes of a maximum pulse width of 50ns.

Note 12-3   if using 100 KHz clock frequency, the next data bit output to the SDA line will be 1250 ns (1000 ns (TR max) + 250 ns (TSU:DAT min) @ 100 kHz) before the SCLK line is released.

12.4   PS/2 Interface Timing Diagrams

FIGURE 12-4:   PS/2 TRANSMIT TIMING
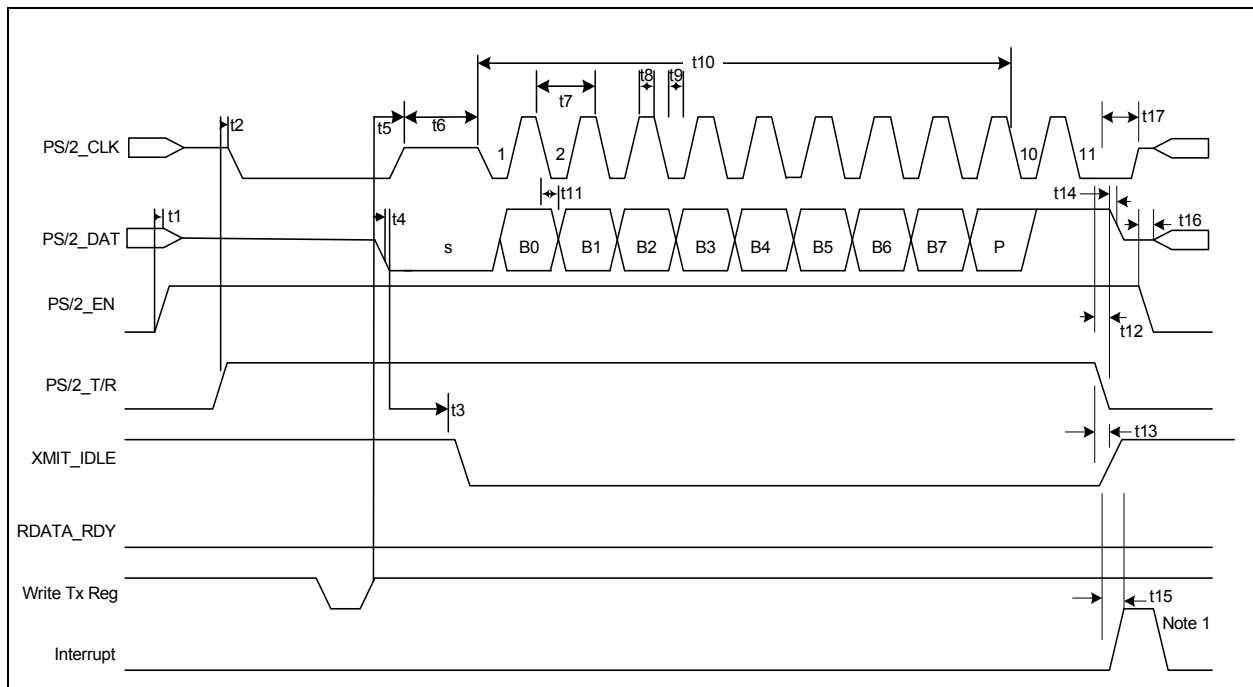
TABLE 12-4:   PS/2 CHANNEL TRANSMISSION TIMING PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	The PS/2 Channel's CLK and DATA lines are floated following PS/2_EN=1 and PS/2_T/R=0.			1000	ns
t2	PS/2_T/R bit set to CLK driven low preparing the PS/2 Channel for data transmission.				
t3	CLK line floated to XMIT_IDLE bit deasserted.			1.7	μs

TABLE 12-4: **PS/2 CHANNEL TRANSMISSION TIMING PARAMETERS (CONTINUED)**

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t4	Trailing edge of 8051 WR of Transmit Register to DATA line driven low.	45		90	ns
t5	Trailing edge of EC WR of Transmit Register to CLK line floated.	90		130	
t6	Initiation of Start of Transmit cycle by the PS/2 channel controller to the auxiliary peripheral's responding by latching the Start bit and driving the CLK line low.	0.002		25.003	ms
t7	Period of CLK	60		302	µs
t8	Duration of CLK high (active)	30		151	
t9	Duration of CLK low (inactive)				
t10	Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk).			2.002	ms
t11	DATA output by ECE1117 following the falling edge of CLK. The auxiliary peripheral device samples DATA following the rising edge of CLK.	3.5		7.1	µs
t12	Rising edge following the 11th falling clock edge to PS_T/R bit driven low.	0		800	ns
t13	Trailing edge of PS_T/R to XMIT_IDLE bit asserted.			500	
t14	DATA released to high-Z following the PS/2_T/R bit going low.				
t15	XMIT_IDLE bit driven high to interrupt generated. Note1- Interrupt is cleared by writing a 1 to the status bit in the PS/2 Interrupt Status Register.				
t16	The PS/2 Channel's CLK and DATA lines are driven to the values stored in the WR_CLK and WR_DATA bits of the Control Register when PS/2_EN is written to 0.				
t17	Trailing edge of CLK is held low prior to going high-Z				

FIGURE 12-5: PS/2 RECEIVE TIMING
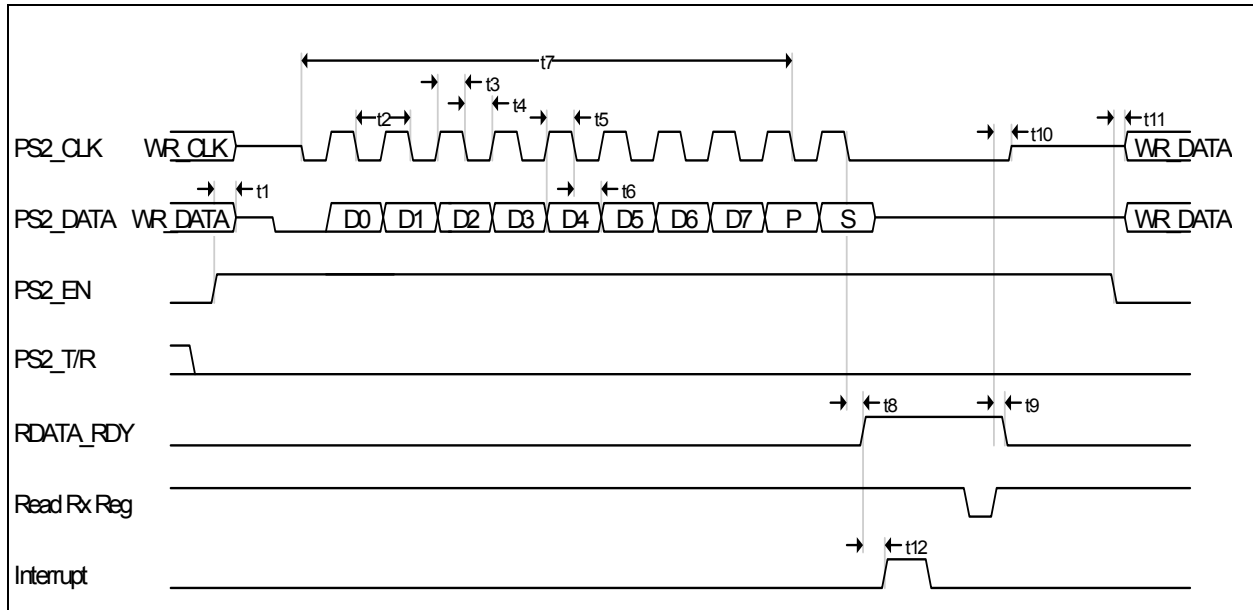
TABLE 12-5: PS/2 CHANNEL RECEIVE TIMING DIAGRAM PARAMETERS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	The PS/2 Channel's CLK and DATA lines are floated following PS/2_EN=1 and PS/2_T/R=0.			1000	ns
t2	Period of CLK	60		302	µs
t3	Duration of CLK high (active)	30		151	
t4	Duration of CLK low (inactive)				
t5	DATA setup time to falling edge of CLK. ECE1117 samples the data line on the falling CLK edge.	1			
t6	DATA hold time from falling edge of CLK. ECE1117 samples the data line on the falling CLK edge.	2			
t7	Duration of Data Frame. Falling edge of Start bit CLK (1st clk) to falling edge of Parity bit CLK (10th clk).			2.002	ms
t8	Falling edge of 11th CLK to RDATA_RDY asserted.			1.6	µs

TABLE 12-5:   PS/2 CHANNEL RECEIVE TIMING DIAGRAM PARAMETERS (CONTINUED)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t9	Trailing edge of the EC's RD signal of the Receive Register to RDATA_RDY bit deasserted.			500	ns
t10	Trailing edge of the EC's RD signal of the Receive Register to the CLK line released to high-Z.				
t11	The PS/2 Channel's CLK and DATA lines are driven to the values stored in the WR_CLK and WR_DATA bits of the Control Register when PS/2_EN is written to 0.				
t12	RDATA_RDY asserted an interrupt is generated. **Note:** Interrupt is cleared by writing a 1 to the bit in PS/2 Interrupt Status Register.				

12.5   Asynchronous Input Signal Timing

The following pin signals function inputs are asynchronous and the minimum input signal pulse width ensured to be detected is 5ns. No filtering is done to prevent detection of narrower signals:

• GPIO[23:00]
• KSI[7:0]

12.6   Synchronous Input signal Timing

The following pin signals function inputs are synchronous and generally used in static mode; however the minimum input signal pulse width ensured to be detected is 2(/10MHz-5%) = 10.5us. No filtering is done to prevent detection of narrower signals:

• SMB_ADDR
• TEST_PIN

APPENDIX A: REVISION HISTORY

TABLE A-1: DATA SHEET REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00001860D (09-23-15)	Product Features on page 1	Added sub-bullet under package bullet for 48-pin SQFN.
	FIGURE 2-1: ECE1117 Package Configuration on page 5	Removed QFN from figure title.
	Table 2-1, "ECE1117 Pin Configuration," on page 5	Removed QFN from table title.
	Section 2.8, "Package Outline Drawings," on page 19	Removed QFN from section title. Added 48-SQFN Package drawing.
	Product Identification System on page 81	Added package information for 48-pin SQFN. Added Note 4 stating "48-pin SQFN available in production with Tape and Reel only. "
DS00001860C (06-22-15)	FIGURE 3-1: Power and Resets Block Diagram on page 23	Diagram modified; series resistor added
	Table 2-9, "Power Interface," on page 8	The following text is removed from pin 21: "(Capacitor Required)"
	Section 2.4, "Notes for the Tables in this Chapter," on page 17	Updated Note 4 to include the requirement for a series resistor on the VR_-CAP pin.
DS00001860B (02-11-15)	Table 11-3, "VCC Supply Current, Rev. C," on page 72	Updated max deep sleep current
DS00001860A (11-26-14)	Document Release	

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PART NO.[1] - **XXX**[2, 4] - **[X]** - **[X]**[3]

Device **Package** **Functional Revision** **Tape and Reel Option**

Device:	ECE1117[1]
Package:	HZH = 48-pin QFN[2]
	Y3 = 48-pin SQFN[2, 4]
Functional Revision Option:	Blank = Rev. B
	1 = Rev. C
Tape and Reel Option:	Blank = Tray packaging
	TR = Tape and Reel[3]

Examples:

a) ECE1117-HZH= QFN, Rev. B, Tray package
b) ECE1117-HZH-1-TR= QFN, Rev. C, Tape and Reel
c) ECE1117-Y3-TR= SQFN, Rev. B, Tape and Reel
d) ECE1117-Y3-1-TR= SQFN, Rev. C, Tape and Reel

Note 1: These products meet the halogen maximum concentration values per IEC61249-2-21.

Note 2: All package options are RoHS compliant. For RoHS compliance and environmental information, please visit http://www.micro-chip.com/pagehandler/en-us/aboutus/ehs.html .

Note 3: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Note 4: 48-pin SQFN available in production with Tape and Reel only.

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