

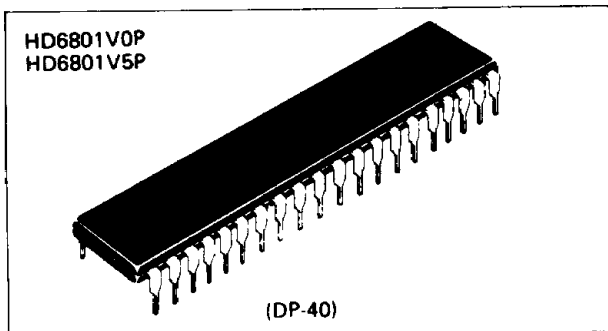
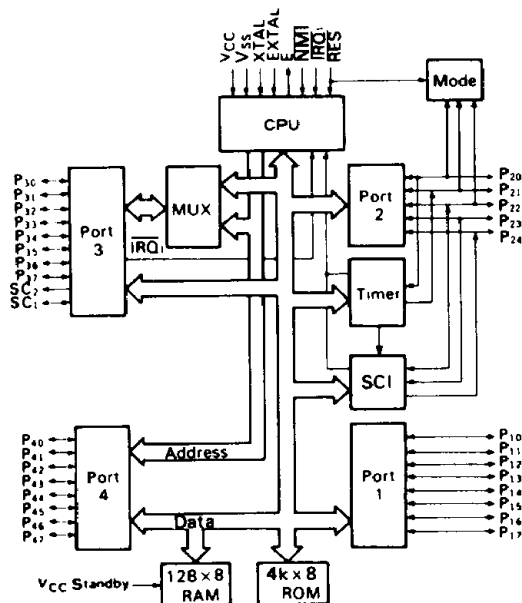
HD6801V0, HD6801V5 MCU (Microcomputer Unit)

The HD6801V MCU is an 8-bit microcomputer unit which is compatible with the HD6801S except the ROM size. The HD6801V MCU is object code compatible with the HD6800 with improved execution times of key instructions plus several new 16-bit and 8-bit instructions including an 8x8 unsigned multiply with 16-bit result. The HD6801V MCU can operate as a single chip microcomputer or be expanded to 65k bytes. The HD6801V MCU is TTL compatible and requires one +5.0 volt power supply. The HD6801V MCU has 4k bytes of ROM and 128 bytes of RAM on chip. Serial Communications Interface (SCI), and parallel I/O as well as a three function 16-bit timer. Features and Block diagram of the HD6801V include the following:

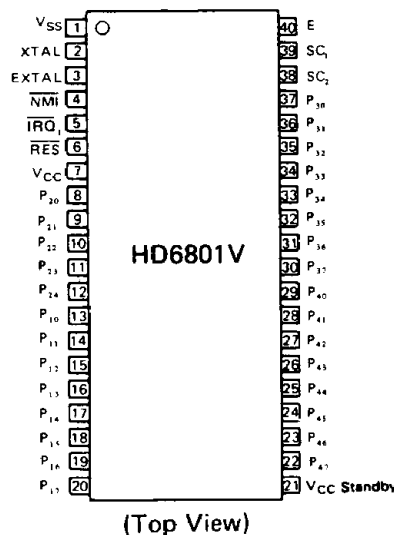
■ FEATURES

- Expanded HMCS6800 Instruction Set
- 8 x 8 Multiply
- On-Chip Serial Communication Interface (SCI)
- Object Code Compatible With The HD6800 MPU
- 16-Bit Timer
- Single Chip Or Expandable To 65k Bytes
- 4k Bytes Of ROM
- 128 Bytes Of RAM (64 Bytes Retainable On Power Down)
- 29 Parallel I/O Lines And 2 Handshake Control Lines
- Internal Clock/Divided-By-Four Circuitry
- TTL Compatible Inputs And Outputs
- Interrupt Capability
- Compatible with MC6801 (except ROM size)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ TYPE OF PRODUCTS

MCU	Bus Timing
HD6801V0	1 MHz
HD6801V5	1.25 MHz

■ PROGRAM DEVELOPMENT SUPPORT TOOLS

- Cross assembler software for use with IBM PCs and compatibles
- In circuit emulator for use with IBM PCs and compatibles



HD6801V0, HD6801V5

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC}^*	-0.3 ~ +7.0	V
Input Voltage	V_{in}^*	-0.3 ~ +7.0	V
Operating Temperature	T_{opr}	0 ~ +70	°C
Storage Temperature	T_{stg}	-55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0 \sim +70^\circ C$, unless otherwise noted.)

Item	Symbol	Test Condition	min	typ	max	Unit	
Input "High" Voltage	RES		4.0	-	V_{CC}	V	
	Other Inputs*		2.0	-	V_{CC}		
Input "Low" Voltage	EXTAL		-0.3	-	0.6	V	
	Other Inputs*		-0.3	-	0.8		
Input Load Current	$P_{40} \sim P_{47}$	$V_{in} = 0 \sim 2.4V$	-	-	0.5	mA	
	SC_1		-	-	0.8		
	EXTAL		-	-	1.2		
Input Leakage Current	NMI, IRQ_1 , RES	$V_{in} = 0 \sim 5.25V$	-	-	2.5	μA	
Three State (Offset) Leakage Current	$P_{10} \sim P_{17}$, $P_{30} \sim P_{37}$	$V_{in} = 0.5 \sim 2.4V$	-	-	10	μA	
	$P_{20} \sim P_{24}$		-	-	100		
Output "High" Voltage	$P_{30} \sim P_{37}$	V_{OH}	$I_{LOAD} = -205 \mu A$	2.4	-	V	
	$P_{40} \sim P_{47}$, E, SC_1 , SC_2		$I_{LOAD} = -145 \mu A$	2.4	-		
	Other Outputs		$I_{LOAD} = -100 \mu A$	2.4	-		
Output "Low" Voltage	All Outputs	V_{OL}	$I_{LOAD} = 1.6 mA$	-	-	0.5	V
Darlington Drive Current	$P_{10} \sim P_{17}$	$-I_{OH}$	$V_{out} = 1.5V$	1.0	-	10.0	mA
Power Dissipation		P_D		-	-	1200	mW
Input Capacitance	$P_{30} \sim P_{37}$, $P_{40} \sim P_{47}$, SC_1	C_{in}	$V_{in} = 0V$, $T_a = 25^\circ C$, $f = 1.0 MHz$	-	-	12.5	pF
	Other Inputs			-	-	10.0	
V_{CC} Standby	Powerdown	V_{SBB}		4.0	-	5.25	V
	Operating	V_{SB}		4.75	-	5.25	
Standby Current	Powerdown	I_{SBB}	$V_{SBB} = 4.0 V$	-	-	8.0	mA

*Except Mode Programming Levels.



● AC CHARACTERISTICS

BUS TIMING ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0 \sim +70^\circ C$, unless otherwise noted.)

Item	Symbol	Test Condition	HD6801V0			HD6801V5			Unit	
			min	typ	max	min	typ	max		
Cycle Time	t_{cyc}	Fig. 1 Fig. 2	1	—	10	0.8	—	10	μs	
Address Strobe Pulse Width "High" *	PW_{ASH}		200	—	—	150	—	—	ns	
Address Strobe Rise Time	t_{ASr}		5	—	50	5	—	50	ns	
Address Strobe Fall Time	t_{ASf}		5	—	50	5	—	50	ns	
Address Strobe Delay Time *	t_{ASD}		60	—	—	30	—	—	ns	
Enable Rise Time	t_{Er}		5	—	50	5	—	50	ns	
Enable Fall Time	t_{Ef}		5	—	50	5	—	50	ns	
Enable Pulse Width "High" Time *	PW_{EH}		450	—	—	340	—	—	ns	
Enable Pulse Width "Low" Time *	PW_{EL}		450	—	—	350	—	—	ns	
Address Strobe to Enable Delay Time *	t_{ASED}		60	—	—	30	—	—	ns	
Address Delay Time	t_{AD}		—	—	260	—	—	260	ns	
Address Delay Time for Latch *	t_{ADL}		—	—	270	—	—	260	ns	
Data Set-up Write Time	t_{DSW}		225	—	—	115	—	—	ns	
Data Set-up Read Time	t_{DSR}		80	—	—	80	—	—	ns	
Data Hold Time	Read		t_{HR}	10	—	—	10	—	—	ns
	Write		t_{HW}	20	—	—	20	—	—	
Address Set-up Time for Latch *	t_{ASL}		60	—	—	20	—	—	ns	
Address Hold Time for Latch	t_{AHL}		20	—	—	20	—	—	ns	
Address Hold Time	t_{AH}		20	—	—	20	—	—	ns	
Peripheral Read Access Time	Non-Multiplexed Bus*		t_{ACCN}	—	—	(610)	—	—	(410)	ns
	Multiplexed Bus*	t_{ACCM}	—	—	(600)	—	—	(410)		
Oscillator stabilization Time	t_{RC}	Fig. 10 Fig. 11	100	—	—	100	—	—	ms	
Processor Control Set-up Time	t_{PCS}		200	—	—	200	—	—	ns	

*These timings change in approximate proportion to t_{cyc} . The figures in this characteristics represent those when t_{cyc} is minimum (=in the highest speed operation).

PERIPHERAL PORT TIMING ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0 \sim +70^\circ C$, unless otherwise noted.)

Item	Symbol	Test Condition	min	typ	max	Unit	
Peripheral Data Setup Time	Port 1, 2, 3, 4	t_{PDSU}	Fig. 3	200	—	—	ns
Peripheral Data Hold Time	Port 1, 2, 3, 4	t_{PDH}	Fig. 3	200	—	—	ns
Delay Time, Enable Positive Transition to $\overline{OS3}$ Negative Transition		t_{OSD1}	Fig. 5	—	—	350	ns
Delay Time, Enable Positive Transition to $\overline{OS3}$ Positive Transition		t_{OSD2}	Fig. 5	—	—	350	ns
Delay Time, Enable Negative Transition to Peripheral Data Valid	Port 1, 2*, 3, 4	t_{PWD}	Fig. 4	—	—	400	ns
Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid	Port 2**, 4	t_{CMOS}	Fig. 4	—	—	2.0	μs
Input Strobe Pulse Width		t_{PWIS}	Fig. 6	200	—	—	ns
Input Data Hold Time	port 3	t_{IH}	Fig. 6	50	—	—	ns
Input Data Set-up Time	Port 3	t_{IS}	Fig. 6	20	—	—	ns

*Except P₂₁ **10k Ω pull up register required for Port 2



HD6801V0, HD6801V5

TIMER, SCI TIMING ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0 \sim +70^\circ C$, unless otherwise noted.)

Item	Symbol	Test Condition	min	typ	max	Unit
Timer Input Pulse Width	t_{PWT}		$2t_{cyc}+200$	—	—	ns
Delay Time, Enable Positive Transition to Timer Out	t_{TOD}	Fig. 7	—	—	600	ns
SCI Input Clock Cycle	t_{Scyc}		1	—	—	t_{cyc}
SCI Input Clock Pulse Width	t_{PWCK}		0.4	—	0.6	t_{Scyc}

MODE PROGRAMMING ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_a = 0 \sim +70^\circ C$, unless otherwise noted.)

Item	Symbol	Test Condition	min	typ	max	Unit
Mode Programming Input "Low" Voltage	V_{MPL}	Fig. 8	—	—	1.7	V
Mode Programming Input "High" Voltage	V_{MPH}		4.0	—	—	V
RES "Low" Pulse Width	PW_{RSTL}		3.0	—	—	t_{cyc}
Mode Programming Set-up Time	t_{MPS}		2.0	—	—	t_{cyc}
Mode Programming Hold Time	RES Rise Time $\geq 1\mu s$	t_{MPH}	0	—	—	ns
	RES Rise Time $< 1\mu s$		100	—	—	

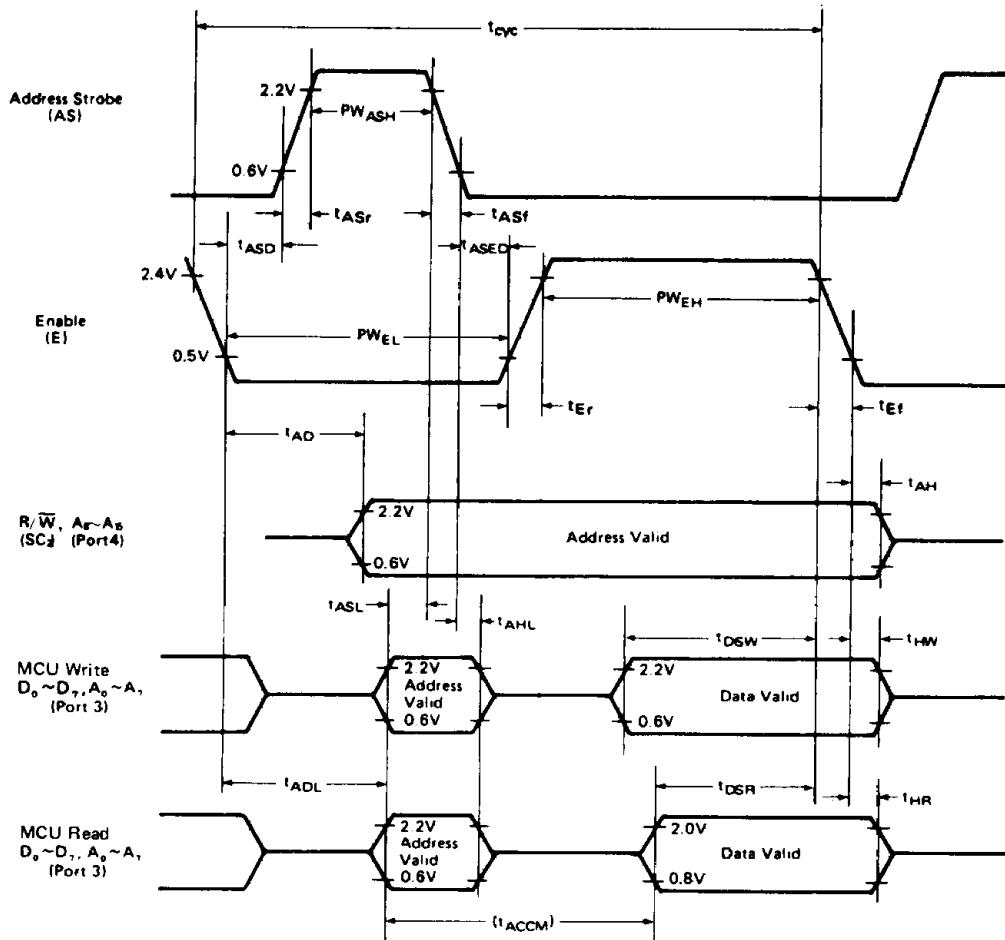


Figure 1 Expanded Multiplexed Bus Timing



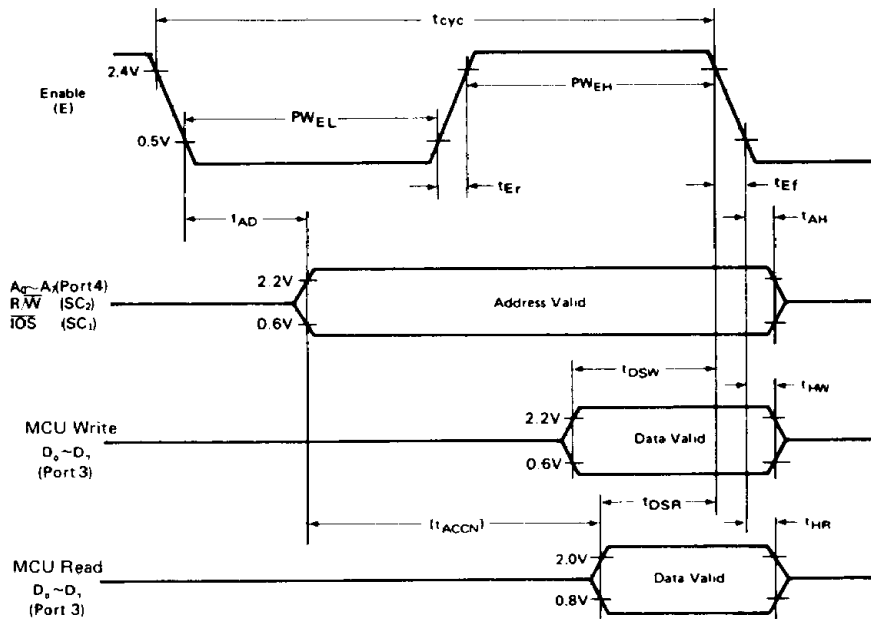
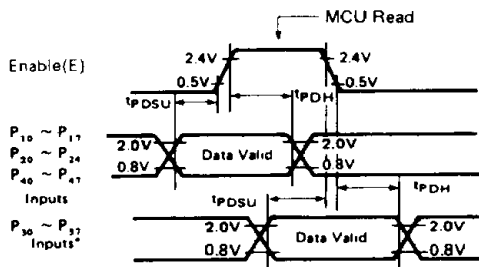
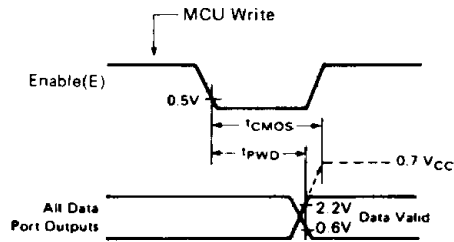


Figure 2 Expanded Non-Multiplexed Bus Timing



*Port 3 Non-Latched Operation (LATCH ENABLE = 0)

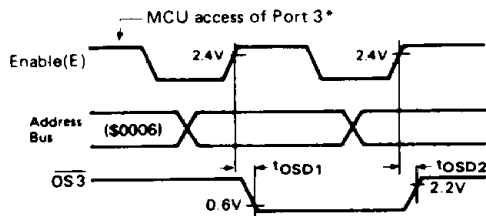
Figure 3 Data Set-up and Hold Times (MCU Read)



(Note)

1. 10 kΩ Pullup resistor required for Port 2 to reach 0.7 V_{CC}
2. Not applicable to P₂₁
3. Port 4 cannot be pulled above V_{CC}

Figure 4 Port Data Delay Timing (MCU Write)



*Access matches Output Strobe Select (OSS = 0, a read. OSS = 1, a write)

Figure 5 Port 3 Output Strobe Timing (Single Chip Mode)

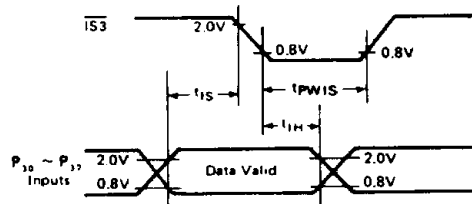


Figure 6 Port 3 Latch Timing (Single Chip Mode)

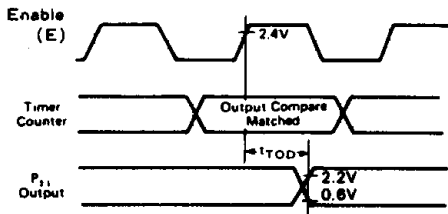


Figure 7 Timer Output Timing

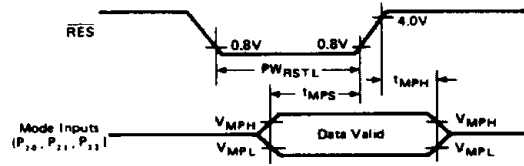
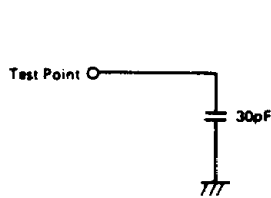
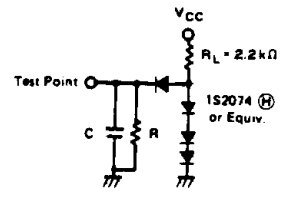


Figure 8 Mode Programming Timing



(a) CMOS Load



$C = 90 \text{ pF}$ for $P_{10} \sim P_{12}, P_{10} \sim P_{12}, E, SC_1, SC_2$
 $= 30 \text{ pF}$ for $P_{10} \sim P_{11}, P_{10} \sim P_{11}, E, SC_1, SC_2$
 $R = 12 \text{ k}\Omega$ for $P_{10} \sim P_{11}, P_{10} \sim P_{11}, E, SC_1, SC_2$
 $= 24 \text{ k}\Omega$ for $P_{10} \sim P_{11}, P_{10} \sim P_{11}$

(b) TTL Load

Figure 9 Bus Timing Test Loads

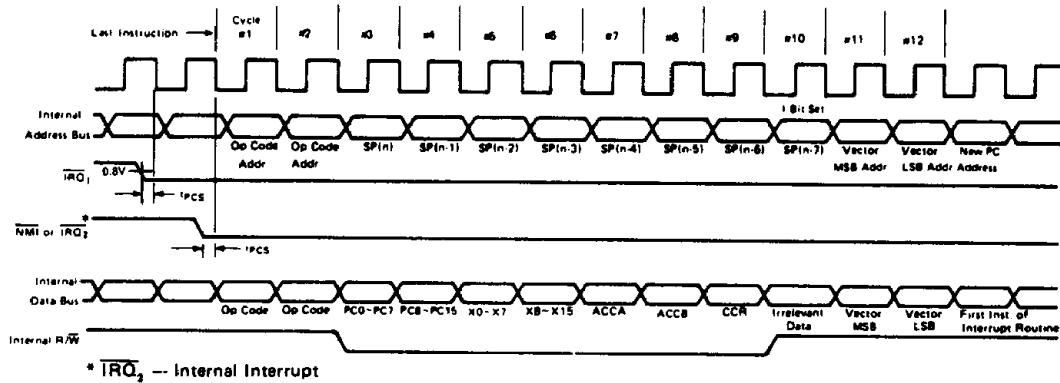


Figure 10 Interrupt Sequence

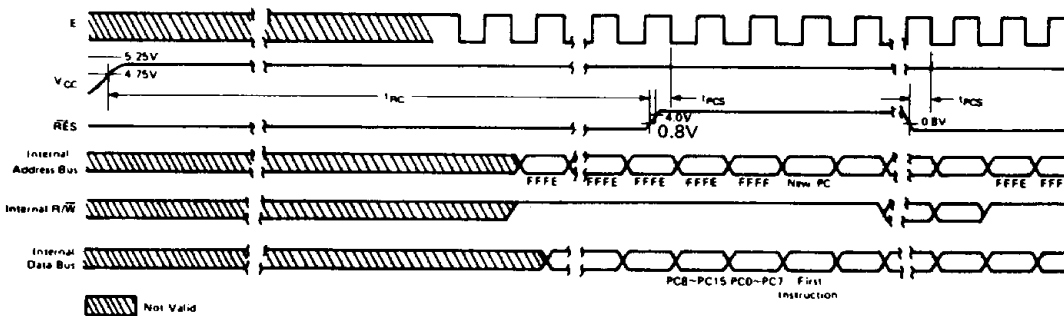


Figure 11 Reset Timing

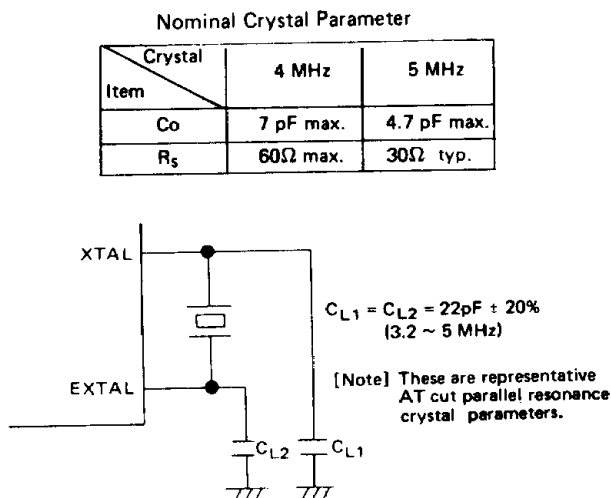
■ SIGNAL DESCRIPTIONS

● VCC and VSS

These two pins are used to supply power and ground to the chip. The voltage supplied will be +5 volts ±5%.

● XTAL and EXTAL

These connections are for a parallel resonant fundamental crystal, AT cut. Divide-by-4 circuitry is included with the internal clock, so a 4 MHz crystal may be used to run the system at 1 MHz. The divide-by-4 circuitry allows for use of the inexpensive 3.58 MHz Color TV crystal for non-time critical applications. Two 22pF capacitors are needed from the two crystal pins to ground to insure reliable operation. An example of the crystal interface is shown in Fig. 12. EXTAL may be driven by an external TTL compatible clock source with a 45% to 55% duty cycle. It will divide by 4 any frequency less than or equal to 5 MHz. XTAL must be grounded if an external clock is used.

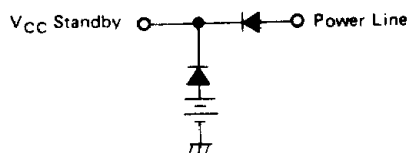


● VCC Standby

This pin will supply +5 volts ±5% to the standby RAM on the chip. The first 64 bytes of RAM will be maintained in the power down mode with 8 mA current max. The circuit of figure 13 can be utilized to assure that VCC Standby does not go below V_{SBB} during power down.

To retain information in the RAM during power down the following procedure is necessary:

- 1) Write "0" into the RAM enable bit, RAME. RAME is bit 6 of the RAM Control Register at location \$0014. This disables the standby RAM, thereby protecting it at power down.
- 2) Keep VCC Standby greater than V_{SBB}.



● Reset (RES)

This input is used to reset and start the CPU from a power down condition, resulting from a power failure or an initial startup of the processor. On power up, the reset must be held "Low" for at least 100 ms. When reset during operation, RES must be held "Low" at least 3 clock cycles.

When a "High" level is detected, the MCU does the following:

- 1) All the higher order address lines will be forced "High".
- 2) I/O Port 2 bits 2, 1, and 0 are latched into programmed control bits PC2, PC1 and PC0.
- 3) The last two (\$FFFE, \$FFFF) locations in memory will be used to load the program addressed by the program counter.
- 4) The interrupt mask bit is set. Clear before the CPU can recognize maskable interrupts.

● Enable (E)

This supplies the external clock for the rest of the system when the internal oscillator is used. It is a single phase, TTL compatible clock, and will be the divide-by-4 result of the crystal oscillator frequency. It will drive one TTL load and 90 pF capacitance.

● Non-Maskable Interrupt (NMI)

A low-going edge on this input requests that a non-maskable-interrupt sequence be generated within the processor. As with interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the NMI signal. The interrupt mask bit in the Condition Code Register has no effect on NMI.

In response to an NMI interrupt, the Index Register, Program Counter, Accumulators, and Condition Code Register are stored on the stack. At the end of the sequence, a 16-bit address will be loaded that points to a vectored address located in memory locations \$FFFC and \$FFFD. An address loaded at these locations causes the CPU to branch to a non-maskable interrupt service routine in memory.

A 3.3 kΩ external resistor to VCC should be used for wire-OR and optimum control of interrupts.

Inputs \overline{IRQ}_1 and NMI are hardware interrupt lines that are sampled during E and will start the interrupt routine on the \overline{E} following the completion of an instruction.

● Interrupt Request (\overline{IRQ}_1)

This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will complete the current instruction before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored on the stack. Next the CPU will respond to the interrupt request by setting the interrupt mask bit "High" so that no further maskable interrupts may occur. At the end of the cycle, a 16-bit address will be loaded that points to a vectored address which is located in memory locations \$FFF8 and \$FFF9. An address loaded at these locations causes the CPU to branch to an interrupt routine in memory.

The \overline{IRQ}_1 requires a 3.3 kΩ external resistor to VCC which should be used for wire-OR and optimum control of interrupts. Internal Interrupts will use an internal interrupt line (\overline{IRQ}_2). This interrupt will operate the same as \overline{IRQ}_1 except that it will use the vector address of \$FFF0 through \$FFF7. \overline{IRQ}_1 will have priority over \overline{IRQ}_2 if both occur at the same time. The Interrupt Mask Bit in the condition code register masks both interrupts (See Table 1).

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Table 1 Interrupt Vector Location

Vector		Interrupt	
			MSB
Highest Priority	FFFE	FFFF	RES
	FFFC	FFFD	NMI
	FFFA	FFFB	Software Interrupt (SWI)
	FFF8	FFF9	\overline{IRQ}_1 (or IS3)
	FFF6	FFF7	ICF (Input Capture)
	FFF4	FFF5	OCF (Output Compare)
	FFF2	FFF3	TOF (Timer Overflow)
	FFF0	FFF1	SC ₁ (RDRF + ORFE + TDRE)
Lowest Priority			

The following pins are available in the Single Chip Mode, and are associated with Port 3 only.

- **Input Strobe ($\overline{IS3}$) (SC₁)**

The function of the $\overline{IS3}$ signal depends on the I/O Port 3 Control/Status Register. If $\overline{IS3}$ Enable bit is set, an interrupt will occur by the fall of the $\overline{IS3}$ signal. If the latch enable bit is set, the data in the I/O Port 3 will be latched at the I/O Port 3 Data Register. The timing condition of the $\overline{IS3}$ signal that is necessary to be latched the input data normally is shown in Figure 6.

- **Output Strobe ($\overline{OS3}$) (SC₂)**

This signal is used by the processor to strobe an external device, indicating valid data is on the I/O pins. The timing for the Output Strobe is shown in Figure 5. I/O Port 3 Control/Status Register is discussed in the following section.

The following pins are available in the Expanded Modes.

- **Read/Write (R/ \overline{W}) (SC₂)**

This TTL compatible output signals the peripherals and memory devices whether the CPU is in a Read ("High") or a Write ("Low") state. The normal standby state of this signal is Read ("High"). This output can drive one TTL load and 90 pF capacitance.

- **I/O Strobe (\overline{IOS}) (SC₁)**

In the expanded non-multiplexed mode of operation, \overline{IOS} internally decodes A₉ through A₁₅ as zero's and A₈ as a one. This allows external access of the 256 locations from \$0100 to \$01FF. The timing diagrams are shown as figure 2.

- **Address Strobe (AS) (SC₁)**

In the expanded multiplexed mode of operation, address strobe is output on this pin. This signal is used to latch the 8 LSB's of address which are multiplexed with data on Port 3. An 8-bit latch is utilized in conjunction with Address Strobe, as shown in figure 19. So I/O port 3 can become data bus during the E pulse. The timing for this signal is shown in Figure 1 of Bus Timing. This signal is also used to disable the address from the multiplexed bus allowing a deselect time, t_{ASD} before the data is enabled to the bus.

- **PORTS**

There are four I/O ports on the HD6801V MCU; three 8-bit ports and one 5-bit port. There are two control lines associated with one of the 8-bit ports. Each port has an associated write only Data Direction Register which allows each I/O line to be programmed to act as an input or an output*. A "1" in the corresponding Data Direction Register bit will cause that I/O line to be an output. A "0" in the corresponding Data Direction Register bit will cause that I/O line to be an input. There are four ports: Port 1, Port 2, Port 3, and Port 4. Their addresses and the addresses of their Data Direction registers are given in Table 2.

* The only exception is bit 1 of Port 2, which can either be data input or Timer output.

Table 2 Port and Data Direction Register Addresses

Ports	Port Address	Data Direction Register Address
I/O Port 1	\$0002	\$0000
I/O Port 2	\$0003	\$0001
I/O Port 3	\$0006	\$0004
I/O Port 4	\$0007	\$0005

- **I/O Port 1**

This is an 8-bit port whose individual bits may be defined as inputs or outputs by the corresponding bit in its data direction register. The 8 output buffers have three-state capability, allowing them to enter a high impedance state when the peripheral data lines are used as inputs. In order to be read properly, the voltage on the input lines must be greater than 2.0 V for a logic "1" and less than 0.8 V for a logic "0". As outputs these lines are TTL compatible and may also be used as a source of up to 1 mA at 1.5 V to directly drive a Darlington base. After Reset, the I/O lines are configured as inputs. In all three modes, Port 1 is always parallel I/O.

- **I/O Port 2**

This port has five lines that may be defined as inputs or outputs by its data direction register. The 5 output buffers have three-state capability, allowing them to enter a high impedance state when used as an input. In order to be read properly, the voltage on the input lines must be greater than 2.0 V for a logic "1" and less than 0.8 V for a logic "0". As outputs, this port has no internal pullup resistors but will drive TTL inputs directly. For driving CMOS inputs, external pullup resistors are required. After Reset, the I/O lines are configured as inputs. Three pins on Port 2 (pins 10, 9, and 8 of the chip) are used to program the mode of operation during reset. The values of these pins at reset are latched into the three MSB's (bits 7, 6, and 5) of Port 2 which are read only. This is explained in the Mode Selection Section.

In all three modes, Port 2 can be configured as I/O and provides access to the Serial Communications Interface and the Timer. Bit 1 is the only pin restricted to data input or Timer output.

- **I/O Port 3**

This is an 8-bit port that can be configured as I/O, a data bus, or an address bus multiplexed with the data bus - depending on the mode of operation hardware programmed by the user at reset. As a data bus, Port 3 is bi-directional. As an input for peripherals, it must be supplied regular TTL levels, that is, greater than 2.0 V for a logic "1" and less than 0.8 V for a logic "0"

Its TTL compatible three-state output buffers can drive one TTL load and 90 pF capacitance. In the Expanded Modes, after reset, the data direction register is inhibited and data flow depends on the state of the R/W line. The input strobe ($\overline{IS3}$) and the output strobe ($\overline{OS3}$) used for handshaking are explained later.

In the three modes, Port 3 assumes the following characteristics:

Single Chip Mode: Parallel Inputs/Outputs as programmed by its associated Data Direction Register. There are two control lines associated with this port in this mode, an input strobe and an output strobe, that can be used for handshaking. They are controlled by the I/O Port 3 Control/Status Register explained at the end of this section. Three options of Port 3 operations are summarized as follows: (1) Port 3 input data can be latched using $\overline{IS3}$ (SC_1) as a control signal, (2) $\overline{OS3}$ can be generated by either a CPU read or write to Port 3's Data Register, and (3) and $\overline{IRQ_1}$ interrupt can be enabled by an $\overline{IS3}$ negative edge. Port 3 latch and strobe timing is shown in Fig. 5 and Fig. 6.

Expanded Non-Multiplexed Mode: In this mode, Port 3 becomes the data bus ($D_0 \sim D_7$).

Expanded Multiplexed Mode: In this mode, Port 3 becomes both the data bus ($D_0 \sim D_7$) and lower bits of the address bus ($A_0 \sim A_7$). An address strobe output is true when the address is on the port.

I/O PORT 3 CONTROL/STATUS REGISTER

	7	6	5	4	3	2	1	0
\$000F	$\overline{IS3}$ FLAG	$\overline{IS3}$ $\overline{IRQ_1}$ ENABLE	X	OSS	LATCH ENABLE	X	X	X

Bit 0; Not used.

Bit 1; Not used.

Bit 2; Not used.

Bit 3; **LATCH ENABLE.** This controls the input latch for I/O Port 3. If this bit is set "High" the input data will be latched with the falling edge of the Input Strobe, $\overline{IS3}$. This bit is cleared by reset, and the latch is "re-opened" with CPU read Port 3.

Bit 4; **OSS.** (Output Strobe Select) This bit will select if the Output Strobe should be generated at $\overline{OS3}$ (SC_2) by a write to I/O Port 3 or a read of I/O Port 3. When this bit is cleared the strobe is generated by a read Port 3. When this bit is set the strobe is generated by a write to Port 3.

Bit 5; Not used.

Bit 6; **$\overline{IS3}$ $\overline{IRQ_1}$ ENABLE.** When set, interrupt will be enabled whenever $\overline{IS3}$ FLAG is set; when clear, interrupt is inhibited. This bit is cleared by reset.

Bit 7; **$\overline{IS3}$ FLAG.** This is a read-only status bit that is set by the falling edge of the input strobe, $\overline{IS3}$ (SC_1). It is cleared by a read of the Control/Status Register followed by a read or write of I/O Port 3. Reset will clear this bit.

• **I/O Port 4**

This is an 8-bit port that can be configured as I/O or as address output lines depending on the mode of operation. In order to be read properly, the voltage on the input lines must be greater than 2.0 V for a logic "1" and less than 0.8 V for a logic "0".

As outputs, each line is TTL compatible and can drive 1 TTL load and 90 pF capacitance. After reset, the lines are configured as inputs. To use the pins as addresses, therefore, they should be programmed as outputs. In the three modes, Port 4 assumes the following characteristics:

Single Chip Mode: Parallel Inputs/Outputs as programmed by its associated Data Direction Register.

Expanded Non-Multiplexed Mode: Port 4 is configured as the lower order address lines ($A_0 \sim A_7$) by writing "1"s to the data direction register. When all eight address lines are not needed, the remaining lines, starting with the most significant bit, may be used as I/O (inputs only).

Expanded Multiplexed Mode: Port 4 is configured as the higher order address lines ($A_8 \sim A_{15}$) by writing "1"s to the data direction register. When all eight address lines are not needed, the remaining lines, starting with the most significant bit, may be used as I/O (inputs only).

■ **OPERATION MODES**

The operation modes that HD6801V will operate after Reset is determined by hardware that the user must wire on pins 10, 9, and 8 of the chip. These pins are the three LSB's (I/O 2, I/O 1, and I/O 0 respectively) of Port 2. They are latched into programmed control bits PC2, PC1, and PC0 when reset goes high. I/O Port 2 Register is shown below.

PORT 2 DATA REGISTER

	7	6	5	4	3	2	1	0
\$0003	PC2	PC1	PC0	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0

An example of external hardware that could be used for Mode Selection is shown in Fig 14. The HD14053B provides the isolation between the peripheral device and MCU during reset, which is necessary if data conflict can occur between peripheral device and Mode generation circuit.

As bits 5, 6 and 7 of Port 2 are read-only, the mode cannot be changed through software. The mode selections are shown in Table 3.

The HD6801V can operate three basic modes; (1) Single Chip Mode. (2) Expanded Multiplexed Mode (compatible with HMCS6800 peripheral family) (3) Expanded Non-Multiplexed Mode.

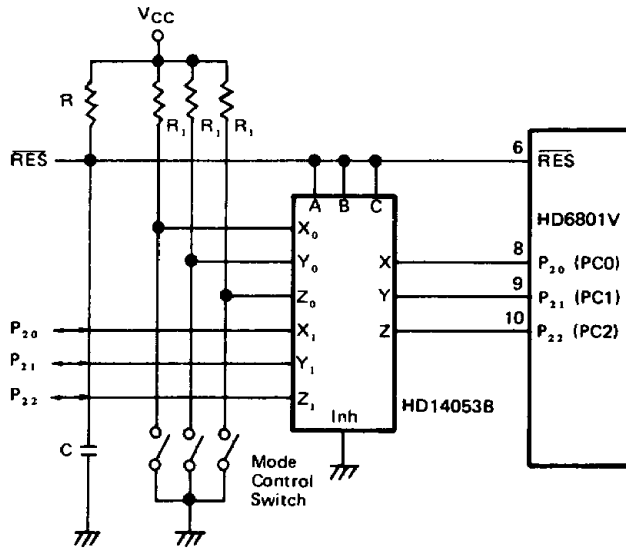
• **Single Chip Mode**

In the Single Chip Mode the Ports are configured as I/O. This is shown in Figure 16 the single Chip Mode. In this mode, Port 3 will have two associated control lines, an input strobe and an output strobe for handshaking data.

• **Expanded Non-Multiplexed Mode**

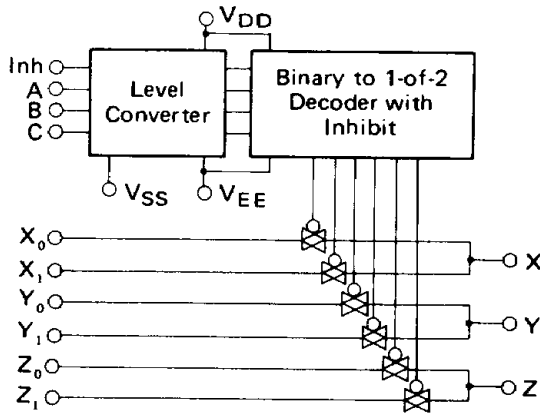
In this mode the HD6801V will directly address HMCS6800 peripherals with no external logic. In this mode Port 3 becomes the data bus. Port 4 becomes the $A_0 \sim A_7$ address bus or partial address and I/O (inputs only). Port 2 can be parallel I/O, serial I/O, Timer, or any combination of them. Port 1 is parallel I/O only. In this mode the HD6801V is expandable to 256 locations. The eight address lines associated with Port 4 may be substituted for I/O (inputs only) if a fewer number of address lines will satisfy the application (See Figure 17).

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- (NOTES) 1) Mode 7 as shown
 2) $RC \approx$ Reset time constant
 3) $R_1 = 10k\Omega$

Figure 14 Recommended Circuit for Mode Selection



Truth Table

Control Input			On Switch		
Inhibit	Select			HD14053B	
	C	B	A	Z	X
0	0	0	0	Z ₀	X ₀
0	0	0	1	Z ₀	X ₁
0	0	1	0	Z ₁	X ₀
0	0	1	1	Z ₁	X ₁
0	1	0	0	Z ₁	X ₀
0	1	0	1	Z ₁	X ₁
0	1	1	0	Z ₁	X ₀
0	1	1	1	Z ₁	X ₁
1	X	X	X	-	-

Figure 15 HD14053B Multiplexers/Demultiplexers

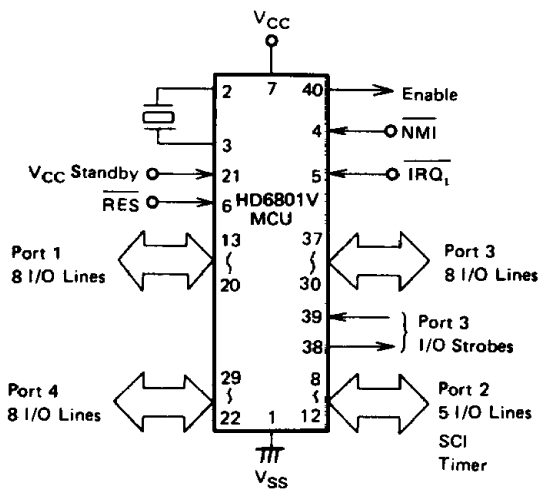


Figure 16 HD6801V MCU Single-Chip Mode

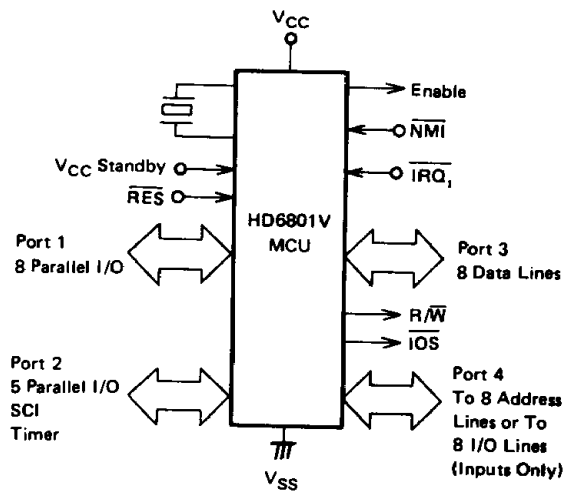


Figure 17 HD6801V MCU Expanded Non-Multiplexed Mode



Table 3 Mode Selection Summary

Mode	P ₂₂ (PC2)	P ₂₃ (PC1)	P ₃₀ (PC0)	ROM	RAM	Interrupt Vectors	Bus Mode	Operating Mode
7	H	H	H	I	I	I	I	Single Chip
6	H	H	L	I	I	I	MUX ⁽⁶⁾	Multiplexed/Partial Decode
5	H	L	H	I	I	I	NMUX ⁽⁶⁾	Non-Multiplexed/Partial Decode
4	H	L	L	I ⁽²⁾	I ⁽¹⁾	I	I	Single Chip Test
3	L	H	H	E	E	E	MUX	Multiplexed/No RAM & ROM
2	L	H	L	E	I	E	MUX	Multiplexed/RAM
1	L	L	H	I	I	E	MUX	Multiplexed/RAM & ROM
0	L	L	L	I	I	I ⁽³⁾	MUX	Multiplexed Test

LEGEND:

I – Internal
 E – External
 MUX – Multiplexed
 NMUX – Non-Multiplexed
 L – Logic "0"
 H – Logic "1"

[NOTES]

- 1) Internal RAM is addressed at \$XX80
- 2) Internal ROM is disabled
- 3) \overline{RES} vector is external for 2 cycles after \overline{RES} goes "High"
- 4) Addresses associated with Ports 3 and 4 are considered external in Modes 0, 1, 2, and 3
- 5) Addresses associated with Port 3 are considered external in Modes 5 and 6
- 6) Port 4 default is user data input; address output is optional by writing to Port 4 Data Direction Register

■ **MEMORY MAPS**

The MCU can provide up to 65k bytes address space depending on the operating mode. A memory map for each operating mode is shown in Figure 20. The first 32 locations of each map are reserved for the MCU's internal register area, as shown in Table 4. With exceptions as indicated.

■ **INTERRUPT FLOWCHART**

The Interrupt flowchart is depicted in Figure 24 and is common to every interrupt excluding reset.

Table 4 Internal Register Area

Register	Address
Port 1 Data Direction Register***	00
Port 2 Data Direction Register***	01
Port 1 Data Register	02
Port 2 Data Register	03
Port 3 Data Direction Register***	04*
Port 4 Data Direction Register***	05**
Port 3 Data Register	06*
Port 4 Data Register	07**
Timer Control and Status Register	08
Counter (High Byte)	09
Counter (Low Byte)	0A
Output Compare Register (High Byte)	0B
Output Compare Register (Low Byte)	0C
Input Capture Register (High Byte)	0D
Input Capture Register (Low Byte)	0E
Port 3 Control and Status Register	0F*
Rate and Mode Control Register	10
Transmit/Receive Control and Status Register	11
Receive Data Register	12
Transmit Data Register	13
RAM Control Register	14
Reserved	15-1F

* External address in Modes 0, 1, 2, 3, 5, 6; cannot be accessed in Mode 5 (No. IOS)

** External addresses in Modes 0, 1, 2, 3

*** 1=Output, 0=Input.

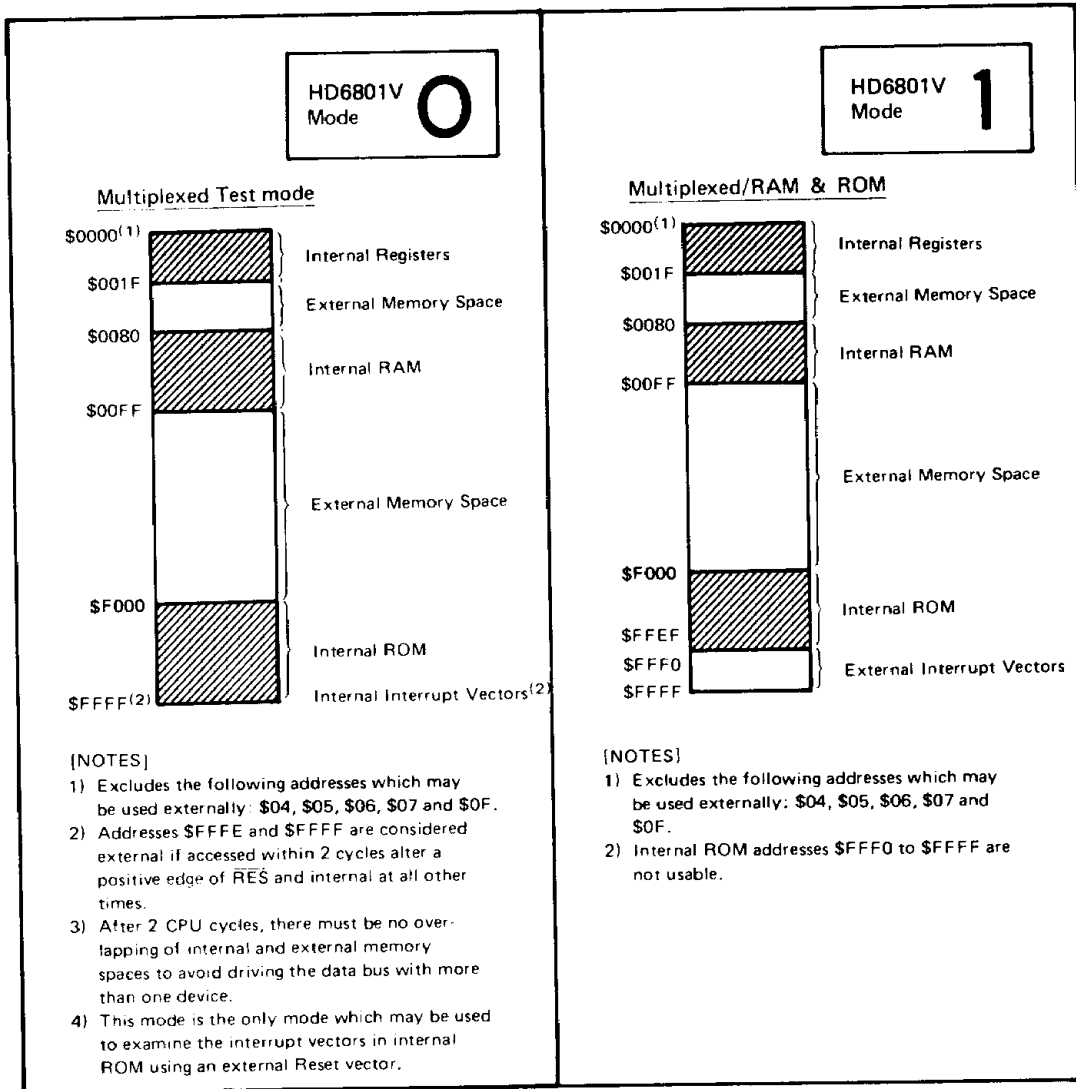


Figure 20 HD6801V Memory Maps

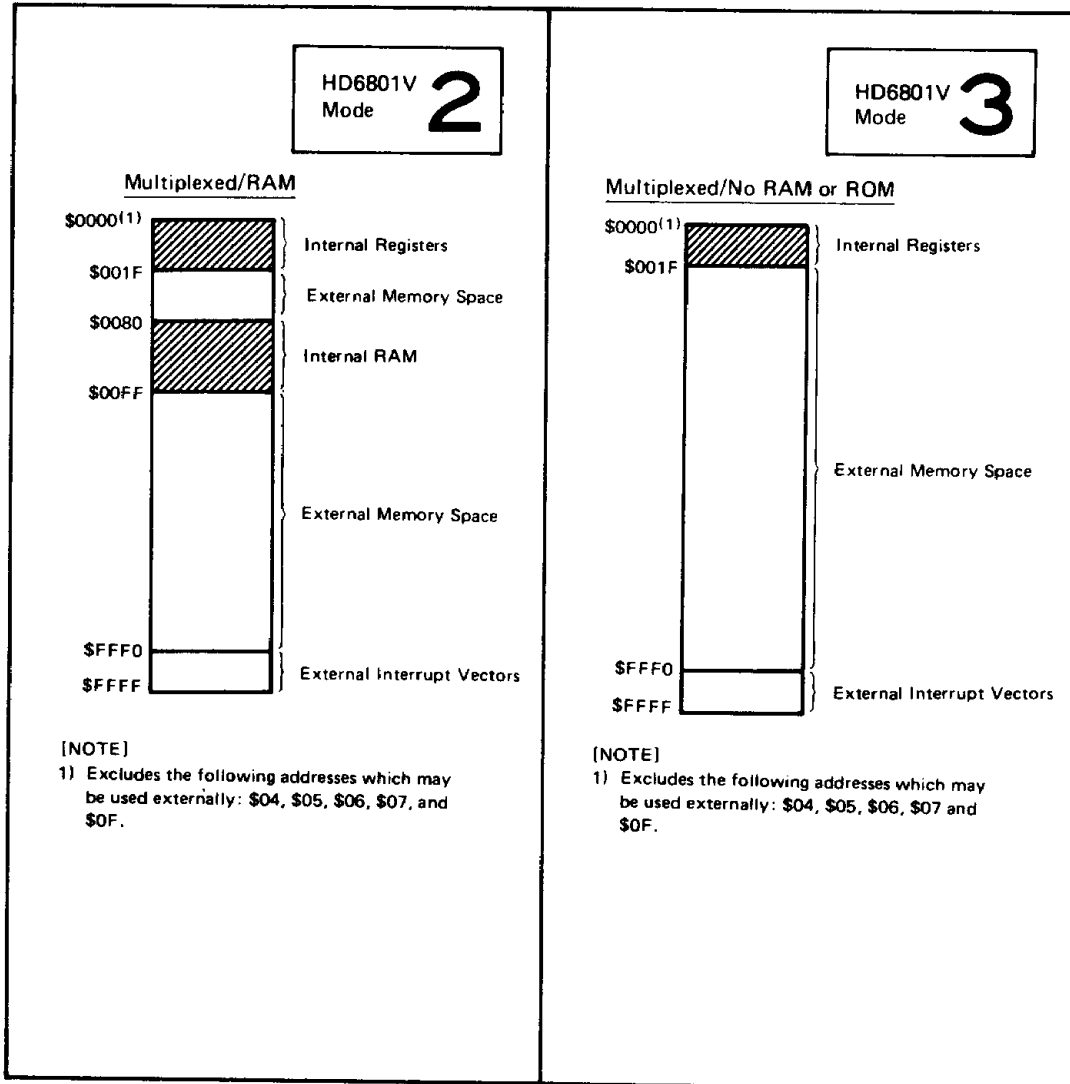


Figure 20 HD6801V Memory Maps (Continued)

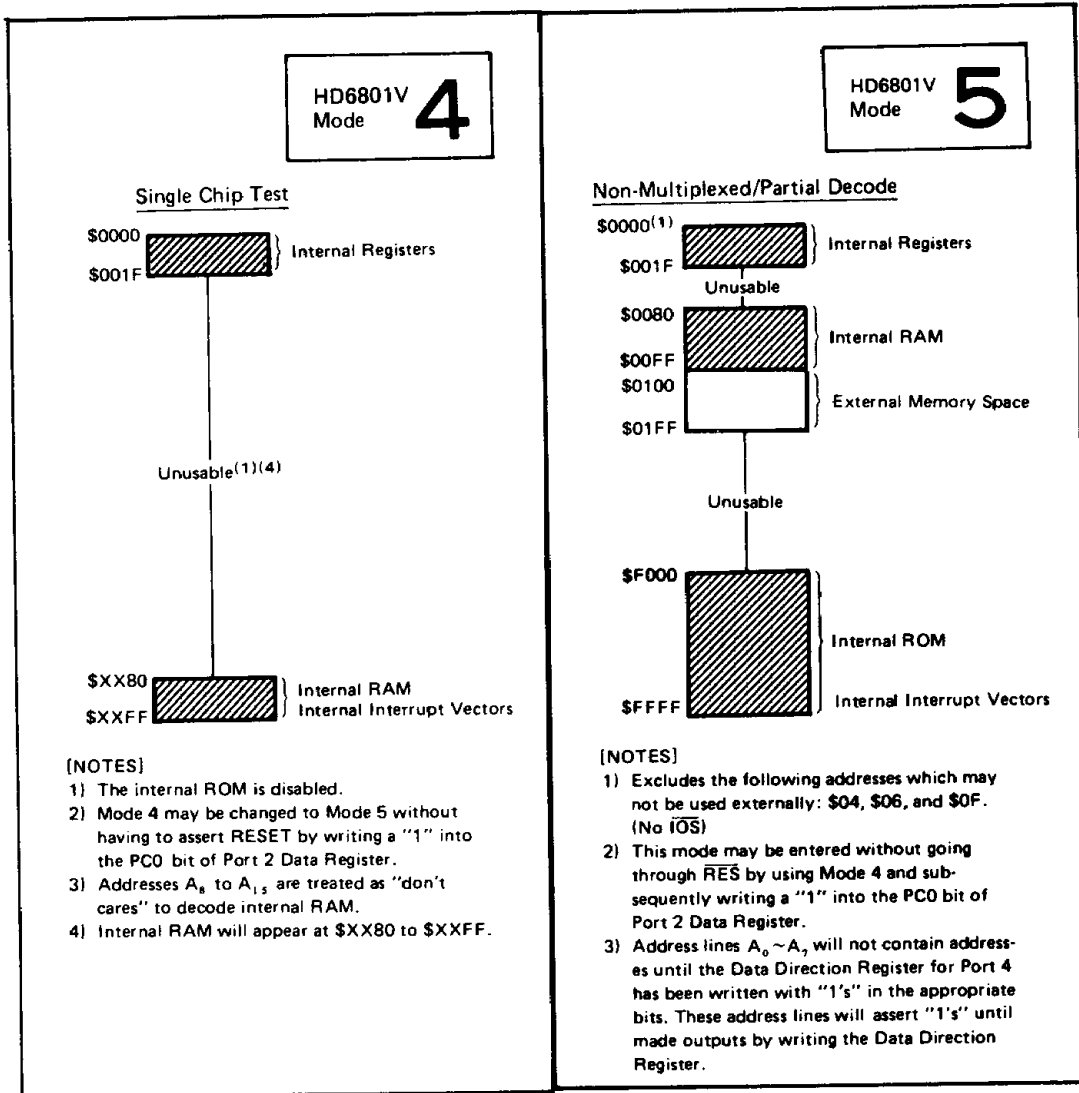


Figure 20 HD6801V Memory Maps (Continued)

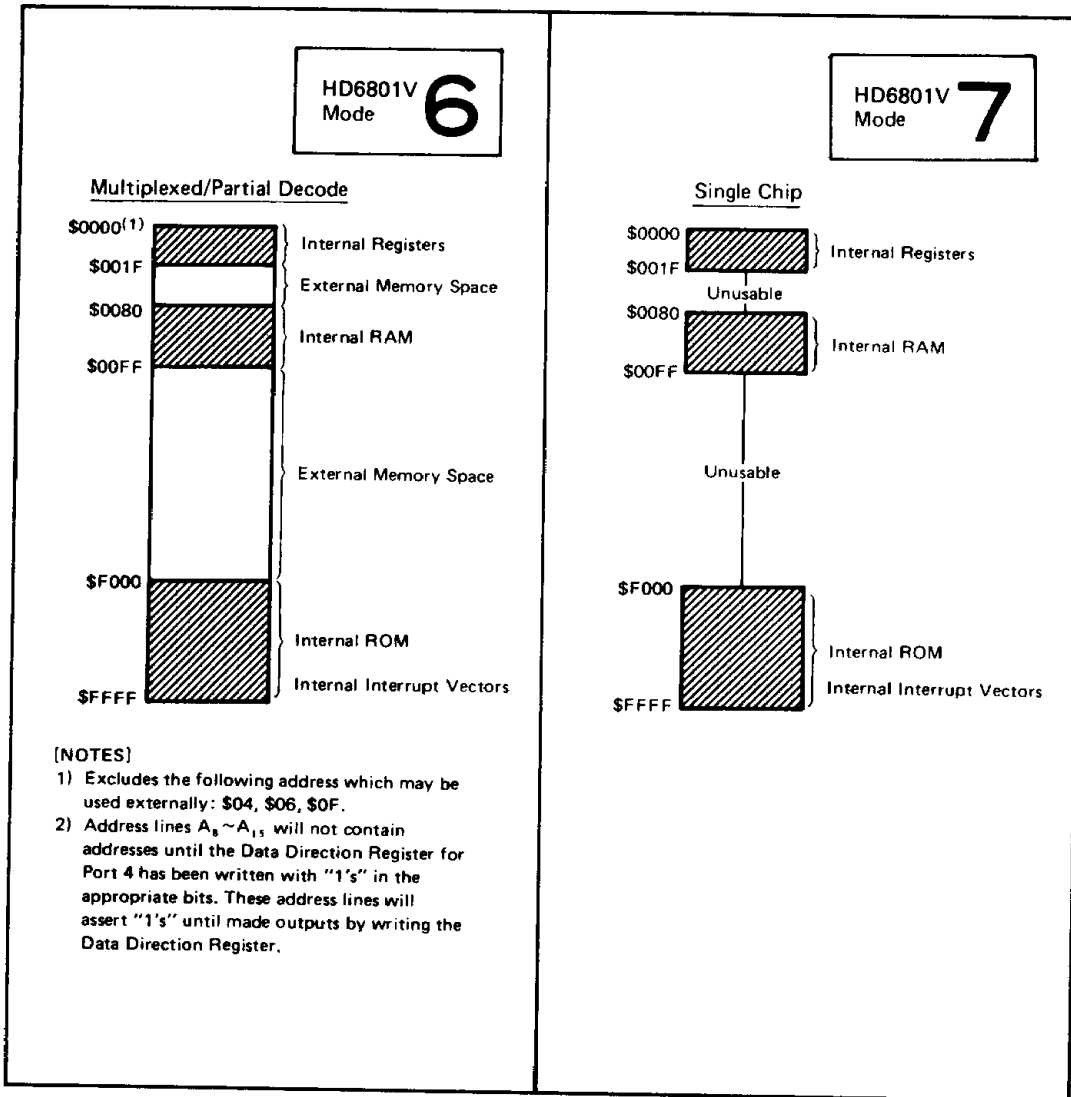


Figure 20 HD6801V Memory Maps (Continued)

■ PROGRAMMABLE TIMER

The HD6801V contains an on-chip 16-bit programmable timer which may be used to perform measurements on an input waveform while independently generating an output waveform. Pulse widths for both input and output signals may vary from a few microseconds to many seconds. The timer hardware consists of

- an 8-bit control and status register,
- a 16-bit free running counter,
- a 16-bit output compare register, and
- a 16-bit input capture register

A block diagram of the timer registers is shown in Figure 21.

● Free Running Counter (\$0009:\$000A)

The key element in the programmable timer is a 16-bit free running counter which is driven to increasing values by E (Enable). The counter value may be read by the CPU software at any time. The counter is cleared to zero by reset and may be considered a read-only register with one exception. Any CPU write to the counter's address (\$09) will always result in preset value of \$FFF8 being loaded into the counter regardless of the value involved in the write. This preset figure is intended for testing operation of the part, but may be of value in some applications.

● Output Compare Register (\$000B:\$000C)

The Output Compare Register is a 16-bit read/write register which is used to control an output waveform. The contents of this register are constantly compared with the current value of the free running counter. When a match is found, a flag is set (OCF) in the Timer Control and Status Register (TCSR) and the current value of the Output Level bit (OLVL) in the TCSR is clocked to the Output Level Register. Providing the Data Direction Register for Port 2, Bit 1 contains a "1" (Output), the output level register value will appear on the pin for Port 2

Bit 1. The values in the Output Compare Register and Output level bit may then be changed to control the output level on the next compare value. The Output Compare Register is set to \$FFFF during reset. The Compare function is inhibited for one cycle following a write to the high byte of the Output Compare Register to insure a valid 16-bit value is in the register before a compare is made.

● Input Capture Register (\$000D:\$000E)

The Input Capture Register is a 16-bit read-only register used to store the current value of the free running counter when the proper transition of an external input signal occurs. The input transition change required to trigger the counter transfer is controlled by the input Edge bit (IEDG) in the TCSR. The Data Direction Register bit for Port 2 Bit 0, should* be clear (zero) in order to gate in the external input signal to the edge detect unit in the timer.

The input pulse width must be at least two E-cycles to ensure an input capture under all conditions.

* With Port 2 Bit 0 configured as an output and set to "1", the external input will still be seen by the edge detect unit.

● Timer Control and Status Register (TCSR) (\$0008)

The Timer Control and Status Register consists of an 8-bit register of which all 8 bits are readable but only the low order 5 bits may be written. The upper three bits contain read-only timer status information and indicate the followings:

- a proper transition has taken place on the input pin with a subsequent transfer of the current counter value to the input capture register.
- a match has been found between the value in the free running counter and the output compare register, and
- when \$0000 is in the free running counter.

Each of the flags may be enabled onto the HD6801V internal bus (IRQ₂) with an individual Enable bit in the TCSR. If the

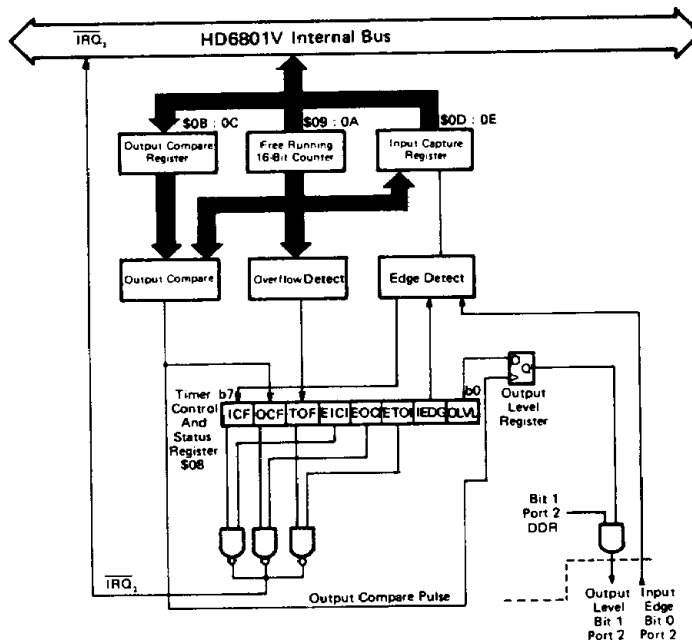
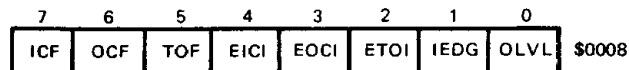


Figure 21 Block Diagram of Programmable Timer

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Timer Control and Status Register



1-bit in the HD6801V Condition Code Register has been cleared, a priority vectored interrupt will occur corresponding to the flag bit(s) set. A description for each bit follows:

- Bit 0 OLVL** Output Level – This value is clocked to the output level register on a successful output compare. If the DDR for Port 2 bit 1 is set, the value will appear on the output pin.
- Bit 1 IEDG** Input Edge – This bit controls which transition of an input will trigger a transfer of the counter to the input capture register. The DDR for Port 2 Bit 0 must be clear for this function to operate. IEDG = 0 Transfer takes place on a negative edge (“High”-to-“Low” transition). IEDG = 1 Transfer takes place on a positive edge (“Low”-to-“High” transition).
- Bit 2 ETOI** Enable Timer Overflow Interrupt – When set, this bit enables \overline{IRQ}_2 to occur on the internal bus for a TOF interrupt; when clear the interrupt is inhibited.
- Bit 3 EOCI** Enable Output Compare Interrupt – When set, this bit enables \overline{IRQ}_2 to appear on the internal bus for an output compare interrupt; when clear the interrupt is inhibited.
- Bit 4 EICI** Enable Input Capture Interrupt – When set, this bit enables \overline{IRQ}_2 to occur on the internal bus for an input capture interrupt; when clear the interrupt is inhibited.
- Bit 5 TOF** Timer Overflow Flag – This read-only bit is set when the counter contains \$FFFF. It is cleared by a read of the TCSR (with TOF set) followed by an CPU read of the Counter (\$09).
- Bit 6 OCF** Output Compare Flag – This read-only bit is set when a match is found between the output compare register and the free running counter. It is cleared by a read of the TCSR (with OCF set) followed by an CPU write to the output compare register (\$0B or \$0C).
- Bit 7 ICF** Input Capture Flag – This read-only status bit is set by a proper transition on the input; it is cleared by a read of the TCSR (with ICF set) followed by an CPU read of the Input Capture Register (\$0D).

■ SERIAL COMMUNICATION INTERFACE

The HD6801V contains a full-duplex asynchronous serial communication interface (SCI) on chip. The controller comprises a transmitter and a receiver which operate independently or each other but in the same data format and at the same data rate. Both transmitter and receiver communicate with the

CPU via the data bus and with the outside world via pins 2, 3, and 4 of Port 2. The hardware, software, and registers are explained in the following paragraphs.

• Wake-Up Feature

In a typical multi-processor application, the software protocol will usually contain a destination address in the initial byte(s) of the message. In order to permit non-selected MCU's to ignore the remainder of the message, a wake-up feature is included whereby all further interrupt processing may be optionally inhibited until the beginning of the next message. When the next message appears, the hardware re-enables (or “wakes-up”) for the next message. The “wake-up” is automatically triggered by a string of ten consecutive 1's which indicates an idle transmit line. The software protocol must provide for the short idle period between any two consecutive messages.

• Programmable Options

The following features of the HD6801V serial I/O section are programmable:

- format – standard mark/space (NRZ)
- Clock – external or internal
- baud rate – one of 4 per given CPU ϕ_2 clock frequency or external clock $\times 8$ input
- wake-up feature – enabled or disabled
- Interrupt requests – enabled or masked individually for transmitter and receiver data registers
- clock output – internal clock enabled or disabled to Port 2 (Bit 2)
- Port 2 (bits 3 and 4) – dedicated or not dedicated to serial I/O individually for transmitter and receiver.

• Serial Communication Hardware

The serial communication hardware is controlled by 4 registers as shown in Figure 22. The registers include:

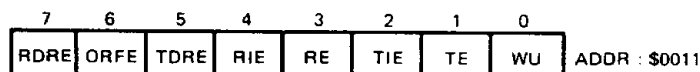
- an 8-bit control and status register
- a 4-bit rate and mode control register (write only)
- an 8-bit read only receive data register and
- an 8-bit write only transmit data register.

In addition to the four registers, the serial I/O section utilizes bit 3 (serial input) and bit 4 (serial output) of Port 2. Bit 2 of Port 2 is utilized if the internal-clock-out or external-clock-in options are selected.

Transmit/Receive Control and Status (TRCS) Register

The TRCS register consists of an 8-bit register of which all 8 bits may be read while only bits 0~4 may be written. The register is initialized to \$20 by reset. The bits in the TRCS register are defined as follows:

Transmit/Receive Control and Status Register



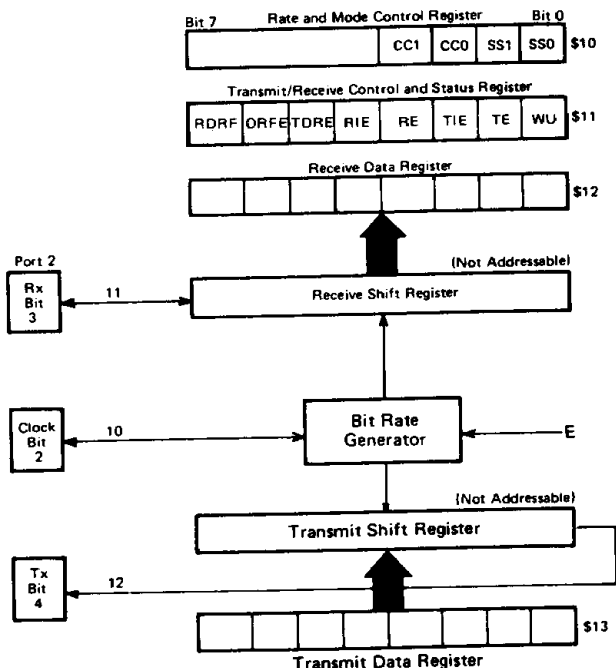


Figure 22 Serial I/O Registers

- Bit 0 WU** "Wake-up" on Next Message – set by HD6801V software and cleared by hardware on receipt of ten consecutive 1's or reset of RE flag. It should be noted that RE flag should be set in advance of CPU set of WU flag.
- Bit 1 TE** Transmit Enable – set by HD6801V to produce preamble of nine consecutive 1's and to enable gating of transmitter output to Port 2, bit 4 regardless of the DDR value corresponding to this bit; when clear, serial I/O has no effect on Port 2 bit 4.
TE should be after at least one bit time of data transmit rate from the set-up of transmit data rate and mode.
- Bit 2 TIE** Transmit Interrupt Enable – when set, will permit an \overline{IRQ}_2 interrupt to occur when bit 5 (TDRE) is set; when clear, the TDRE value is masked from the bus.
- Bit 3 RE** Receiver Enable – when set, gates Port 2 bit 3 to input of receiver regardless of DDR value for this bit; when clear, serial I/O has no effect on Port 2 bit 3.
- Bit 4 RIE** Receiver Interrupt Enable – when set, will permit an \overline{IRQ}_2 interrupt to occur when bit 7 (RDRF) or bit 6 (ORFE) is set; when clear, the interrupt is masked.
- Bit 5 TDRE** Transmit Data Register Empty – set by hardware when a transfer is made from the transmit data register to the output shift register. The TDRE bit is cleared by reading the status register, then writing a new byte into the transmit data register,

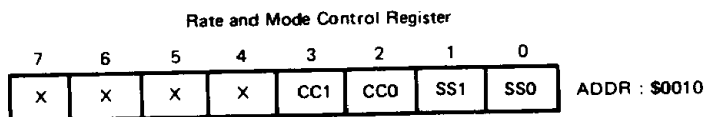
- Bit 6 ORFE** Over-Run-Framing Error – set by hardware when an overrun or framing error occurs (receive only). An overrun is defined as a new byte received with last byte still in Data Register/Buffer. A framing error has occurred when the byte boundaries in bit stream are not synchronized to bit counter. If WU flag is set, the ORFE bit will not be set. The ORFE bit is cleared by reading the status register, then reading the Receive Data Register, or by reset.
- Bit 7 RDRF** Receiver Data Register Full – set by hardware when a transfer from the input shift register to the receiver data register is made. If WU flag is set, the RDRF bit will not be set. The RDRF bit is cleared by reading the status register, then reading the Receive Data Register, or by reset.

Rate and Mode Control Register

The Rate and Mode Control register controls the following serial I/O variables:

- Baud rate
- format
- clocking source, and
- Port 2 bit 2 configuration

The register consists of 4 bits all of which are write-only and cleared by reset. The 4 bits in the register may be considered as a pair of 2-bit fields. The two low order bits control the bit rate for internal clocking and the remaining two bits control the format and clock select logic. The register definition is as follows:



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Bit 0 **SS0** } Speed Select – These bits select the Baud rate for
 Bit 1 **SS1** } the internal clock. The four rates which may be
 selected are a function of the CPU ϕ_2 clock
 frequency. Table 5 lists the available Baud rates.

Bit 2 **CC0** } Clock Control and Format Select – this 2-bit field
 Bit 3 **CC1** } controls the format and clock select logic. Table 6
 defines the bit field.

Table 5 SCI Bit Times and Rates

SS1 : SS0	XTAL	2.4576 MHz	4.0 MHz	4.9152 MHz*
	E	614.4 kHz	1.0 MHz	1.2288 MHz
0 0	$E \div 16$	26 μ s/38,400 Baud	16 μ s/62,500 Baud	13 μ s/76,800 Baud
0 1	$E \div 128$	208 μ s/4,800 Baud	128 μ s/7812.5 Baud	104.2 μ s/9,600 Baud
1 0	$E \div 1024$	1.67 ms/600 Baud	1.024 ms/976.6 Baud	833.3 μ s/1,200 Baud
1 1	$E \div 4096$	6.67 ms/150 Baud	4.096 ms/244.1 Baud	3.33 ms/300 Baud

*HD6801V5 Only

Table 6 SCI Format and Clock Source Control

CC1: CC0	Format	Clock Source	Port 2 Bit 2	Port 2 Bit 3	Port 2 Bit 4
0 0	–	–	–	–	–
0 1	NRZ	Internal	Not Used	**	**
1 0	NRZ	Internal	Output*	**	**
1 1	NRZ	External	Input	**	**

* Clock output is available regardless of values for bits RE and TE.

** Bit 3 is used for serial input if RE = "1" in TRCS; bit 4 is used for serial output if TE = "1" in TRCS.

Internally Generated Clock

If the user wishes for the serial I/O to furnish a clock, the following requirements are applicable:

- the values of RE and TE are immaterial.
- CC1, CC0 must be set to 10
- the maximum clock rate will be $E \div 16$.
- the clock will be at $1 \times$ the bit rate and will have a rising edge at mid-bit.

Externally Generated Clock

If the user wishes to provide an external clock for the serial I/O, the following requirements are applicable:

- the CC1, CC0, field in the Rate and Mode Control Register must be set to 11,
- the external clock must be set to 8 times ($\times 8$) the desired baud rate and
- the maximum external clock frequency is 1.0 MHz.

Serial Operations

The serial I/O hardware should be initialized by the HD6801V software prior to operation. This sequence will normally consist of;

- writing the desired operation control bits to the Rate and Mode Control Register and
- writing the desired operational control bits in the Transmit/Receive Control and Status Register.

The Transmitter Enable (TE) and Receiver Enable (RE) bits may be left set for dedicated operations.

Transmit Operations

The transmit operation is enabled by the TE bit in the Transmit/Receive Control and Status Register. This bit when set, gates the output of the serial transmit shift register to Port 2 Bit 4 and takes unconditional control over the Data Direction Register value for Port 2, Bit 4.

Following a RES the user should configure both the Rate and Mode Control Register and the Transmit/Receive Control and Status Register for desired operation. Setting the TE bit during this procedure initiates the serial output by first transmitting a nine-bit preamble of 1's. Following the preamble, internal synchronization is established and the transmitter section is ready for operation.

At this point one of two situation exist:

- 1) if the Transmit Data Register is empty (TDRE = 1), a continuous string of ones will be sent indicating an idle line, or,
- 2) if data has been loaded into the Transmit Data Register (TDRE = 0), the word is transferred to the output shift register and transmission of the data word will begin.

During the data transmit, the 0 start bit is first transmitted. Then the 8 data bits (beginning with bit 0) followed by the stop bit, are transmitted. When the Transmitter Data Register has been emptied, the hardware sets the TDRE flag bit.

If the HD6801V fails to respond to the flag within the proper time, (TDRE is still set when the next normal transfer from the parallel data register to the serial output register should occur) then a 1 will be sent (instead of a 0) at "Start" bit time, followed by more 1's until more data is supplied to the data register. No 0's will be sent while TDRE remains a 1.



Receive Operation

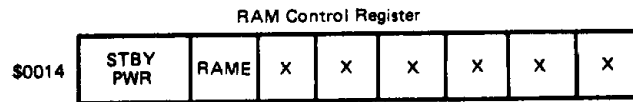
The receive operation is enabled by the RE bit which gates in the serial input through Port 2 Bit 3. The receiver section operation is conditioned by the contents of the Transmit/Receive Control and Status Register and the Rate and Mode Control Register.

The receiver bit interval is divided into 8 sub-intervals for internal synchronization. In the NRZ Mode, the received bit stream is synchronized by the first 0 (space) encountered.

The approximate center of each bit time is strobed during the next 10 bits. If the tenth bit is not a 1 (stop bit) a framing error is assumed, and bit ORFE is set. If the tenth bit as a 1, the data is transferred to the Receive Data Register, and interrupt flag RDRF is set. If RDRF is still set at the next tenth bit time, ORFE will be set, indicating an over-run has occurred. When the HD6801V responds to either flag (RDRF or ORFE) by reading the status register followed by reading the Data Register, RDRF (or ORFE) will be cleared.

RAM CONTROL REGISTER

This register, which is addressed at \$0014, gives status information about the standby RAM. A 0 in the RAM enable bit (RAME) will disable the standby RAM, thereby protecting it at power down if V_{CC} Standby is held greater than V_{SBB} volts, as explained previously in the signal description for V_{CC} Standby.



- Bit 0 Not used.
- Bit 1 Not used.
- Bit 2 Not used.
- Bit 3 Not used.
- Bit 4 Not used.
- Bit 5 Not used.

Bit 6 RAME The RAM Enable control bit allows the user the ability to disable the standby RAM. This bit is set to a logic "1" by RES which enables the standby RAM and can be written to one or zero under program control. When the RAM is disabled, data is read from external memory.

Bit 7 STBY PWR The Standby Power bit is cleared when the standby voltage is removed. This bit is a read/write status flag that the user can read which indicates that the standby RAM voltage has been applied, and the data in the standby RAM is valid.

GENERAL DESCRIPTION OF INSTRUCTION SET

The HD6801V is upward object code compatible with the HD6800 as it implements the full HMCS6800 instruction set. The execution times of key instructions have been reduced to increase throughout. In addition, new instructions have been added; these include 16-bit operations and a hardware multiply.

Included in the instruction set section are the following:

- CPU Programming Model (Figure 23)
- Addressing modes
- Accumulator and memory instructions – Table 7
- New instructions
- Index register and stack manipulations instructions – Table 8
- Jump and branch instructions – Table 9

- Condition code register manipulation instructions – Table 10
- Instructions Execution times in machine cycles – Table 11
- Summary of cycle by cycle operation – Table 12
- Summary of undefined instructions operation
- Op codes Map – Table 13

CPU Programming Model

The programming model for the HD6801V is shown in Figure 23. The double (D) accumulator is physically the same as the Accumulator A concatenated with the Accumulator B so that any operation using accumulator D will destroy information in A and B.

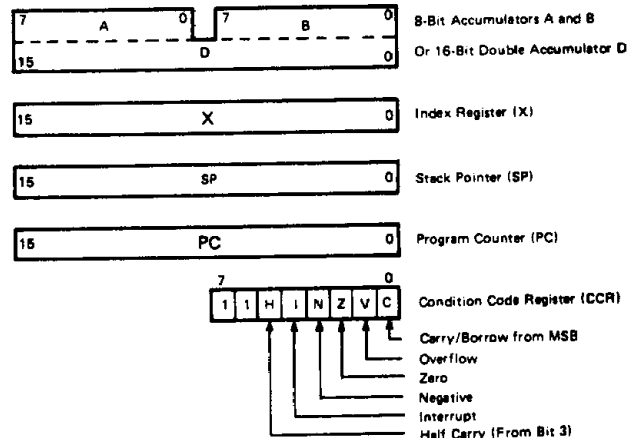


Figure 23 CPU Programming Model

CPU Addressing Modes

The HD6801V eight-bit microcomputer unit has seven address modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Table 11 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 4 MHz, these times would be microseconds.

Accumulator (ACCX) Addressing

In accumulator only addressing, either accumulator A or accumulator B is specified. These are one-byte instructions.

Immediate Addressing

In immediate addressing, the operand is contained in the second byte of the instruction except LDS and LDX which have the operand in the second and third bytes of the instruction. The CPU addresses this location when it fetches the immediate instruction for execution. These are two or three-byte instructions.

Table 7 Accumulator & Memory Instructions

Operations	Mnemonic	Addressing Modes												Boolean/ Arithmetic Operation	Condition Code Register								
		IMMED.			DIRECT			INDEX			EXTEND				IMPLIED			5	4	3	2	1	0
		OP	~	#	OP	~	#	OP	~	#	OP	~	#		OP	~	#	H	I	N	Z	V	C
Add	ADDA	8B	2	2	9B	3	2	AB	4	2	BB	4	3			$A + M \rightarrow A$	†	•	†	†	†	†	
	ADDB	CB	2	2	DB	3	2	EB	4	2	FB	4	3			$B + M \rightarrow B$	†	•	†	†	†	†	
Add Double	ADDD	C3	4	3	D3	5	2	E3	6	2	F3	6	3			$A : B + M : M + 1 \rightarrow A : B$	•	•	†	†	†	†	
Add Accumulators	ABA													1B	2	1	$A + B \rightarrow A$	†	•	†	†	†	†
Add With Carry	ADCA	89	2	2	99	3	2	A9	4	2	B9	4	3			$A + M + C \rightarrow A$	†	•	†	†	†	†	
	ADCB	C9	2	2	D9	3	2	E9	4	2	F9	4	3			$B + M + C \rightarrow B$	†	•	†	†	†	†	
AND	ANDA	84	2	2	94	3	2	A4	4	2	B4	4	3			$A \cdot M \rightarrow A$	•	•	†	†	R	•	
	ANDB	C4	2	2	D4	3	2	E4	4	2	F4	4	3			$B \cdot M \rightarrow B$	•	•	†	†	R	•	
Bit Test	BIT A	85	2	2	95	3	2	A5	4	2	B5	4	3			$A \cdot M$	•	•	†	†	R	•	
	BIT B	C5	2	2	D5	3	2	E5	4	2	F5	4	3			$B \cdot M$	•	•	†	†	R	•	
Clear	CLR							6F	6	2	7F	6	3			$00 \rightarrow M$	•	•	R	S	R	R	
	CLRA													4F	2	1	$00 \rightarrow A$	•	•	R	S	R	R
	CLRB													5F	2	1	$00 \rightarrow B$	•	•	R	S	R	R
Compare	CMPA	81	2	2	91	3	2	A1	4	2	B1	4	3			$A - M$	•	•	†	†	†	†	
	CMPB	C1	2	2	D1	3	2	E1	4	2	F1	4	3			$B - M$	•	•	†	†	†	†	
Compare Accumulators	CBA													11	2	1	$A - B$	•	•	†	†	†	†
Complement, 1's	COM							63	6	2	73	6	3			$\bar{M} \rightarrow M$	•	•	†	†	R	S	
	COMA													43	2	1	$\bar{A} \rightarrow A$	•	•	†	†	R	S
	COMB													53	2	1	$\bar{B} \rightarrow B$	•	•	†	†	R	S
Complement, 2's (Negate)	NEG							60	6	2	70	6	3			$00 - M \rightarrow M$	•	•	†	†	①	②	
	NEGA													40	2	1	$00 - A \rightarrow A$	•	•	†	†	①	②
	NEGB													50	2	1	$00 - B \rightarrow B$	•	•	†	†	①	②
Decimal Adjust, A	DAA													19	2	1	Converts binary add of BCD characters into BCD format	•	•	†	†	†	③
Decrement	DEC							6A	6	2	7A	6	3			$M - 1 \rightarrow M$	•	•	†	†	④	•	
	DECA													4A	2	1	$A - 1 \rightarrow A$	•	•	†	†	④	•
	DECB													5A	2	1	$B - 1 \rightarrow B$	•	•	†	†	④	•
Exclusive OR	EORA	88	2	2	98	3	2	A8	4	2	B8	4	3			$A \oplus M \rightarrow A$	•	•	†	†	R	•	
	EORB	C8	2	2	D8	3	2	E8	4	2	F8	4	3			$B \oplus M \rightarrow B$	•	•	†	†	R	•	
Increment	INC							6C	6	2	7C	6	3			$M + 1 \rightarrow M$	•	•	†	†	⑤	•	
	INCA													4C	2	1	$A + 1 \rightarrow A$	•	•	†	†	⑤	•
	INCB													5C	2	1	$B + 1 \rightarrow B$	•	•	†	†	⑤	•
Load Accumulator	LDAA	86	2	2	96	3	2	A6	4	2	B6	4	3			$M \rightarrow A$	•	•	†	†	R	•	
	LDAB	C6	2	2	D6	3	2	E6	4	2	F6	4	3			$M \rightarrow B$	•	•	†	†	R	•	
Load Double Accumulator	LDD	CC	3	3	DC	4	2	EC	5	2	FC	5	3			$M + 1 \rightarrow B, M \rightarrow A$	•	•	†	†	R	•	
Multiply Unsigned	MUL													3D	10	1	$A \times B \rightarrow A : B$	•	•	•	•	•	⑩
OR, Inclusive	ORAA	8A	2	2	9A	3	2	AA	4	2	BA	4	3			$A + M \rightarrow A$	•	•	†	†	R	•	
	ORAB	CA	2	2	DA	3	2	EA	4	2	FA	4	3			$B + M \rightarrow B$	•	•	†	†	R	•	
Push Data	PSHA													36	3	1	$A \rightarrow Msp, SP - 1 \rightarrow SP$	•	•	•	•	•	•
	PSHB													37	3	1	$B \rightarrow Msp, SP - 1 \rightarrow SP$	•	•	•	•	•	•
Pull Data	PULA													32	4	1	$SP + 1 \rightarrow SP, Msp \rightarrow A$	•	•	•	•	•	•
	PULB													33	4	1	$SP + 1 \rightarrow SP, Msp \rightarrow B$	•	•	•	•	•	•
Rotate Left	ROL							69	6	2	79	6	3										
	ROLA													49	2	1							
	ROLB													59	2	1							
Rotate Right	ROR							66	6	2	76	6	3										
	RORA													46	2	1							
	RORB													56	2	1							

The Condition Code Register notes are listed after Table 10.

(Continued)



HD6801V0, HD6801V5

• New Instructions

In addition to the existing 6800 Instruction Set, the following new instructions are incorporated in the HD6801V Microcomputer.

- ABX** Adds the 8-bit unsigned accumulator B to the 16-bit X-Register taking into account the possible carry out of the low order byte of the X-Register.
- ADDD** Adds the double precision ACCD* to the double precision value M:M+1 and places the results in ACCD.
- ASLD** Shifts all bits of ACCD one place to the left. Bit 0 is loaded with zero. The C bit is loaded from the most significant bit of ACCD.
- LDD** Loads the contents of double precision memory location into the double accumulator A:B. The condition codes are set according to the data.
- LSRD** Shifts all bits of ACCD one place to the right. Bit 15 is loaded with zero. The C bit is loaded from the least significant bit to ACCD.
- MUL** Multiplies the 8 bits in accumulator A with the 8 bits in accumulator B to obtain a 16-bit unsigned number in A:B, ACCA contains MSB of result.
- PSHX** The contents of the index register is pushed onto the stack at the address contained in the stack pointer. The stack pointer is decremented by 2.
- PULX** The index register is pulled from the stack beginning at the current address contained in the stack pointer +1. The stack pointer is incremented by 2 in total.
- STD** Stores the contents of double accumulator A:B in memory. The contents of ACCD remain unchanged.
- SUBD** Subtracts the contents of M:M + 1 from the contents of double accumulator AB and places the result in ACCD.
- BRN** Never branches. If effect, this instruction can be considered a two byte NOP (No operation) requiring three cycles for execution.
- CPX** Internal processing modified to permit its use with any conditional branch instruction.

*ACCD is the 16 bit register (A:B) formed by concatenating the A and B accumulators. The A-accumulator is the most significant byte.

Table B Index Register and Stack Manipulation Instructions

Pointer Operations	Mnemonic	Addressing Modes										Boolean/ Arithmetic Operation	Condition Code Register										
		IMMED.			DIRECT			INDEX			EXTND			IMPLIED			5	4	3	2	1	0	
		OP	~	#	OP	~	#	OP	~	#	OP		~	#	OP	~	#	H	I	N	Z	V	C
Compare Index Reg	CPX	8C	4	3	9C	5	2	AC	6	2	BC	6	3			X - M : M + 1	•	•	‡	‡	‡	‡	
Decrement Index Reg	DEX													09	3	1	X - 1 → X	•	•	•	‡	•	•
Decrement Stack Pntr	DES													34	3	1	SP - 1 → SP	•	•	•	•	•	•
Increment Index Reg	INX													08	3	1	X + 1 → X	•	•	•	‡	•	•
Increment Stack Pntr	INS													31	3	1	SP + 1 → SP	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	5	2	FE	5	3			M → X _H , (M + 1) → X _L	•	•	⑦	‡	R	•	
Load Stack Pntr	LDS	8E	3	3	9E	4	2	AE	5	2	BE	5	3			M → SP _H , (M + 1) → SP _L	•	•	⑦	‡	R	•	
Store Index Reg	STX				DF	4	2	EF	5	2	FF	5	3			X _H → M, X _L → (M + 1)	•	•	⑦	‡	R	•	
Store Stack Pntr	STS				9F	4	2	AF	5	2	BF	5	3			SP _H → M, SP _L → (M + 1)	•	•	⑦	‡	R	•	
Index Reg → Stack Pntr	TXS													35	3	1	X - 1 → SP	•	•	•	•	•	•
Stack Pntr → Index Reg	TSX													30	3	1	SP + 1 → X	•	•	•	•	•	•
Add	ABX													3A	3	1	B + X → X	•	•	•	•	•	•
Push Data	PSHX													3C	4	1	X _L → M _{sp} , SP - 1 → SP X _H → M _{sp} , SP - 1 → SP	•	•	•	•	•	•
Pull Data	PULX													38	5	1	SP + 1 → SP, M _{sp} → X _H SP + 1 → SP, M _{sp} → X _L	•	•	•	•	•	•

The Condition Code Register notes are listed after Table 10.



Table 11 Instruction Execution Times in Machine Cycle

	ACCX	Imme- diate	Direct	Ex- tended	In- dexed	Im- plied	Re- lative		ACCX	Imme- diate	Direct	Ex- tended	In- dexed	Im- plied	Re- lative
ABA	•	•	•	•	•	2	•	INX	•	•	•	•	•	3	•
ABX	•	•	•	•	•	3	•	JMP	•	•	•	3	3	•	•
ADC	•	2	3	4	4	•	•	JSR	•	•	5	6	6	•	•
ADD	•	2	3	4	4	•	•	LDA	•	2	3	4	4	•	•
ADDD	•	4	5	6	6	•	•	LDD	•	3	4	5	5	•	•
AND	•	2	3	4	4	•	•	LDS	•	3	4	5	5	•	•
ASL	2	•	•	6	6	•	•	LDX	•	3	4	5	5	•	•
ASLD	•	•	•	•	•	3	•	LSR	2	•	•	6	6	•	•
ASR	2	•	•	6	6	•	•	LSRD	•	•	•	•	•	3	•
BCC	•	•	•	•	•	•	3	MUL	•	•	•	•	•	10	•
BCS	•	•	•	•	•	•	3	NEG	2	•	•	6	6	•	•
BEQ	•	•	•	•	•	•	3	NOP	•	•	•	•	•	2	•
BGE	•	•	•	•	•	•	3	ORA	•	2	3	4	4	•	•
BGT	•	•	•	•	•	•	3	PSH	3	•	•	•	•	•	•
BHI	•	•	•	•	•	•	3	PSHX	•	•	•	•	•	4	•
BIT	•	2	3	4	4	•	•	PUL	4	•	•	•	•	•	•
BLE	•	•	•	•	•	•	3	PULX	•	•	•	•	•	5	•
BLS	•	•	•	•	•	•	3	ROL	2	•	•	6	6	•	•
BLT	•	•	•	•	•	•	3	ROR	2	•	•	6	6	•	•
BMI	•	•	•	•	•	•	3	RTI	•	•	•	•	•	10	•
BNE	•	•	•	•	•	•	3	RTS	•	•	•	•	•	5	•
BPL	•	•	•	•	•	•	3	SBA	•	•	•	•	•	2	•
BRA	•	•	•	•	•	•	3	SBC	•	2	3	4	4	•	•
BRN	•	•	•	•	•	•	3	SEC	•	•	•	•	•	2	•
BSR	•	•	•	•	•	•	6	SEI	•	•	•	•	•	2	•
BVC	•	•	•	•	•	•	3	SEV	•	•	•	•	•	2	•
BVS	•	•	•	•	•	•	3	STA	•	•	3	4	4	•	•
CBA	•	•	•	•	•	2	•	STD	•	•	4	5	5	•	•
CLC	•	•	•	•	•	2	•	STS	•	•	4	5	5	•	•
CLI	•	•	•	•	•	2	•	STX	•	•	4	5	5	•	•
CLR	2	•	•	6	6	•	•	SUB	•	2	3	4	4	•	•
CLV	•	•	•	•	•	2	•	SUBD	•	4	5	6	6	•	•
CMP	•	2	3	4	4	•	•	SWI	•	•	•	•	•	12	•
COM	2	•	•	6	6	•	•	TAB	•	•	•	•	•	2	•
CPX	•	4	5	6	6	•	•	TAP	•	•	•	•	•	2	•
DAA	•	•	•	•	•	2	•	TBA	•	•	•	•	•	2	•
DEC	2	•	•	6	6	•	•	TPA	•	•	•	•	•	2	•
DES	•	•	•	•	•	3	•	TST	2	•	•	6	6	•	•
DEX	•	•	•	•	•	3	•	TSX	•	•	•	•	•	3	•
EOR	•	2	3	4	4	•	•	TXS	•	•	•	•	•	3	•
INC	2	•	•	6	6	•	•	WAI	•	•	•	•	•	9	•
INS	•	•	•	•	•	3	•								

● Summary of Cycle by Cycle Operation

Table 12 provides a detailed description of the information present on the Address Bus, Data Bus, and the Read/Write line (R/W) during each cycle for each instruction.

This information is useful in comparing actual with expected results during debug of both software and hardware as the

control program is executed. The information is categorized in groups according to addressing mode and number of cycles per instruction. (In general, instructions with the same addressing mode and number of cycles execute in the same manner; exceptions are indicated in the table).

Table 12 Cycle by Cycle Operation

Address Mode & Instructions	Cycles	Cycle #	Address Bus	R/W Line	Data Bus
IMMEDIATE					
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	2	1 2	Op Code Address Op Code Address + 1	1 1	Op Code Operand Data
LDS LDX LDD	3	1 2 3	Op Code Address Op Code Address + 1 Op Code Address + 2	1 1 1	Op Code Operand Data (High Order Byte) Operand Data (Low Order Byte)
CPX SUBD ADD	4	1 2 3 4	Op Code Address Op Code Address + 1 Op Code Address + 2 Address Bus FFFF	1 1 1 1	Op Code Operand Data (High Order Byte) Operand Data (Low Order Byte) Low Byte of Restart Vector
DIRECT					
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	3	1 2 3	Op Code Address Op Code Address + 1 Address of Operand	1 1 1	Op Code Address of Operand Operand Data
STA	3	1 2 3	Op Code Address Op Code Address + 1 Destination Address	1 1 0	Op Code Destination Address Data from Accumulator
LDS LDX LDD	4	1 2 3 4	Op Code Address Op Code Address + 1 Address of Operand Operand Address + 1	1 1 1 1	Op Code Address of Operand Operand Data (High Order Byte) Operand Data (Low Order Byte)
STS STX STD	4	1 2 3 4	Op Code Address Op Code Address + 1 Address of Operand Address of Operand + 1	1 1 0 0	Op Code Address of Operand Register Data (High Order Byte) Register Data (Low Order Byte)
CPX SUBD ADD	5	1 2 3 4 5	Op Code Address Op Code Address + 1 Operand Address Operand Address + 1 Address Bus FFFF	1 1 1 1 1	Op Code Address of Operand Operand Data (High Order Byte) Operand Data (Low Order Byte) Low Byte of Restart Vector
JSR	5	1 2 3 4 5	Op Code Address Op Code Address + 1 Subroutine Address Stack Pointer Stack Pointer + 1	1 1 1 0 0	Op Code Irrelevant Data First Subroutine Op Code Return Address (Low Order Byte) Return Address (High Order Byte)

(Continued)



Table 12 Cycle by Cycle Operation (Continued)

Address Mode & Instructions	Cycles	Cycle #	Address Bus	R/W Line	Data Bus
INDEXED					
JMP	3	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	4	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register Plus Offset	1	Operand Data
STA	4	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register Plus Offset	0	Operand Data
LDS LDX LDD	5	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register Plus Offset	1	Operand Data (High Order Byte)
		5	Index Register Plus Offset + 1	1	Operand Data (Low Order Byte)
STS STX STD	5	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register Plus Offset	0	Operand Data (High Order Byte)
		5	Index Register Plus Offset + 1	0	Operand Data (Low Order Byte)
ASL LSR ASR NEG CLR ROL COM ROR DEC TST* INC	6	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register Plus Offset	1	Current Operand Data
		5	Address Bus FFFF	1	Low Byte of Restart Vector
		6	Index Register Plus Offset	0	New Operand Data
CPX SUBD ADDD	6	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register + Offset	1	Operand Data (High Order Byte)
		5	Index Register + Offset + 1	1	Operand Data (Low Order Byte)
		6	Address Bus FFFF	1*	Low Byte of Restart Vector
JSR	6	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Index Register + Offset	1	First Subroutine Op Code
		5	Stack Pointer	0	Return Address (Low Order Byte)
		6	Stack Pointer - 1	0	Return Address (High Order Byte)

* In the TST instruction, R/W line of the sixth cycle is "1" level, and AB=FFFF, DB=Low Byte of Reset Vector.

(Continued)



Table 12 Cycle by Cycle Operation (Continued)

Address Mode & Instructions	Cycles	Cycle #	Address Bus	R/W Line	Data Bus
EXTENDED					
JMP	3	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Jump Address (High Order Byte)
		3	Op Code Address + 2	1	Jump Address (Low Order Byte)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	4	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	Address of Operand	1	Operand Data
STA	4	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Destination Address (High Order Byte)
		3	Op Code Address + 2	1	Destination Address (Low Order Byte)
		4	Operand Destination Address	0	Data from Accumulator
LDS LDX LDD	5	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	Address of Operand	1	Operand Data (High Order Byte)
		5	Address of Operand + 1	1	Operand Data (Low Order Byte)
STS STX STD	5	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	Address of Operand	0	Operand Data (High Order Byte)
		5	Address of Operand + 1	0	Operand Data (Low Order Byte)
ASL LSR ASR NEG CLR ROL COM ROR DEC TST* INC	6	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	Address of Operand	1	Current Operand Data
		5	Address Bus FFFF	1	Low Byte of Restart Vector
		6	Address of Operand	0	New Operand Data
CPX SUBD ADD	6	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Operand Address (High Order Byte)
		3	Op Code Address + 2	1	Operand Address (Low Order Byte)
		4	Operand Address	1	Operand Data (High Order Byte)
		5	Operand Address + 1	1	Operand Data (Low Order Byte)
		6	Address Bus FFFF	1	Low Byte of Restart Vector
JSR	6	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Address of Subroutine (High Order Byte)
		3	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
		4	Subroutine Starting Address	1	Op Code of Next Instruction
		5	Stack Pointer	0	Return Address (Low Order Byte)
		6	Stack Pointer - 1	0	Return Address (High Order Byte)

* In the TST instruction, R/W line of the sixth cycle is "1" level, and AB = FFFF, DB = Low Byte of Reset Vector.

(Continued)



Table 12 Cycle by Cycle Operation (Continued)

Address Mode & Instructions	Cycles	Cycle #	Address Bus	R/W Line	Data Bus
IMPLIED					
ABA DAA SEC ASL DEC SEI ASR INC SEV CBA LSR TAB CLC NEG TAP CLI NOP TBA CLR ROL TPA CLV ROR TST COM SBA	2	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Op Code of Next Instruction
ABX	3	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Irrelevant Data
		3	Address Bus FFFF	1	Low Byte of Restart Vector
ASLD LSRD	3	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Irrelevant Data
		3	Address Bus FFFF	1	Low Byte of Restart Vector
DES INS	3	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Op Code of Next Instruction
		3	Previous Register Contents	1	Irrelevant Data
INX DEX	3	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Op Code of Next Instruction
		3	Address Bus FFFF	1	Low Byte of Restart Vector
PSHA PSHB	3	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Op Code of Next Instruction
		3	Stack Pointer	0	Accumulator Data
TSX	3	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Op Code of Next Instruction
		3	Stack Pointer	1	Irrelevant Data
TXS	3	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Op Code of Next Instruction
		3	Address Bus FFFF	1	Low Byte of Restart Vector
PULA PULB	4	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Op Code of Next Instruction
		3	Stack Pointer	1	Irrelevant Data
		4	Stack Pointer + 1	1	Operand Data from Stack
PSHX	4	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Irrelevant Data
		3	Stack Pointer	0	Index Register (Low Order Byte)
		4	Stack Pointer - 1	0	Index Register (High Order Byte)
PULX	5	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Irrelevant Data
		3	Stack Pointer	1	Irrelevant Data
		4	Stack Pointer + 1	1	Index Register (High Order Byte)
		5	Stack Pointer + 2	1	Index Register (Low Order Byte)
RTS	5	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Irrelevant Data
		3	Stack Pointer	1	Irrelevant Data
		4	Stack Pointer + 1	1	Address of Next Instruction (High Order Byte)
		5	Stack Pointer + 2	1	Address of Next Instruction (Low Order Byte)
WAI**	9	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Op Code of Next Instruction
		3	Stack Pointer	0	Return Address (Low Order Byte)
		4	Stack Pointer - 1	0	Return Address (High Order Byte)

(Continued)



Table 12 Cycle by Cycle Operation (Continued)

Address Mode & Instructions	Cycles	Cycle #	Address Bus	R/W Line	Data Bus
WAI**		5	Stack Pointer - 2	0	Index Register (Low Order Byte)
		6	Stack Pointer - 3	0	Index Register (High Order Byte)
		7	Stack Pointer - 4	0	Contents of Accumulator A
		8	Stack Pointer - 5	0	Contents of Accumulator B
		9	Stack Pointer - 6	0	Contents of Cond. Code Register
MUL	10	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Irrelevant Data
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Address Bus FFFF	1	Low Byte of Restart Vector
		5	Address Bus FFFF	1	Low Byte of Restart Vector
		6	Address Bus FFFF	1	Low Byte of Restart Vector
		7	Address Bus FFFF	1	Low Byte of Restart Vector
		8	Address Bus FFFF	1	Low Byte of Restart Vector
		9	Address Bus FFFF	1	Low Byte of Restart Vector
		10	Address Bus FFFF	1	Low Byte of Restart Vector
RTI	10	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Irrelevant Data
		3	Stack Pointer	1	Irrelevant Data
		4	Stack Pointer + 1	1	Contents of Cond. Code Reg. from Stack
		5	Stack Pointer + 2	1	Contents of Accumulator B from Stack
		6	Stack Pointer + 3	1	Contents of Accumulator A from Stack
		7	Stack Pointer + 4	1	Index Register from Stack (High Order Byte)
		8	Stack Pointer + 5	1	Index Register from Stack (Low Order Byte)
		9	Stack Pointer + 6	1	Next Instruction Address from Stack (High Order Byte)
		10	Stack Pointer + 7	1	Next Instruction Address from Stack (Low Order Byte)
SWI	12	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Irrelevant Data
		3	Stack Pointer	0	Return Address (Low Order Byte)
		4	Stack Pointer - 1	0	Return Address (High Order Byte)
		5	Stack Pointer - 2	0	Index Register (Low Order Byte)
		6	Stack Pointer - 3	0	Index Register (High Order Byte)
		7	Stack Pointer - 4	0	Contents of Accumulator A
		8	Stack Pointer - 5	0	Contents of Accumulator B
		9	Stack Pointer - 6	0	Contents of Cond. Code Register
		10	Stack Pointer - 7	1	Irrelevant Data
		11	Vector Address FFFA (Hex)	1	Address of Subroutine (High Order Byte)
		12	Vector Address FFFB (Hex)	1	Address of Subroutine (Low Order Byte)

**While the MCU is in the "Wait" state, its bus state will appear as a series of MCU reads of an address which is seven locations less than the original contents of the Stack Pointer. Contrary to the HD6800, none of the ports are driven to the high impedance state by a WAI instruction.

(Continued)



HD6801V0, HD6801V5

Table 12 Cycle by Cycle Operation (Continued)

Address Mode & Instruction	Cycles	Cycle #	Address Bus	R/W Line	Data Bus
RELATIVE					
BCC BHT BNE	3	1	Op Code Address	1	Op Code
BCS BLE BPL		2	Op Code Address + 1	1	Branch Offset
BEQ BLS BRA		3	Address Bus FFFF	1	Low Byte of Restart Vector
BGE BLT BVC					
BGT BMT BVS BRN					
BSR	6	1	Op Code Address	1	Op Code
		2	Op Code Address + 1	1	Branch Offset
		3	Address Bus FFFF	1	Low Byte of Restart Vector
		4	Subroutine Starting Address	1	Op Code of Next Instruction
		5	Stack Pointer	0	Return Address (Low Order Byte)
		6	Stack Pointer - 1	0	Return Address (High Order Byte)

● **Summary of Undefined Instruction Operations**

The HD6801V has 36 undefined instructions. When these are carried out, the contents of Register and Memory in MCU change at random.

When the op codes (4E, 5E) are used to execute, the MCU continues to increase the program counter and it will not stop until the Reset signal enters. These op codes are used to test the LSI.

Table 13 Op codes Map

HD6801V MICROCOMPUTER INSTRUCTIONS																	
OP CODE										ACCA or SP				ACCB or X			
		ACC A	ACC B	IND	EXT	IMM	DIR	IND	EXT	IMM	DIR	IND	EXT				
LO	HI	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0		SBA	BRA	TSX	NEG				SUB				0			
0001	1	NOP	CBA	BRN	INS					CMP							
0010	2			BHI	PULA (+1)					SBC							
0011	3			BLS	PULB (+1)	COM				*	SUBD (+2)		*	ADDD (+2)	3		
0100	4	LSRD (+1)		BCC	DES	LSR				AND				4			
0101	5	ASLD (+1)		BCS	TXS					BIT				5			
0110	6	TAP	TAB	BNE	PSHA	ROR				LDA				6			
0111	7	TPA	TBA	BEQ	PSHB	ASR					STA		STA	7			
1000	8	INX (+1)		BVC	PULX (+2)	ASL				EOR				8			
1001	9	DEX (+1)	DAA	BVS	RTS (+2)	ROL				ADC				9			
1010	A	CLV		BPL	ABX	DEC				ORA				A			
1011	B	SEV	ABA	BMI	RTI (+7)					ADD				B			
1100	C	CLC		BGE	PSHX (+1)	INC				*	CPX (+2)		*	LDD (+1)	C		
1101	D	SEC		BLT	MUL (+7)	TST				BSR (+4)	JSR (+2)	*	(+1)	STD (+1)	D		
1110	E	CLI		BGT	WAI (+6)	**	JMP (-3)			*	LDS (+1)		*	LDX (+1)	E		
1111	F	SEI		BLE	SWI (+9)	CLR				*	(+1)	STS (+1)	*	(+1)	STX (+1)	F	
BYTE/CYCLE		1/2	1/2	2/3	1/3	1/2	1/2	2/6	3/6	2/2	2/3	2/4	3/4	2/2	2/3	2/4	3/4

- (NOTES)
- 1) Undefined Op codes are marked with .
 - 2) () indicate that the number in parenthesis must be added to the cycle count for that instruction.
 - 3) The instructions shown below are all 3 bytes and are marked with "****". Immediate addressing mode of SUBD, CPX, LDS, ADDD, LDD and LDX instructions, and undefined op codes (8F, CD, CF).
 - 4) The Op codes (4E, 5E) are 1 byte/∞ cycles instructions, and are marked with "****"



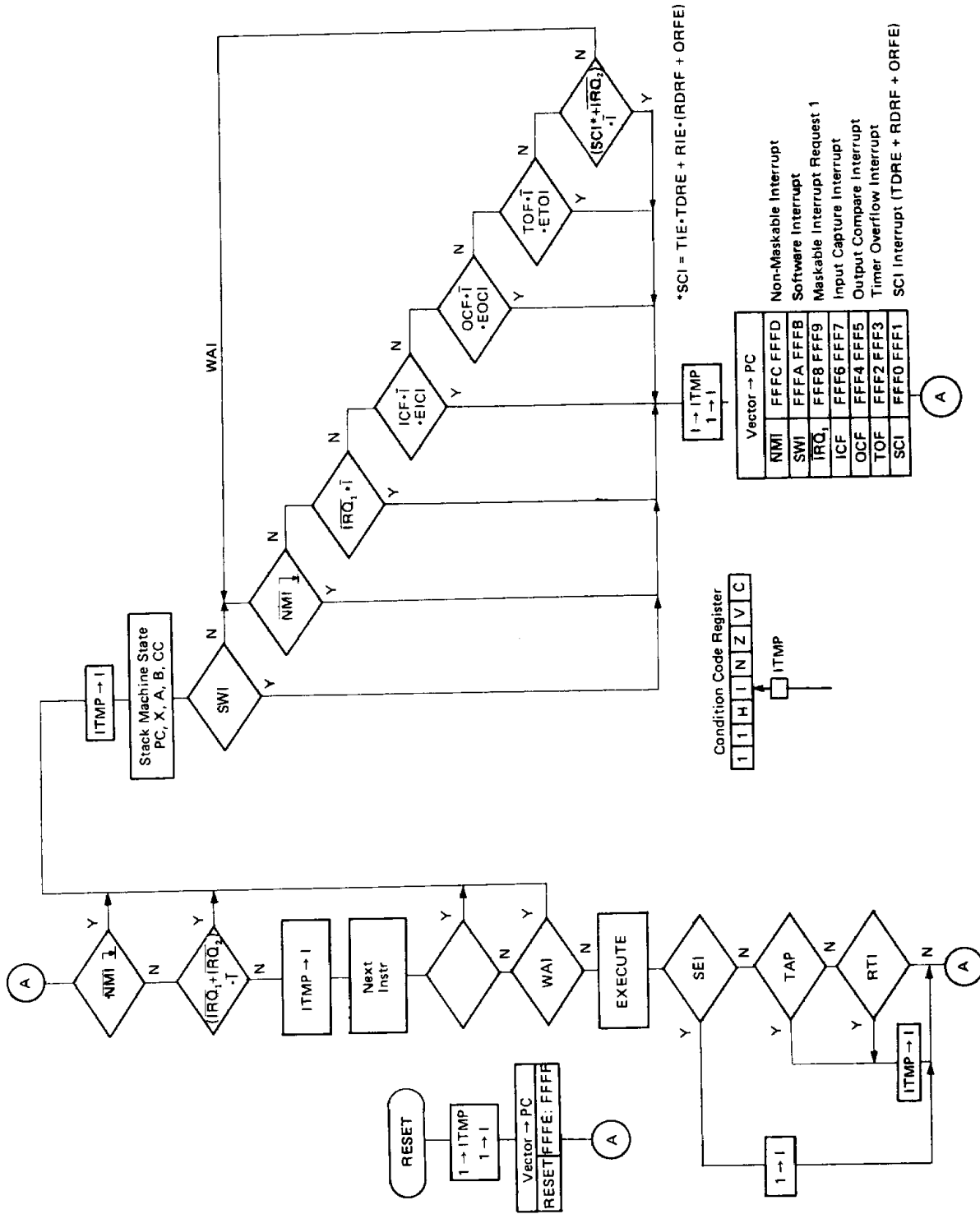


Figure 24 Interrupt Flowchart

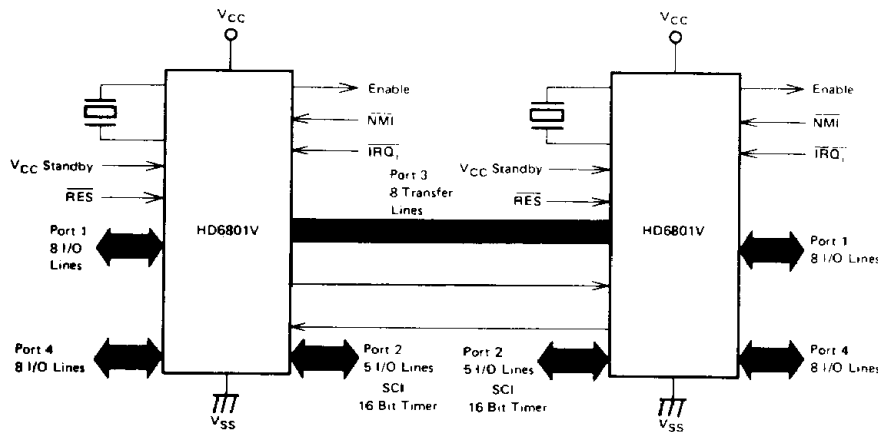


Figure 25 HD6801V MCU Single-Chip Dual Processor Configuration

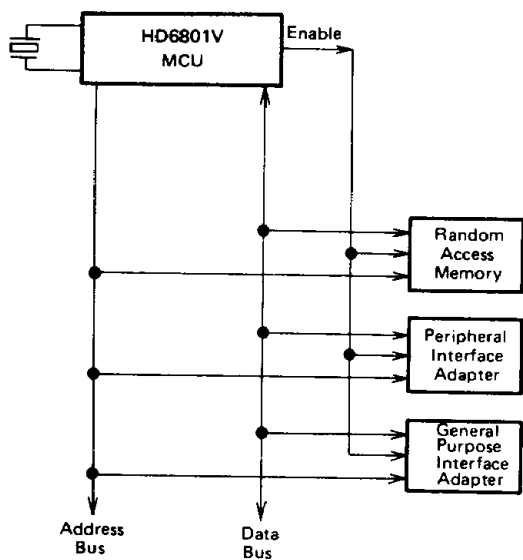


Figure 26 HD6801V MCU Expanded Non-Multiplexed Mode

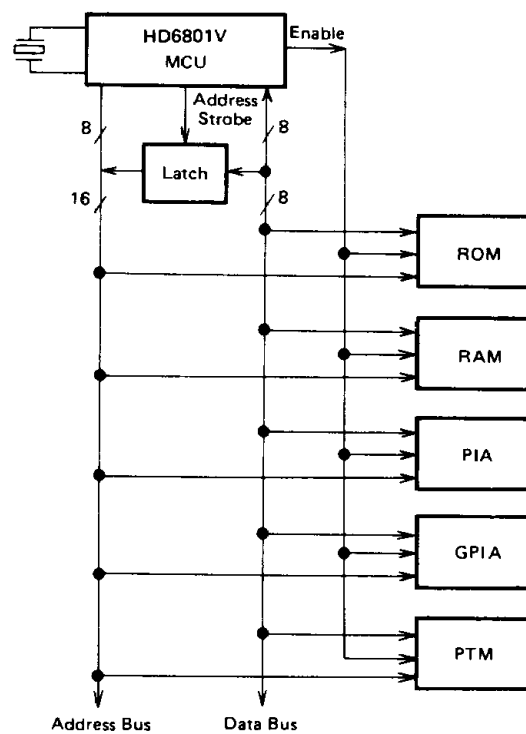


Figure 27 HD6801V MCU Expanded Multiplexed Mode

■ PRECAUTIONS

● PRECAUTION CONCERNING COUNTER TIMER

(1) Timer Output (P₂₁)

After CPU reset, P₂₁ is uncertain until the value of the free running counter equals the value of the output compare register or until the free running counter completes a software time-out cycle.

(2) Initialization of ICF

ICF should be cleared by software after initiating a reset, otherwise ICF may be set if P₂₁ is "low" after initiating a reset.

● PRECAUTION CONCERNING WRITE-ONLY REGISTER

The write-only register cannot be changed like DDR for I/O ports using Read/Modify/Write instructions.

(1) The CPU cannot read the write-only register. Proceed with

Read/Modify/Write instructions as follows:

- (i) read the data of specified address;
- (ii) modify the data; and
- (iii) write the modified data to original address.

The Read/Modify/Write instructions cannot be used with the write-only register like DDR.

(2) Store instructions can be used for writing to the write-only register.

*Read/Modify/Write instructions—NEG, COM, LSR, ROR, ASR, ASL, ROL, DEC, INC, TST, CLR

■ PRECAUTION CONCERNING HD6801 SERIES SCI, TIMER STATUS FLAG

● Caution for the HD6801 Family SCI, TIMER Status Flag

The flags shown in Table 14 are cleared by reading/writing (flag reset condition 2) the data register corresponding to each flag after reading the status register (flag reset condition 1).

To clear the flag correctly, use the following procedure:

1. Read the status register
2. Test the flag
3. Read the data register

The SCI, Timer status flag is cleared by reading a "1" for each status flag and then reading the data register. SCI software routines should read the received data after confirming a "1" as the received status flag. Avoid reading dummy data after a "0" for the received status flag.

Table 14 Status Flag Reset Conditions

	Status Flag	Flag Reset Condition 1 (Status Register)	Flag Reset Condition 2 (Data Register)
TIMER	ICF	When each flag is "1", TRCSR/Read	ICR/Read
	OCF		OCR/Read
	TOF		TC/Read
SCI	RDRF	When Each flag is "1", TRCSR/Read	RDR/Read
	ORFE		RDR/Read
	TDRE		TDR/Write

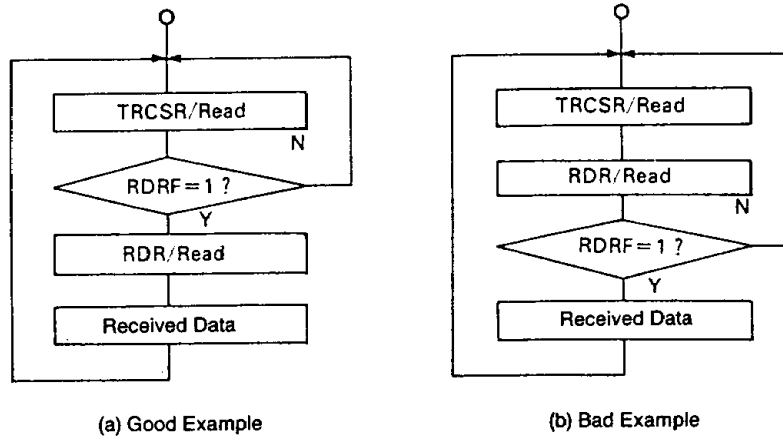


Figure 28 Software polling of SCI-RDRF

● TERMINAL CONDITION DURING RESET, AFTER RESET

Table 15 Terminal Condition During Reset, After Reset

CPU Mode		0	1	2	3	4	5	6	7
During Reset	Port 1	I Z	←	←	←	←	←	←	←
	Port 2	I Z	←	←	←	←	←	←	←
	Port 3	I Z	←	←	←	←	←	←	←
	Port 4	I H	←	←	←	←	←	←	←
	SC ₁	I/O H	←	←	←	I H	O H	I/O H	I H
	SC ₂	O H	←	←	←	←	←	←	←
After Reset	Port 1	I Z	←	←	←	←	←	←	←
	Port 2	I Z	←	←	←	←	←	←	←
	Port 3	I/O ABL/DB	←	←	←	I Z	I DB	I/O ABL/DB	I Z
	Port 4	O ABH	←	←	←	I H	←	←	←
	SC ₁	O AS	←	←	←	I H	O IOS	O AS	I H
	SC ₂	O R/W	←	←	←	O OS3	O R/W	←	O OS3

I : Input
 O : Output
 I/O : Input/Output
 Upper : Input Condition
 Lower : Level, Terminal Function
 H : High Level
 L : Low Level
 Z : High Impedance
 DB : Data Bus
 ABL : Address Bus Low
 ABH : Address Bus High
 AS : Address Strobe
 R/W : Read/Write
 IOS : IOS Signal
 OS3 : OS3 Signal

