



EMI/RFI T-Filter

Features

- Highly integrated bus termination network
- 1% absolute tolerance terminations
- Ultra-low crosstalk
- 18 terminating lines in QSOP package
- Saves board space and improves system reliability
- Reduces assembly cost and rework

Product Description

High speed microprocessors like Intel's Pentium® Pro Processor, demand unique, high speed bus termination schemes. The PACR6G series network provides 18 terminations per package. Four termination resistor values are available. The 47, 50 and 56 ohm terminations are suitable for use with the Intel server chip set and the 68 ohm termination is suitable for use with the Intel desktop chip set. The tight resistor tolerance minimizes noise contribution from termination mismatching.

The PACR6G network offers high performance, high reliability, and low cost through manufacturing efficiency. It meets or exceeds all Intel specifications for termina-

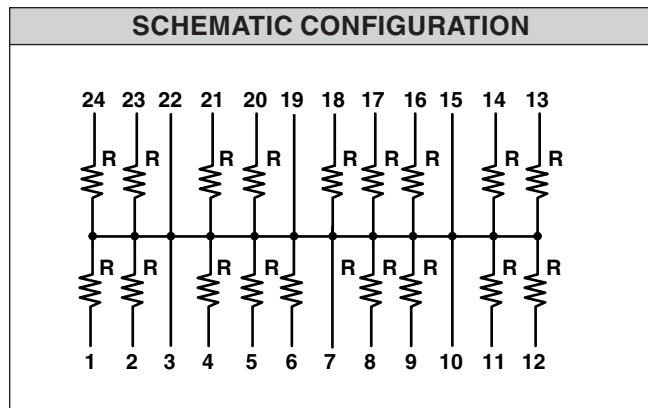
Applications

- Pentium® Pro servers & desktop systems
- Engineering workstations
- Embedded processor systems
- GTL, ECL, NTL, HSTL terminator

tion performance and provides an additional degree of system noise margin. The termination resistor elements are fabricated using state-of-the-art thin film manufacturing. This highly integrated solution is silicon-based and has the same reliability characteristics as any of today's microprocessor products. The thin film resistors[†] have excellent stability over temperature, over applied voltage, and over product life. In addition, the QSOP industry standard packaging is easy to handle in manufacturing and provides interconnect reliability — on par with other common semiconductor components — and far better than traditional thick film-based chip products.

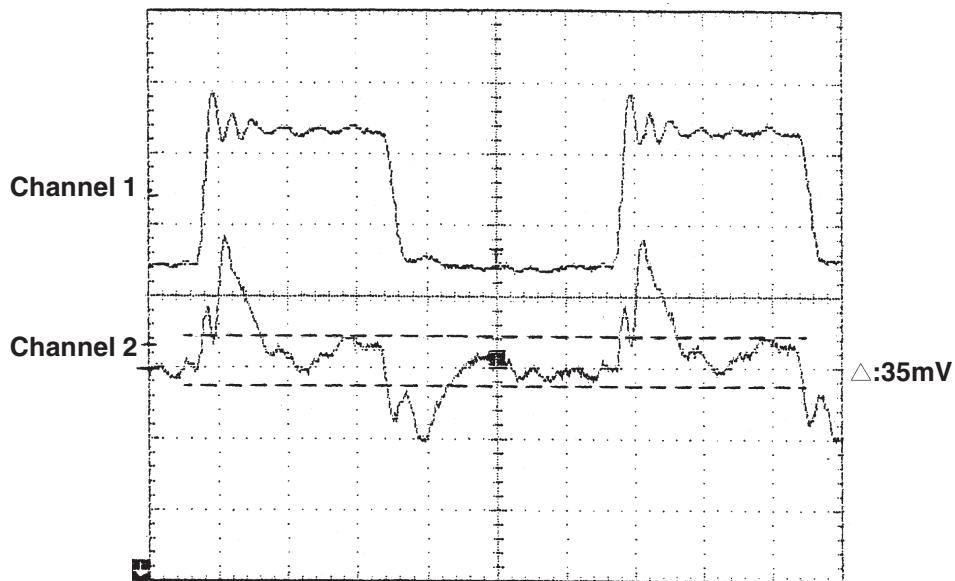
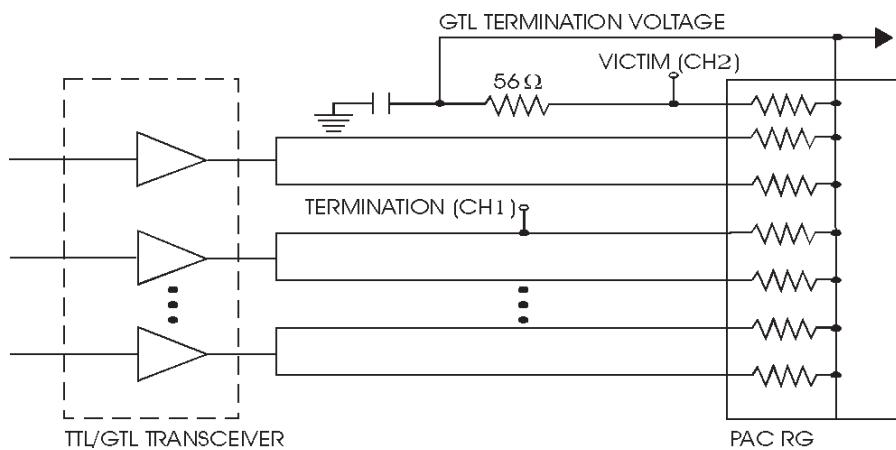
STANDARD SPECIFICATIONS	
Absolute Tolerance (0°C to 70°C)	±1%
Operating Temperature Range	0°C to 70°C
Power Rating/Resistor	100mW
Max Package Power Rating (70°C)	1.00w, Max
Crosstalk (See Test Circuit)	±18mV (typical)

STANDARD VALUES	
R (W)	Code
47	470
50	500
56	560
68	680



**Signal at Termination and Victim Line (TA = 25°C) (See Test Circuit)**

Channel 1 (500mV/division) Termination Signal, Channel 2 (50mV/division) Victim Voltage. The victim voltage crosstalk measures 35mV in the critical areas around the system clock. The system clock occurs approximately 4ns before each data transition. The horizontal dashed lines are 35mV apart. The time scale is 5.0ns/division. (The signal voltage rise and fall times have been adjusted at the driver to conform to Intel specifications.) Measurements made using Tektronix TDS820 6 GHz Digitizing Oscilloscope with P6207 FET Probes.

**Test Circuit Block Diagram**



Test Circuit

