

1. Description

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching applications.

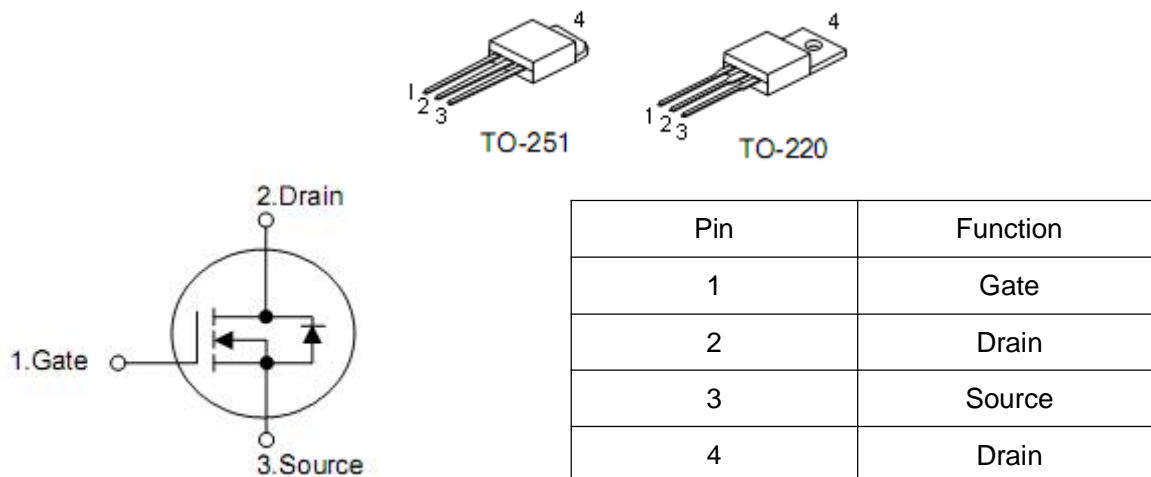
2. Features

- n $R_{DS(ON)}=72\text{ m}\Omega@V_{GS}=10\text{V}$
- n Improved dv/dt capability
- n Fast switching
- n 100% EAS guaranteed
- n Green device available

3. Applications

- n Networking
- n Load switch
- n Led applications

4. Symbol



5. Absolute maximum ratings

($T_A=25^{\circ}\text{C}$, unless otherwise noted)

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	100	V
Gate-source voltage		V_{GSS}	± 20	V
Operating junction temperature range		T_J	-50 to 150	$^{\circ}\text{C}$
Storage temperature range		T_{STG}	-50 to 150	$^{\circ}\text{C}$
Continuous drain current	$T_C=25^{\circ}\text{C}$	I_D	15	A
	$T_C=100^{\circ}\text{C}$		9.5	A
Pulsed drain current ¹		I_{DM}	60	A
Maximum power dissipation	$T_C=25^{\circ}\text{C}$	P_D	50	W
	Derate above 25°C		0.4	W/ $^{\circ}\text{C}$

6. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance, Junction-ambient	$R_{\theta JA}$	62	$^{\circ}\text{C}/\text{W}$
Thermal resistance, Junction-case	$R_{\theta JC}$	2.5	$^{\circ}\text{C}/\text{W}$

7. Electrical characteristics

(T_A=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	100	-	-	V
BV _{DSS} temperature coefficient	ΔBV _{DSS} /ΔT _J	Reference to 25°C, I _D =1mA	-	0.05	-	V/°C
Zero gate voltage drain current	I _{DSS}	V _{DS} =100V, V _{GS} =0V T _J =25°C	-	-	1	μA
		V _{DS} =80V, V _{GS} =0V T _J =125°C	-	-	10	
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	1.6	2.5	V
V _{GS(th)} temperature coefficient	ΔV _{GS(th)}		-	-5	-	mV/°C
Forward transconductance	g _{fs}	V _{DS} =10V, I _D =3A	-	8.7	-	S
Gate leakage current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} =10V, I _{DS} =5A	-	72	90	mΩ
Gate resistance	R _g	V _{DS} =0V, V _{GS} =0V, f=1MHz	-	1.3	2.6	Ω
Diode forward voltage	V _{SD}	I _{SD} =1A, V _{GS} =0V, T _J =25°C	-	-	1	V
Reverse recovery time ²	t _{rr}	I _S =1A, V _{GS} =30V dI _{SD} /dt=100A/μs, T _J =25°C	-	-	-	nS
Reverse recovery charge ²	Q _{rr}		-	-	-	nC
Input capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=1MHz	-	1480	2150	pF
Output capacitance	C _{oss}		-	480	700	
Reverse transfer capacitance	C _{rss}		-	35	55	
Turn-on delay time ^{2,3}	t _{d(on)}	V _{DD} =30V, I _D =1A, R _G =3.3Ω, V _{GS} =10V	-	2.9	6	ns
Rise time ^{2,3}	t _r		-	9.5	18	
Turn-off delay time ^{2,3}	t _{d(off)}		-	18.4	35	
Fall time ^{2,3}	t _f		-	5.3	10	
Total gate charge ^{2,3}	Q _g	V _{DS} =48V, V _{GS} =10V I _D =5A	-	9.3	13	nC
Gate-source charge ^{2,3}	Q _{gs}		-	2.1	4.2	
Gate-drain charge ^{2,3}	Q _{gd}		-	1.8	4	
Continuous source current	I _S	V _G =V _D =0V, force current	-	-	15	A
Pulsed source current	I _{SM}		-	-	60	A

Note : 1. Repetitive rating, pulse width limited by maximum junction temperature

2. The data tested by pulse, pulse width ≤ 300μs duty cycle ≤ 2%.

3. Essentially independent of operating temperature.

8. Test circuits and waveforms

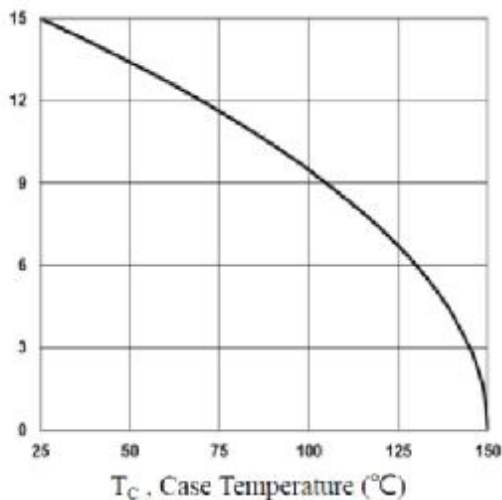


Fig.1 Continuous Drain Current vs. TC

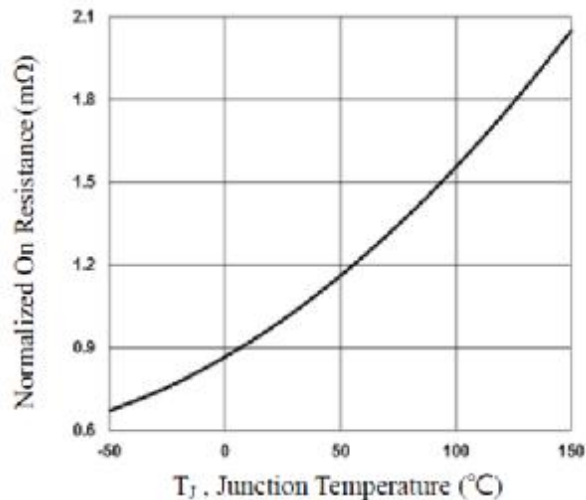


Fig.2 Normalized RDSON vs. TJ

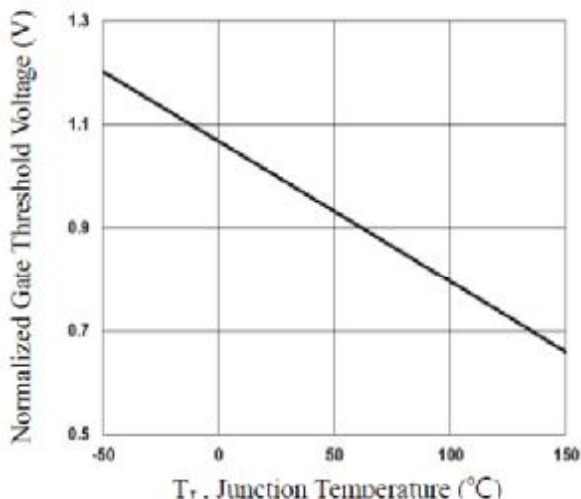


Fig.3 Normalized Vth vs. TJ

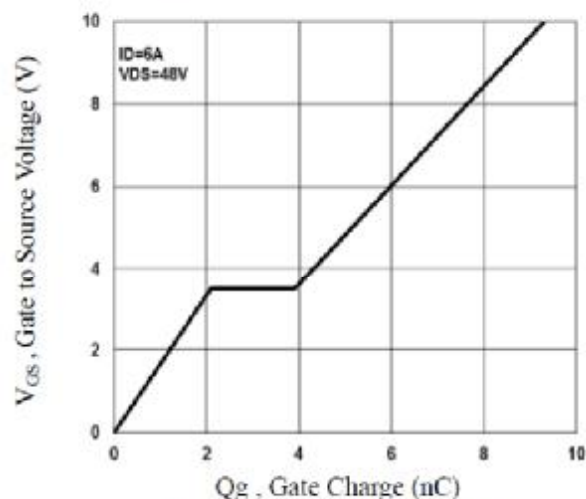


Fig.4 Gate Charge Characteristics

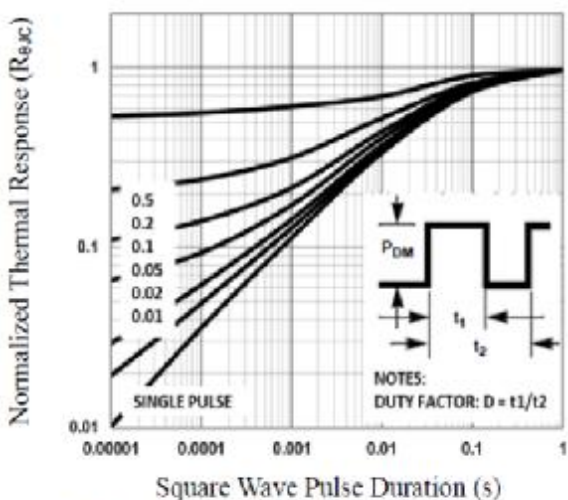


Fig.5 Normalized Transient Impedance

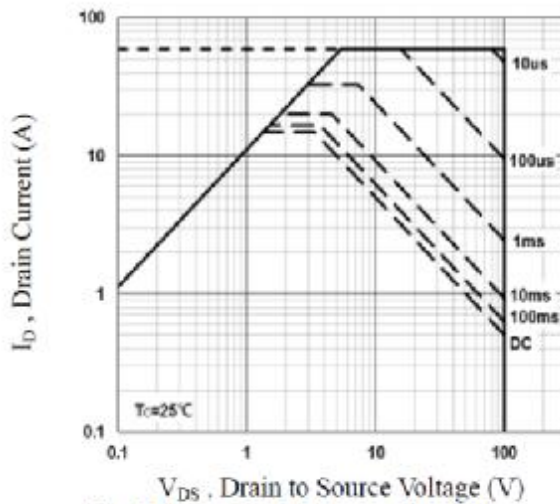


Fig.6 Maximum Safe Operation Area

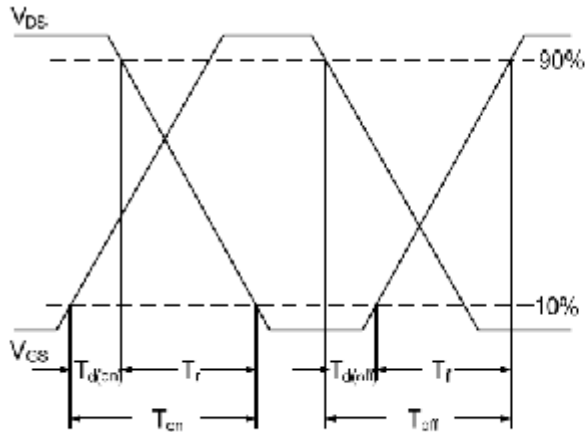


Fig.7 Switching Time Waveform

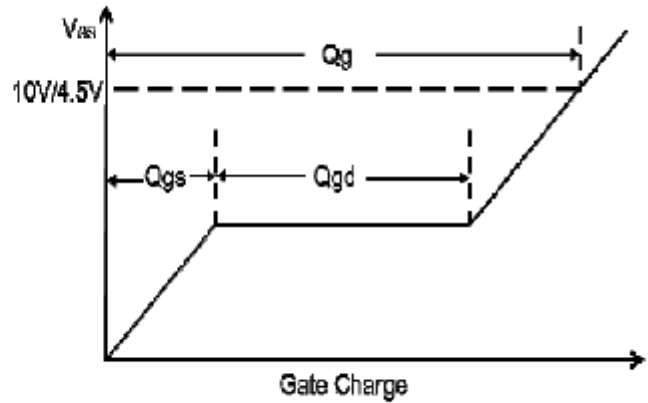


Fig.8 Gate Charge Waveform