AMERICAN MICROSYSTEMS, INC.

FS6245

Dual PLL VCXO Clock Generator IC

December 2000

1.0 Features

- On-chip tunable voltage-controlled crystal oscillator circuitry (VCXO) allows precise system frequency tuning (pull range typically 300ppm)
- VCXO tuning range: 0-3V
- Uses inexpensive fundamental-mode crystals
- Two integrated phase-locked loops (PLL) multiply VCXO frequency to the higher system frequencies needed
- 5V core supply voltage (contact factory for 3.3V)
- 3.3V / 5V output supply voltage
- Small circuit board footprint (20-pin SOIC)
- Custom frequency selections available - contact your local AMI Sales Representative for more information

2.0 Description

The FS6245 is a monolithic CMOS clock generator IC designed to minimize cost and component count in digital video/audio systems.

At the core of the FS6245 is circuitry that implements a voltage-controlled crystal oscillator when an external resonator is attached. The VCXO allows device frequencies to be precisely adjusted for use in systems that have frequency matching requirements, such as digital satellite receivers.

Two high-resolution phase-locked loops generate the output clock frequencies (CLKA, CLKB, and CLKC). These frequencies are phase-locked and frequency-locked to the VCXO frequency. Synthesis error of the PLLs is +/-0 ppm unless otherwise noted.

Figure 1: Pin Configuration

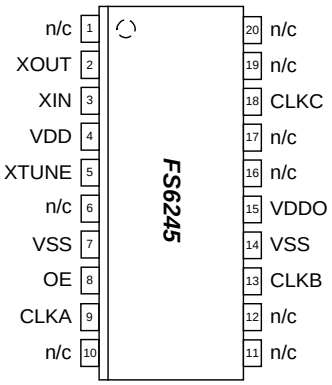
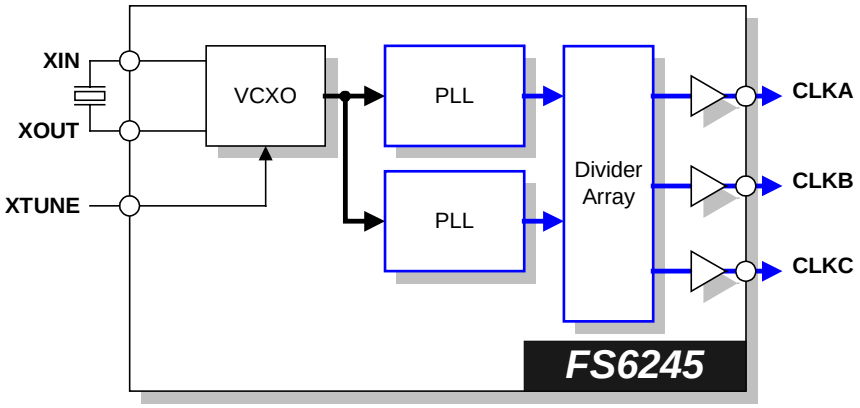


Table 1: Crystal / Output Frequencies

DEVICE	f_{XIN} (MHz)	CLKA (MHz)	CLKB (MHz)	CLKC (MHz)
FS6245-01	13.500	11.0592	18.432	27.000

NOTE: Contact AMI for custom PLL frequencies

Figure 2: Block Diagram



ISO9001

Table 2: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION
1	-	N/C	No Connection
2	AI	XIN	VCXO Crystal Feedback
3	AO	XOUT / FREF	VCXO Crystal Drive / External Reference Clock Input
4	P	VDD	Core Power Supply
5	AI	XTUNE	VCXO Tune Input
6	-	N/C	No Connection
7	P	VSS	Ground
8	DI^U	OE	Output Enable
9	DO	CLKA	Clock Output “A”
10	-	N/C	No Connection
11	-	N/C	No Connection
12	-	N/C	No Connection
13	DO	CLKB	Clock Output “B”
14	P	VSS	Ground
15	P	VDDO	Output Power Supply (must be less than or equal to VDD)
16	-	N/C	No Connection
17	-	N/C	No Connection
18	DO	CLKC	Clock Output “C”
19	-	N/C	No Connection
20	-	N/C	No Connection

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3.0 Functional Block Description

3.1 Phase-Locked Loop (PLL)

The on-chip PLL is a standard frequency- and phase-locked loop architecture. The PLL multiplies the reference oscillator to the desired frequency by a ratio of integers. The frequency multiplication is exact with a zero synthesis error (unless otherwise noted).

3.2 Voltage-Controlled Crystal Oscillator (VCXO)

The VCXO provides a tunable, low-jitter frequency reference for the rest of the FS6245 system components. Loading capacitance for the crystal is internal to the FS6245. No external components (other than the crystal resonator itself) are required for operation of the VCXO.

Continuous fine-tuning of the VCXO frequency is accomplished by varying the voltage on the XTUNE pin.

The oscillator operates the crystal resonator in the parallel-resonant mode. Crystal warping, or the “pulling” of the crystal oscillation frequency, is accomplished by altering the effective load capacitance presented to the crystal by the oscillator circuit. The actual amount that changing the load capacitance alters the oscillator frequency will be dependent on the characteristics of the crystal as well as the oscillator circuit itself.

Specifically, the motional capacitance of the crystal (usually referred to by crystal manufacturers as C_1), the static capacitance of the crystal (C_0), and the load capacitance (C_L) of the oscillator determine the “warping” or “pulling” capability of the crystal in the oscillator circuit.

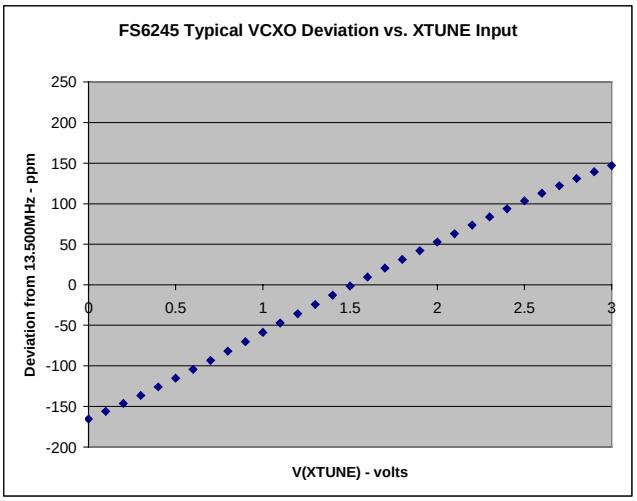
A simple formula to obtain the warping capability of a crystal oscillator is:

$$\Delta f\ (ppm) = \frac{C_1 \times (C_{L2} - C_{L1}) \times 10^6}{2 \times (C_0 + C_{L2}) \times (C_0 + C_{L1})}$$

where C_{L1} and C_{L2} are the two extremes of the applied load capacitance.

EXAMPLE: A crystal with the following parameters is used. With C_1 = 0.025pF, C_0 = 6pF, C_{L1} = 10pF, and C_{L2} = 20pF, the tuning range is

$$\Delta f = \frac{0.025 \times (20 - 10) \times 10^6}{2 \times (6 + 20) \times (6 + 10)} = 300\,ppm.$$



4.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Core Supply Voltage (VDD)	V_{DD}	5V ± 10%	4.75	5	5.25	V
CLK Pin Supply Voltage (VDDO)	V_{DDO}		3.0	-	V_{DD}+0.3	V
Ambient Operating Temperature Range	T_A		0		70	°C
Crystal Resonator Frequency	f_{XTAL}	Fundamental Mode	5	13.5	18	MHz
Crystal Resonator Motional Capacitance	$C_{1(xtal)}$	AT cut		25		fF
Crystal Load Capacitance	$C_{L(xtal)}$	AT cut		14		pF

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Table 5: DC Electrical Specifications

Unless otherwise stated, V_{DD} = 5V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{XTAL} = 13.5MHz; C_L = 10pF		20		mA
Voltage Controlled Crystal Oscillator - VDD=5.0V						
Crystal Loading Capacitance	$C_{L(xtal)}$	As seen by a crystal connected to XIN and XOUT (@ V_{XTUNE} = 1.65V)		14		pF
Crystal Resonator Motional Capacitance	$C_{1(xtal)}$	AT cut		25		fF
VCXO Tuning Range		f_{XTAL} = 13.5MHz; $C_{L(xtal)}$ = 14pF; $C_{1(xtal)}$ = 25fF		300		ppm
VCXO Tuning Characteristic		Note: positive ΔF for positive ΔV		100		ppm/V
Crystal Drive Level		R_{XTAL}=20Ω; $C_{L(xtal)}$ = 14pF		200		uW
Clock Outputs (CLKx) - VDDO=3.3V						
High-Level Output Source Current *	I_{OH}	V_O = 2.0V		-40		mA
Low-Level Output Sink Current *	I_{OL}	V_O = 0.4V		17		mA
Output Impedance *	z_{OH}	V_O = 0.5V_{DD}; output driving high		30		Ω
	z_{OL}	V_O = 0.5V_{DD}; output driving low		30		
Short Circuit Source Current *	I_{OSH}	V_O = 0V; shorted for 30s, max.		-55		mA
Short Circuit Sink Current *	I_{OSL}	V_O = 3.3V; shorted for 30s, max.		55		mA
Clock Outputs (CLKx) - VDDO=5.0V						
High-Level Output Source Current *	I_{OH}	V_O = 4.5V		-30		mA
Low-Level Output Sink Current *	I_{OL}	V_O = 0.4V		26		mA
Output Impedance *	z_{OH}	V_O = 0.5V_{DD}; output driving high		25		Ω
	z_{OL}	V_O = 0.5V_{DD}; output driving low		25		
Short Circuit Source Current *	I_{OSH}	V_O = 0V; shorted for 30s, max.		-100		mA
Short Circuit Sink Current *	I_{OSL}	V_O = 5V; shorted for 30s, max.		100		mA

Table 6: AC Timing Specifications

Unless otherwise stated, V_{DD} = 5V ± 10%, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits. Where given, MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
VCXO Stabilization Time *	$t_{VCXOSTB}$	From power valid		10		ms
PLL Stabilization Time *	t_{PLLSTB}	From VCXO stable		500		us
Output Frequency Synthesis Error		(unless otherwise noted in Frequency Table)			0	ppm
Clock Output (CLK)						
Duty Cycle *		Ratio of high pulse width (as measured from rising edge to next falling edge at $V_{DD}/2$) to one clock period	45		55	%
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to next rising edge at $V_{DD}/2$, C_L = 10pF		300		ps
Jitter, Long Term ($\sigma_y(\tau)$) *	$t_{j(LT)}$	From 0-500µs at $V_{DD}/2$, C_L = 10pF compared to ideal clock source		150		ps
Rise Time *	t_r	V_{DD} = 5V; V_{DDO} = 3.3V; V_O = 0.3V to 3.0V; C_L = 10pF		1.8		ns
Fall Time *	t_f	V_{DD} = 5V; V_{DDO} = 3.3V; V_O = 0.3V to 3.0V; C_L = 10pF		1.4		ns
Rise Time *	t_r	V_{DD} = 5V; V_{DDO} = 5.0V; V_O = 0.5V to 4.5V; C_L = 10pF		1.4		ns
Fall Time *	t_f	V_{DD} = 5V; V_{DDO} = 5.0V; V_O = 4.5V to 0.5V; C_L = 10pF		1.25		ns

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5.0 Package Information

Table 7: 20-pin SOIC (0.300") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.0926	0.1043	2.35	2.65
A_1	0.004	0.0118	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.0091	0.0125	0.23	0.32
D	0.4961	0.5118	12.60	13.00
E	0.2914	0.2992	7.40	7.60
e	0.05 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
h	0.010	0.029	0.25	0.75
L	0.016	0.050	0.40	1.27
Θ	0°	8°	0°	8°

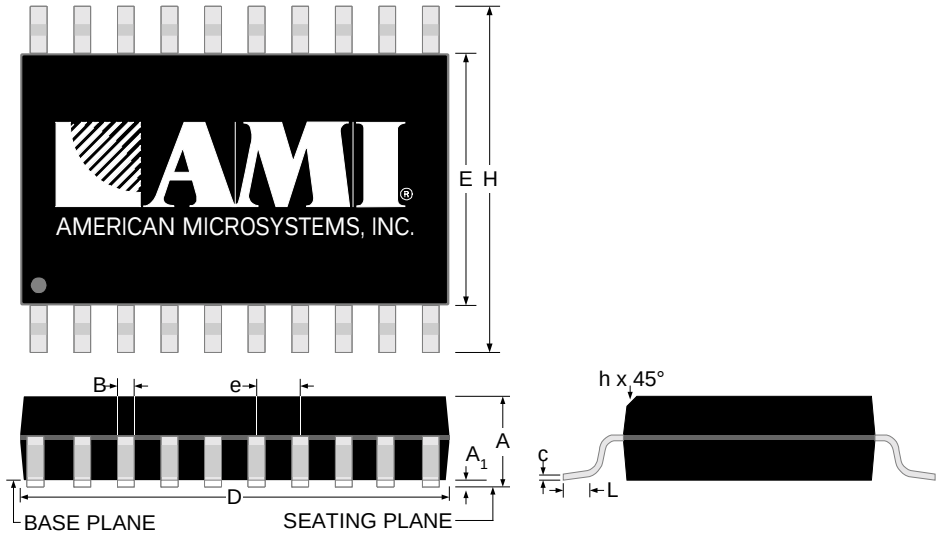

Table 8: 20-pin SOIC (0.300") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	80	°C/W
Lead Inductance, Self	L_{11}	Center lead	2.5	nH
Lead Inductance, Mutual	L_{12}	Center lead to any adjacent lead	0.85	nH
Lead Capacitance, Bulk	C_{11}	Center lead to V_{SS}	0.42	pF
Lead Capacitance, Mutual	C_{12}	Center lead to any adjacent lead	0.08	pF

6.0 Ordering Information

ORDERING CODE	DEVICE NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
11640-223	FS6245-01	20-pin (0.300") SOIC (Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel

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