

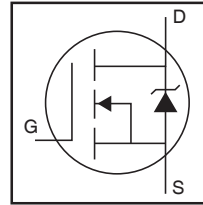
HEXFET® Power MOSFET

**Applications**

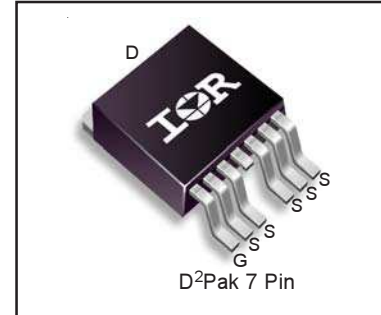
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

**Benefits**

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



$V_{DSS}$		<b>24V</b>
$R_{DS(on)}$	typ.	<b>0.8mΩ</b>
	max.	<b>1.0mΩ</b>
$I_D$ (Silicon Limited)		<b>429A</b> ①
$I_D$ (Package Limited)		<b>240A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF1324S-7PPbF	D²Pak-7Pin	Tube	50	IRF1324S-7PPbF
		Tape and Reel Left	800	IRF1324STRL-7PP

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	429①	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	303①	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	240	
$I_{DM}$	Pulsed Drain Current ②	1640	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ③	1.6	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	230	mJ
$I_{AR}$	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
$E_{AR}$	Repetitive Avalanche Energy ⑤		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥	—	0.50	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D²Pak ⑧	—	40	

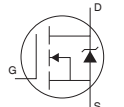
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	24	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.023	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5mA <sup>②</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	0.80	1.0	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 160A <sup>③</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 19V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -20V
R <sub>G</sub>	Internal Gate Resistance	—	3.0	—	Ω	

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

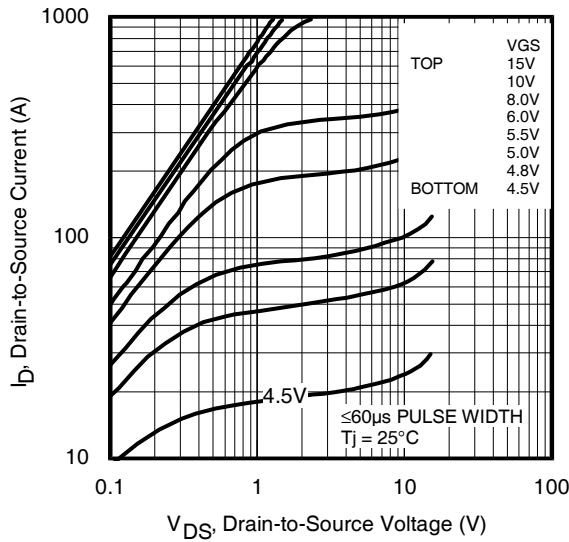
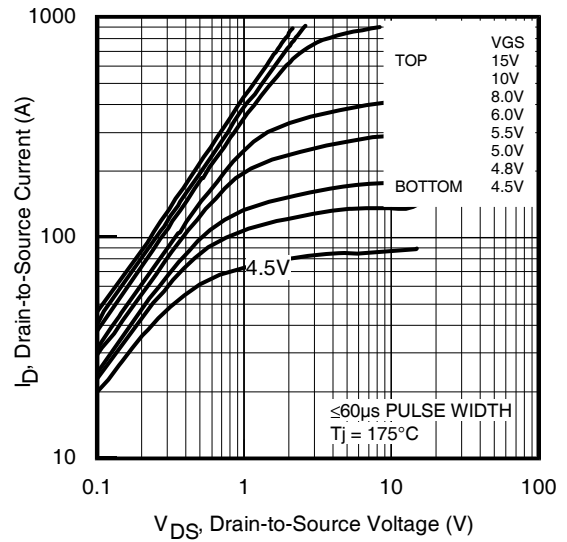
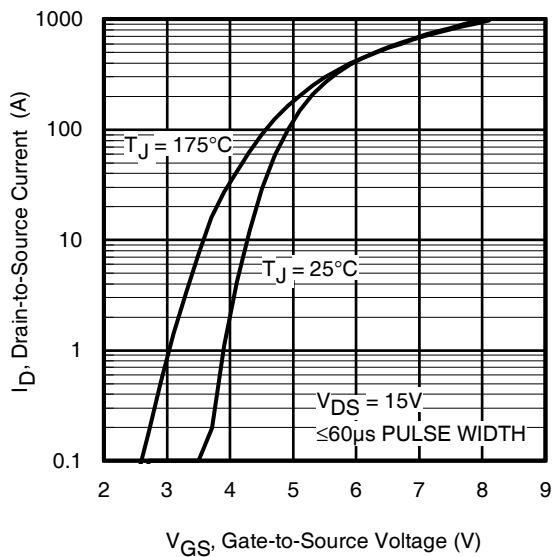
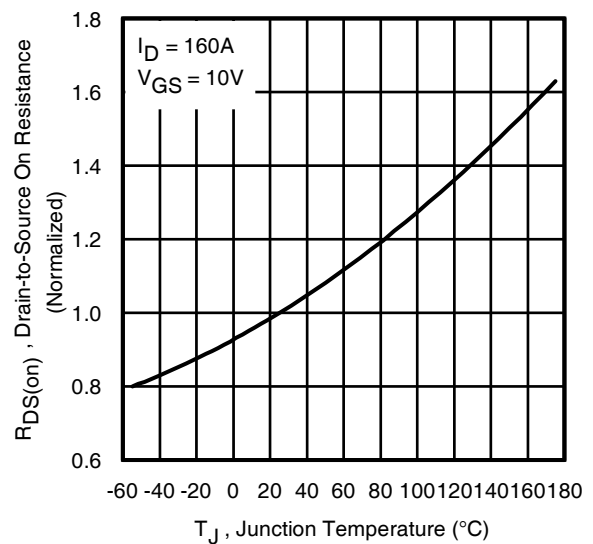
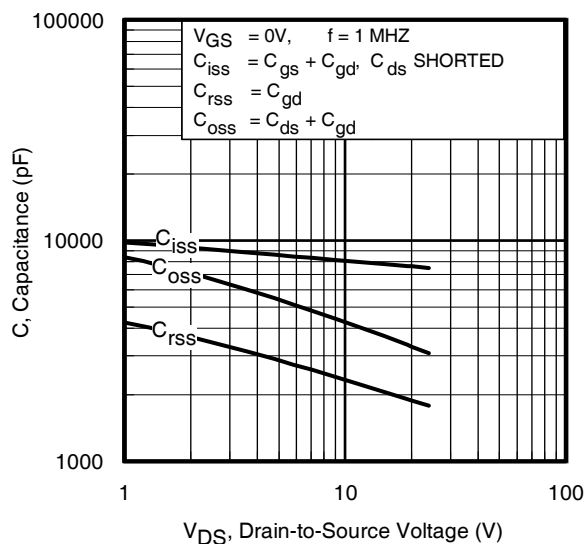
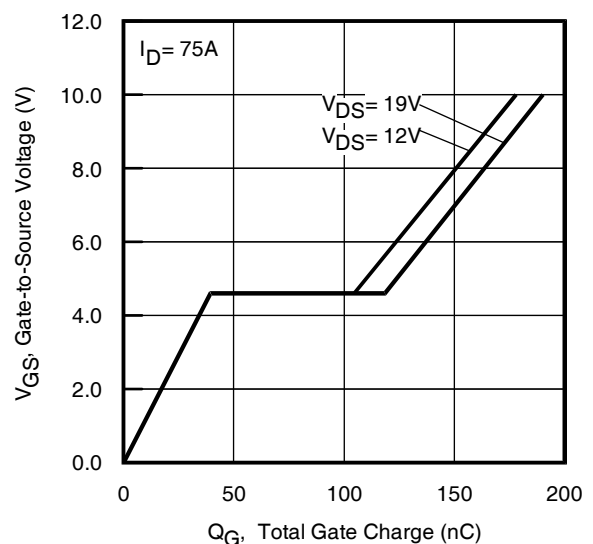
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	270	—	—	S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 160A
Q <sub>g</sub>	Total Gate Charge	—	180	252	nC	I <sub>D</sub> = 75A
Q <sub>gs</sub>	Gate-to-Source Charge	—	47	—		V <sub>DS</sub> = 12V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	58	—		V <sub>GS</sub> = 10V <sup>⑤</sup>
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	122	—		I <sub>D</sub> = 75A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V <sup>⑤</sup>
t <sub>d(on)</sub>	Turn-On Delay Time	—	19	—	ns	V <sub>DD</sub> = 16V
t <sub>r</sub>	Rise Time	—	240	—		I <sub>D</sub> = 160A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	86	—		R <sub>G</sub> = 2.7Ω
t <sub>f</sub>	Fall Time	—	93	—		V <sub>GS</sub> = 10V <sup>⑤</sup>
C <sub>iss</sub>	Input Capacitance	—	7700	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	3380	—		V <sub>DS</sub> = 19V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	1930	—		f = 1.0MHz, See Fig.5
C <sub>oss</sub> eff. (ER)	Effective Output Capacitance (Energy Related)	—	4780	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 19V <sup>⑦</sup> , See Fig.11
C <sub>oss</sub> eff. (TR)	Effective Output Capacitance (Time Related) <sup>⑥</sup>	—	4970	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 19V <sup>⑥</sup>

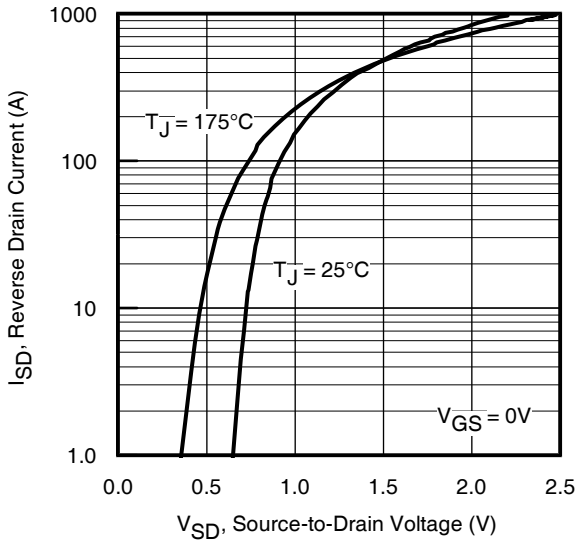
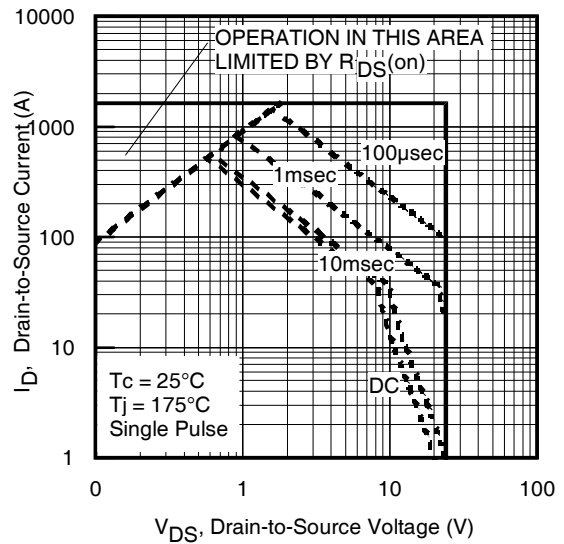
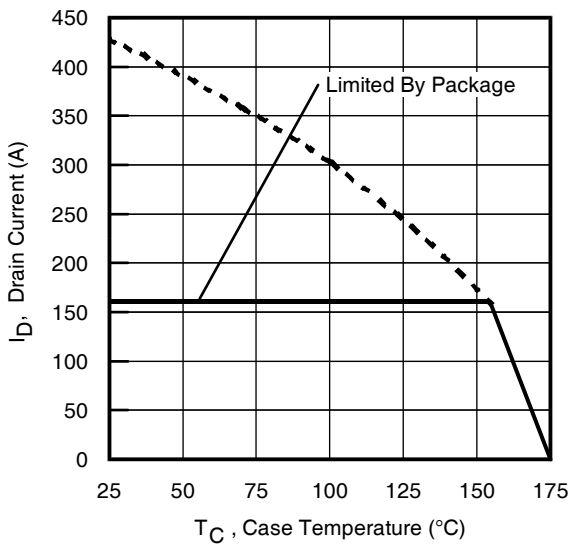
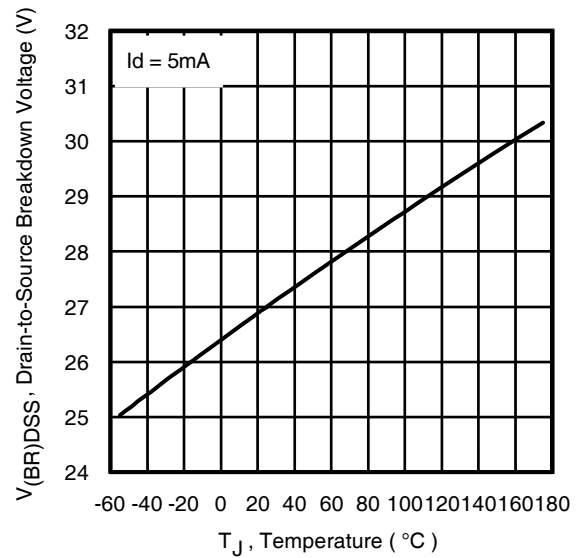
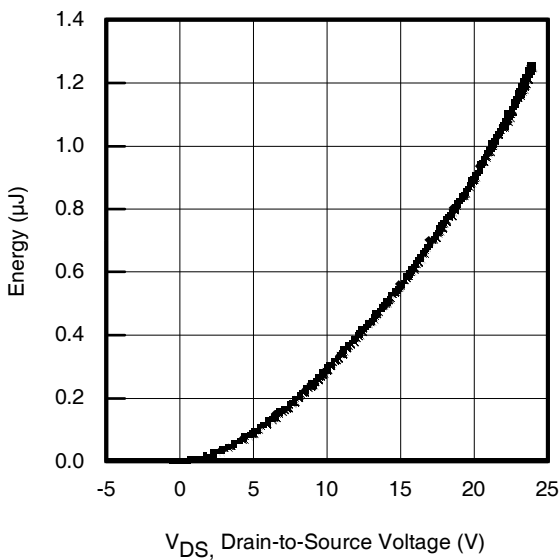
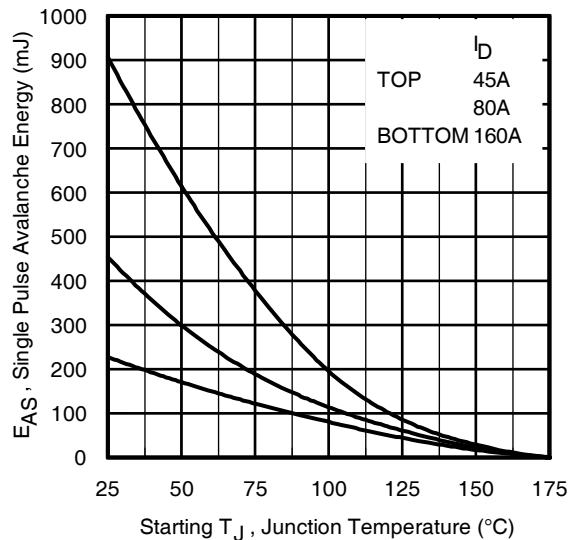
**Diode Characteristics**

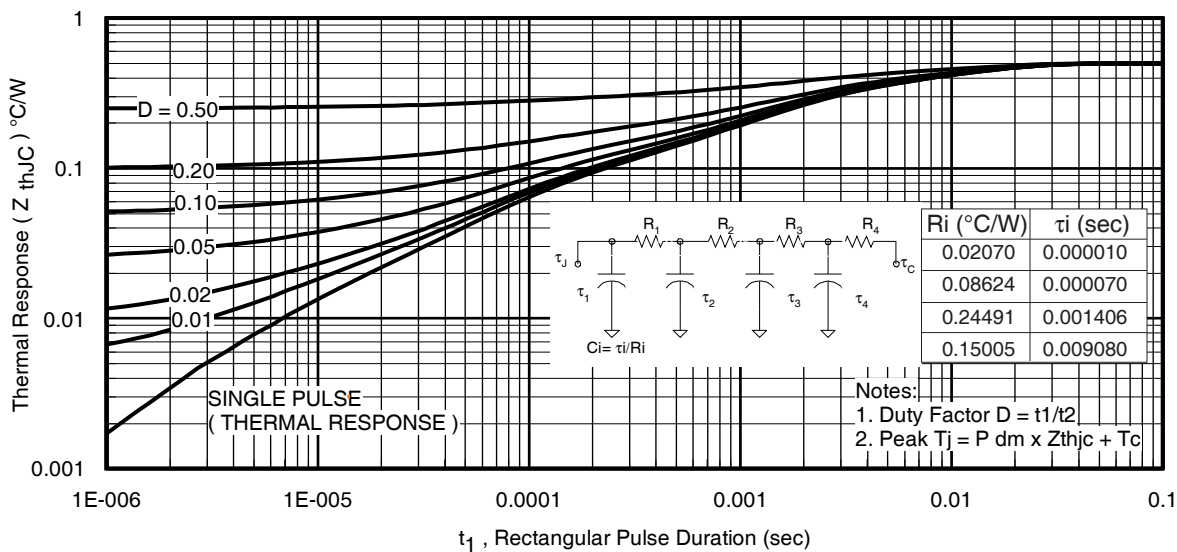
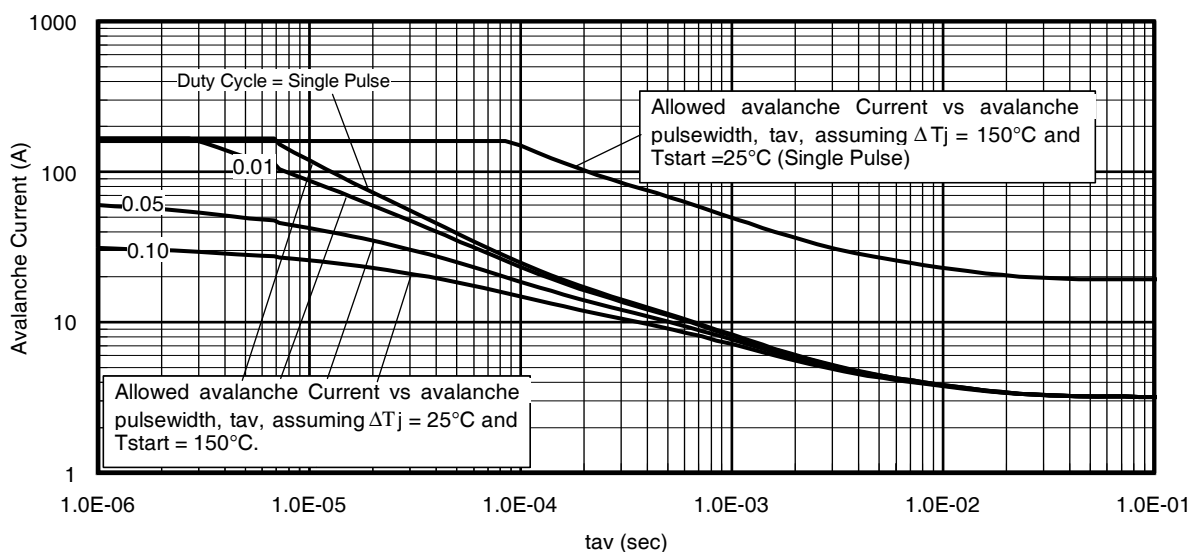
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	429 <sup>①</sup>	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>②</sup>	—	—	1636	A	
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 160A, V <sub>GS</sub> = 0V <sup>③</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	71	107	ns	T <sub>J</sub> = 25°C V <sub>R</sub> = 20V,
		—	74	110		T <sub>J</sub> = 125°C I <sub>F</sub> = 160A
Q <sub>rr</sub>	Reverse Recovery Charge	—	83	120	nC	T <sub>J</sub> = 25°C di/dt = 100A/μs <sup>⑤</sup>
		—	92	140		T <sub>J</sub> = 125°C
I <sub>R<sub>RM</sub></sub>	Reverse Recovery Current	—	2.0	—	A	T <sub>J</sub> = 25°C
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

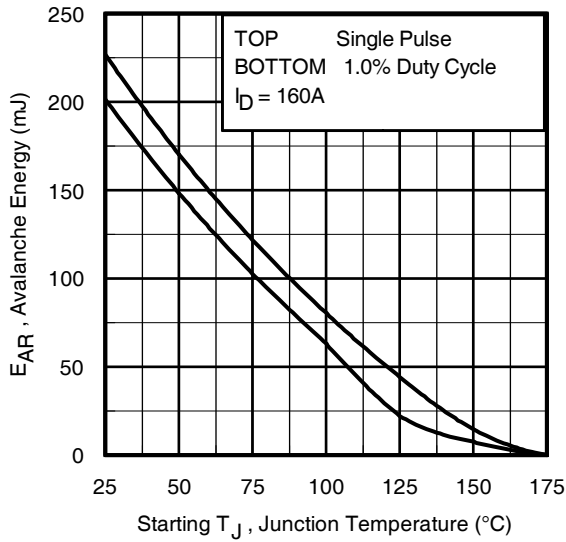
**Notes:**

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140 <http://www.irf.com/technical-info/appnotes/an-1140.pdf>)
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T<sub>Jmax</sub>, starting T<sub>J</sub> = 25°C, L = 0.018mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 160A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ④ I<sub>SD</sub> ≤ 160A, di/dt ≤ 600A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑥ C<sub>oss</sub> eff. (TR) is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑦ C<sub>oss</sub> eff. (ER) is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R<sub>θ</sub> is measured at T<sub>J</sub> approximately 90°C


**Fig 1. Typical Output Characteristics**

**Fig 2. Typical Output Characteristics**

**Fig 3. Typical Transfer Characteristics**

**Fig 4. Normalized On-Resistance vs. Temperature**

**Fig 5. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 7. Typical Source-Drain Diode Forward Voltage**

**Fig 8. Maximum Safe Operating Area**

**Fig 9. Maximum Drain Current vs. Case Temperature**

**Fig 10. Drain-to-Source Breakdown Voltage**

**Fig 11. Typical C<sub>OSS</sub> Stored Energy**

**Fig 12. Maximum Avalanche Energy vs. Drain Current**


**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

**Fig 14.** Typical Avalanche Current vs. Pulsewidth

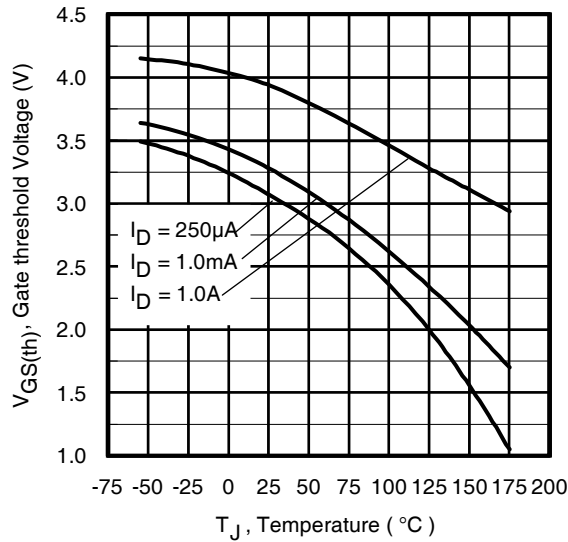

**Notes on Repetitive Avalanche Curves , Figures 14, 15:  
(For further info, see AN-1005 at www.irf.com)**

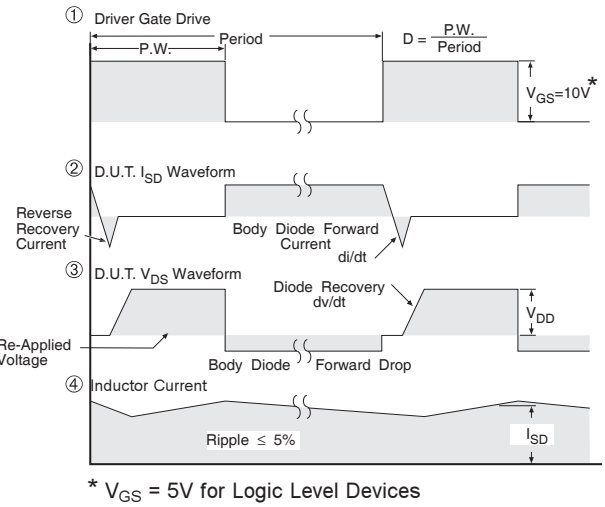
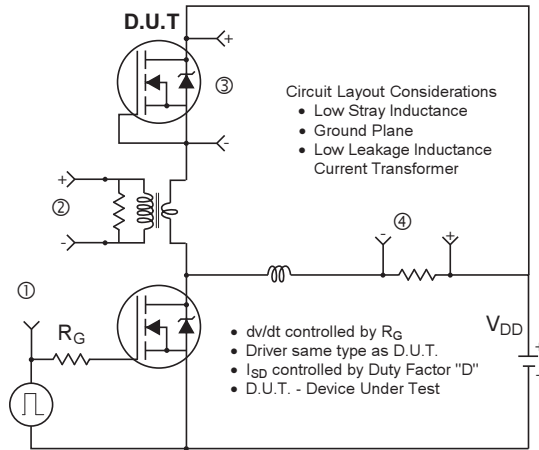
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

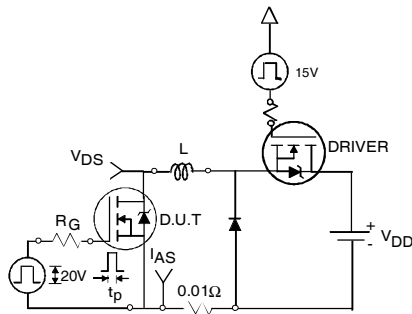
$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

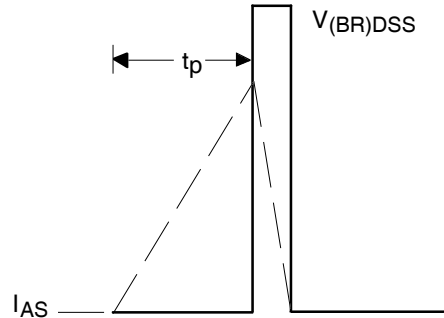
**Fig 15. Maximum Avalanche Energy vs. Temperature**

**Fig 16. Threshold Voltage Vs. Temperature**



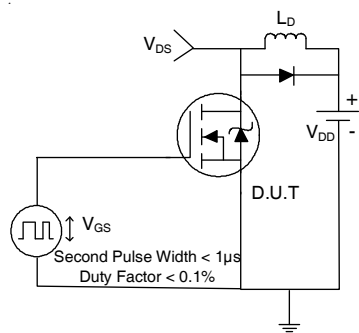
**Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**



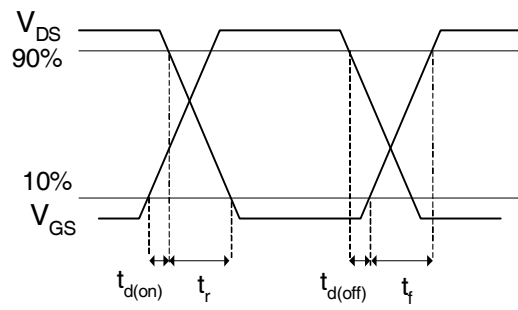
**Fig 22a. Unclamped Inductive Test Circuit**



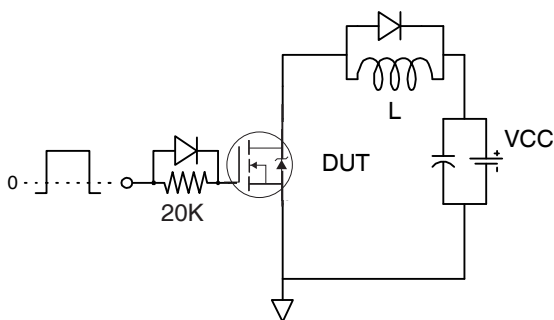
**Fig 22b. Unclamped Inductive Waveforms**



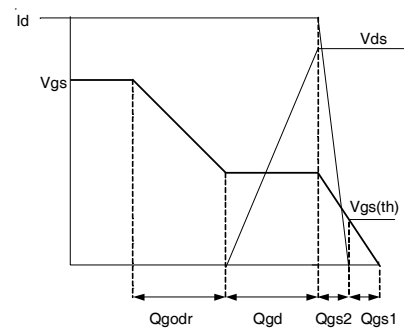
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



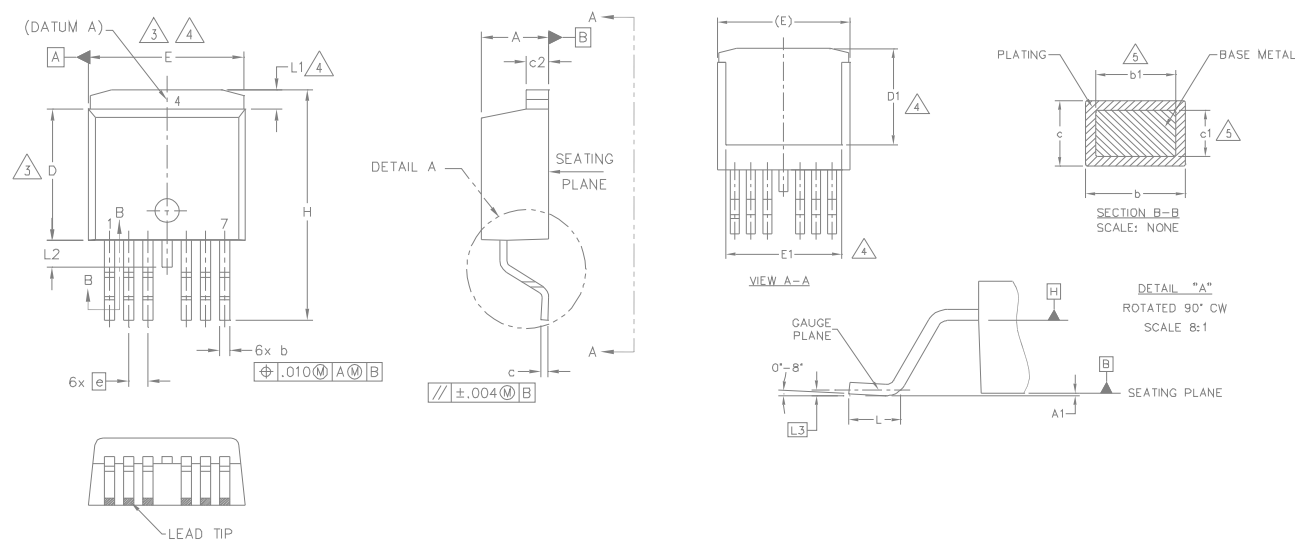
**Fig 24a. Gate Charge Test Circuit**



**Fig 24b. Gate Charge Waveform**

## D<sup>2</sup>Pak - 7 Pin Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	—	0.254	—	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	7.42	.270	.292	4
E	9.65	10.54	.380	.415	3,4
E1	6.22	8.48	.245	.334	4
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	4
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

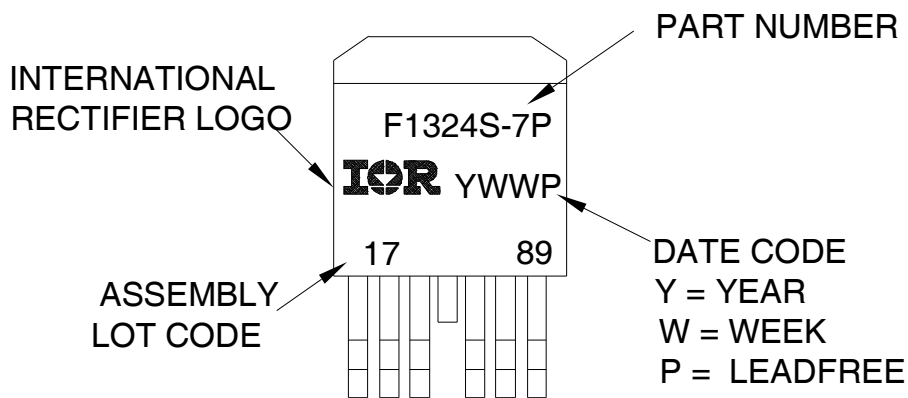
NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB. EXCEPT FOR DIMS. E, E1 & D1.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>



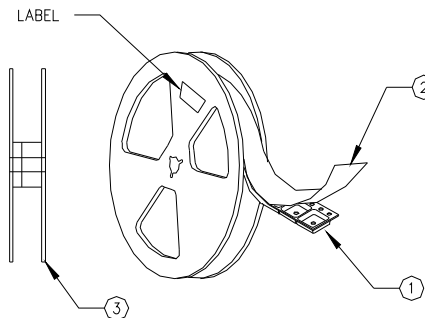
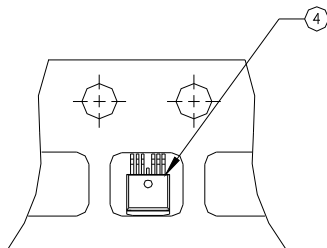
## D<sup>2</sup>Pak - 7 Pin Part Marking Information



## D<sup>2</sup>Pak - 7 Pin Tape and Reel

### NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
  - 1.1 REEL SIZE 13 INCH DIAMETER.
  - 1.2 EACH REEL CONTAINING 800 DEVICES.
  - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
  - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
  - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
  - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.
2. LABELLING (REEL AND SHIPPING BAG).
  - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
  - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
  - 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
  - 2.4 QUANTITY:
  - 2.5 VENDOR CODE: IR
  - 2.6 LOT CODE:
  - 2.7 DATE CODE:



**Note:** For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification information<sup>†</sup>**

Qualification level	Industrial <sup>††</sup>	
	(per JEDEC JESD47F <sup>†††</sup> guidelines)	
Moisture Sensitivity Level	D <sup>2</sup> Pak-7PIN	MSL1
		(per JEDEC J-STD-020D <sup>††</sup> )
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
4/8/2014	<ul style="list-style-type: none"> <li>• Added Ordering information table on page 1</li> <li>• Updated package outline on page 8</li> <li>• Updated part marking on page 9</li> <li>• Added Qualification table on page 10.</li> <li>• Updated data sheet with new IR corporate template</li> </ul>