ARM® Cortex®-M

32-bit Microcontroller

NuMicro™ Family
Nano100(A) Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

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1 GENERAL DESCRIPTION

The Nano100 series ultra-low power 32-bit microcontroller is embedded with ARM® Cortex™-M0 core operated at a wide voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 32K/64K-byte embedded Flash and 8K/16K-byte embedded SRAM. Integrating USB 2.0 full-speed function, RTC, 12-bit SAR ADC, and provides high performance connectivity peripheral interfaces such as UART, SPI, I2C, I2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and ISO-7816-3 for Smart card, the Nano100 series supports Brown-Out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano100 series provides low power voltage, low power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and lowest cost 32-bit microcontrollers. The Nano100 series is suitable for a wide range of battery device applications such as:

- Portable Data Collector
- Portable Medical Monitor
- Portable RFID Reader
- Portable Barcode Scanner
- Security Alarm System
- System Supervisors
- Power Metering
- USB Accessories
- Smart Card Reader
- Wireless Game Control Device
- IPTV Remote Smart Keyboard
- Wireless Sensors Node Device (WSN)
- Wireless RF4CE Remote Control
- Wireless Audio
- Wireless Automatic Meter Reader (AMR)
- Electronic Toll Collection(ETC)

The Nano100 Base line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 32K/64K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates RTC, 8- channels 12-bit SAR ADC, and provides high performance connectivity peripheral interfaces such as 2xUART, 3xSPI, 2xI2C, I2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 2xISO-7816-3 for Smart card. The Nano100 Base line supports Brown-Out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano120 USB Connectivity line, an ultra-low power 32-bit microcontroller with the embedded ARM® Cortex™-M0 core, operates at wide voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 32K/64K bytes embedded flash and 8K/16K bytes embedded SRAM. It integrates USB 2.0 full-speed device function, RTC, 8-channels 12-bit SAR ADC, and provides high performance connectivity peripheral interfaces such as 2xUART, 3xSPI, 2xI2C, I2S, GPIOs, EBI (External Bus Interface) for external memory-mapped device access and 2xISO-7816-3 for Smart card. The Nano120 USB Connectivity line supports Brown-Out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

Product Line	UART	SPI	I2C	I2S	USB	ADC	RTC	EBI	SC	Timer
Nano100	•	•	•	•		•	•	•	•	•
Nano120	•	•	•	•	•	•	•	•	•	•

Table 1-1 Connectivity Support Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 Nano100 Features – Base Line

- Core
  - ARM® Cortex™-M0 core running up to 32 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
  - Runs up to 32 MHz with zero wait state for discontinuous address read access
  - 64K/32K bytes application program memory (APROM)
  - 4 KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
  - 16K/8K bytes embedded SRAM
  - Supports DMA mode
- DMA: Supports 5 channels: one VDMA channel and 4 PDMA channels
  - VDMA
    - Memory-to-memory transfer
    - Supports block transfer with stride
    - Supports word/half-word/byte boundary address
    - Supports address direction: increment and decrement
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around

- Clock Control
  - Flexible selection for different applications
  - Built-in 12 MHz OSC (Trimmed to 1%) for system operation, and low power 10 kHz OSC for watchdog and wake-up idle operation
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 96 MHz, for high performance system operation (32 MHz) and USB application (48 MHz).
  - External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance (except ADC shared pins PC.6 and PC.7)
- Timer
  - Supports 4 sets of 32-bit timers, each with 24-bit up-counting timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot, output toggle and periodic operation modes
  - Internal trigger event to ADC module
  - Supports PDMA mode
  - Timer can wake system up from power down or idle mode
- Watchdog Timer
  - Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable when watchdog time-out
  - Wake system up from Power-down or Idle mode
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode

- Automatic leap year recognition
- Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Wake system up from Power-down or Idle mode
- Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers

- PWM/Capture
  - Supports 2 PWM modules, each has two 16-bit PWM generators
  - Provides eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
  - Up to eight 16-bit digital Capture timers (shared with PWM timers), and provides eight capture inputs (rising, falling, or both)
  - Supports One-shot and Continuous mode
  - Supports Capture interrupt
- UART
  - Up to two 16-byte FIFO UART controllers
  - UART ports with flow control (TX, RX, CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Supports LIN function
  - Supports RS-485 9 bit mode and direction control.
  - Programmable baud rate generator
  - Supports PDMA mode
  - Wake system up from Power-down or Idle mode
- SPI
  - Up to three sets of SPI controller
  - Master up to 16 MHz, and Slave up to 6 MHz
  - Supports SPI/MICROWIRE Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 4 to 32 bits
  - MSB or LSB first data transfer
  - RX and TX on both rising or falling edge of serial clock independently
  - Two slave/device select lines when SPI controller is used as the master, and 1 slave/device select line when SPI controller is used as the slave
  - Supports byte suspend mode in 32-bit transmission
  - Supports two channel PDMA requests, one for transmit and another for receive
  - Supports three wire mode, no slave select signal, bi-direction interface
  - Wake system up from Power-down or Idle mode

- I2C
  - Up to two sets of I2C device
  - Master/Slave up to 1 Mbit/s
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
  - Programmable clocks allowing for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
- I2S
  - Interface with external audio CODEC
  - Operated as either Master or Slave mode
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Supports Mono and stereo audio data
  - Supports I2S and MSB justified data format
  - Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two PDMA requests: one for transmitting and the other for receiving
- ADC
  - 12-bit SAR ADC
  - Up to 8-ch single-ended input from external pin
  - One internal channel from AVDD, AVSS, Temp sensor, and internal reference voltage
  - Supports Single Scan, Single Cycle Scan, and Continuous Scan mode
  - Each channel with individual result register
  - Only scan on enabled channels
  - Threshold voltage detection (comparator function)
  - Conversion started by software programming or external input
  - Supports PDMA mode
  - Supports up to four timer time-out events (TRM0_CH0, TMR0_CH1, TMR1_CH0

and TMR1_CH1) to enable ADC

- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separates receive/transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8 bit time out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
- EBI (External bus interface) support
  - Accessible space: 64 KB in 8-bit mode or 128 KB in 16-bit mode
  - Supports 8bit/16bit data width
  - Supports byte write in 16-bit Data Width mode
- One built-in temperature sensor with 1℃ resolution
- 96-bit unique ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin(14x14) / 64-pin(7x7) / 48-pin(7x7) / QFN 33-pin(5x5)

2.2 Nano120 Features – USB Connectivity Line

- Core
  - ARM® Cortex™-M0 core running up to 32 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- Flash EPROM Memory
  - Runs up to 32 MHz with zero wait state for discontinuous address read access.
  - 64K/32K bytes application program memory (APROM)
  - 4KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
  - 16K/8K bytes embedded SRAM
  - Support PDMA mode
- DMA: Support 5 channels: one VDMA channel and 4 PDMA channels
  - VDMA
    - Memory-to-memory transfer
    - Support block transfer with stride
    - Support word/half-word/byte boundary address
    - Support address direction: increment and decrement
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Support word boundary address
    - Support word alignment transfer length in memory-to-memory mode
    - Support word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Support word/half-word/byte transfer data width from/to peripheral
    - Support address: increment, fixed, and wrap around
- Clock Control
  - Flexible selection for different applications

- Built-in 12MHz OSC (Trimmed to 1%) for system operation, and low power 10 kHz OSC for watchdog and wake-up operation
- Low power 10 kHz OSC for watchdog and low power system operation
- Support one PLL, up to 96 MHz, for high performance system operation (32MHz) and USB application (48MHz).
- External 4~24 MHz crystal input for precise timing operation
- External 32.768 kHz crystal input for RTC function and low power system operation

- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin can be configured as interrupt source with edge/level setting
  - High driver and high sink IO mode support
  - Support input 5V tolerance (except ADC shared pins PC.6 and PC.7)
- Timer
  - Support 4 sets of 32-bit timers, each with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot, output toggle and periodic operation modes
  - Internal trigger event to ADC module
  - Support PDMA mode
  - Wake system up from Power-down or Idle mode
- Watchdog Timer
  - Clock Source from LIRC. (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable on watchdog time-out
  - Wake system up from Power-down or Idle mode
- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32,

1/16, 1/8, 1/4, 1/2 and 1 second

- Wake system up from Power-down or Idle mode
- Support 80 bytes spare registers and a snoop pin to clear the content of these spare registers

- PWM/Capture
  - Support 2 PWM module, each has two 16-bit PWM generators
  - Provide eight PWM outputs or four complementary paired PWM outputs
  - Each PWM generator equipped with one clock divider, one 8-bit prescaler , two clock selectors, and one Dead-Zone generator for complementary paired PWM
  - Up to eight 16-bit digital Capture timers (shared with PWM timers) provide eight rising/falling capture inputs
  - Support one shot and continuous mode
  - Support Capture interrupt
- UART
  - Up to two 16-byte FIFO UART controllers
  - UART ports with flow control (TX, RX, CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Supports LIN function
  - Supports RS-485 9 bit mode and direction control. (Low Density Only)
  - Programmable baud rate generator
  - Supports PDMA mode
  - Wake system up from Power-down or Idle mode
- SPI
  - Up to three sets of SPI controller
  - Master up to 16 MHz, and Slave up to 6 MHz
  - Supports SPI/MICROWIRE Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 4 to 32 bits
  - MSB or LSB first data transfer
  - RX and TX on both rising or falling edge of serial clock independently
  - Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
  - Supports byte suspend mode in 32-bit transmission
  - Supports two channel PDMA requests, one for transmit and another for receive
  - Supports three wire, no slave select signal, bi-direction interface
  - Wake system up from Power-down or Idle mode
- I2C
    - Up to two sets of I2C device

- Master/Slave up to 1Mbit/s
- Bi-directional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
- Programmable clocks allow versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave addresses with mask option)

- I2S
  - Interface with external audio CODEC
  - Operated as either Master or Slave mode
  - Capable of handling 8, 16, 24 and 32 bit word sizes
  - Supports Mono and stereo audio data
  - Supports I2S and MSB justified data format
  - Provides two 8 word FIFO data buffers: one for transmitting and the other for receiving
  - Generates interrupt requests when buffer levels cross a programmable boundary
  - Supports two PDMA requests: one for transmitting and the other for receiving
- ADC
  - 12-bit SAR ADC with 800K SPS
  - Up to 8-ch single-end input from external pin.
  - One internal channel from AVDD, AVSS, Temp sensor, and internal reference voltage.
  - Supports single scan, single cycle scan, and continuous scan modes
  - Each channel with individual result register
  - Only scan on enabled channels
  - Threshold voltage detection (comparator function)
  - Conversion start by software programming or external input
  - Supports PDMA mode
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2, TMR3) to enable ADC
- SmartCard (SC)

- Compliant to ISO-7816-3 T=0, T=1
- Supports up to two ISO-7816-3 ports
- Separates receive / transmit 4 bytes entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- A 24-bit and two 8 bit time out counter for Answer to Request (ATR) and waiting times processing
- Supports auto inverse convention function
- Supports transmitter and receiver error retry and error limit function
- Supports hardware activation sequence process
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detect the card is removal

- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12Mbps
  - On-chip USB Transceiver
  - Provides 1 interrupt source with 4 interrupt events
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provide 6 programmable endpoints
  - Include 512 Bytes internal SRAM as USB buffer
  - Provide remote wake-up capability
- One built-in temperature sensor with 1℃ resolution
- 96-bit unique ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin(14x14) / 64-pin(7x7) / 48-pin(7x7) / QFN 33-pin(5x5)

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ Nano100 Series Selection Code

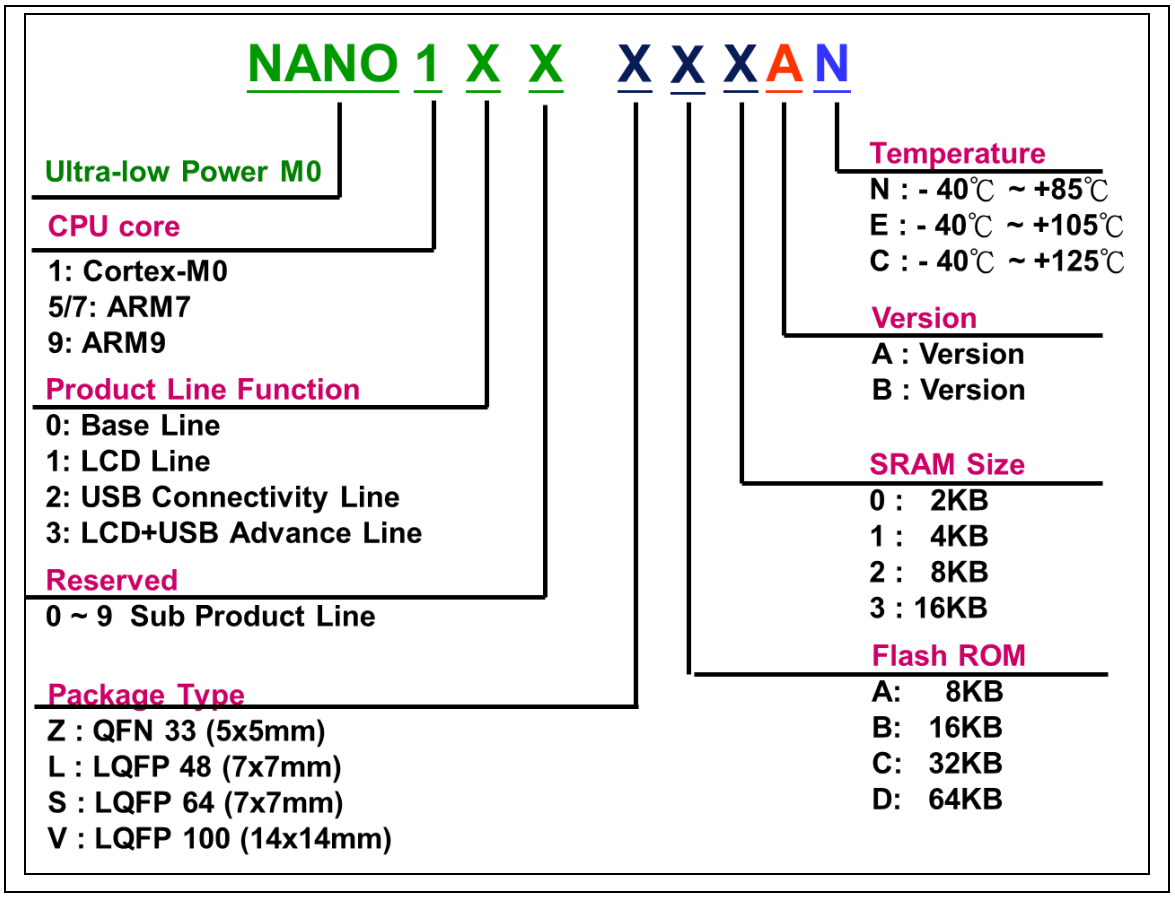


Figure 3-1 NuMicro™ Nano100 Series Selection Code

3.2 NuMicro™ Nano100 Products Selection Guide

3.2.1 NuMicro™ Nano100 Base Line Selection Guide

Part No.	Flash (Kbytes)	SRAM (Kbytes)	Data Flash	ISP ROM (Kbytes)	I/O	Timer (32-bit)	Connectivity				I²S	PWM	12-bit ADC	RTC	EBI	IRC 10KHz 12MHz	PDMA	ISO-7816-3	ICP ISP IAP	Package
							UART	SPI	I²C	USB										
NANO100ZC2AN	32K	8K	Configurable	4K	up to 26	4	2	2	2	-	-	2	5	V	-	V	4	-	V	QFN33
NANO100ZD2AN	64K	8K	Configurable	4K	up to 26	4	2	2	2	-	-	2	5	V	-	V	4	-	V	QFN33
NANO100ZD3AN	64K	16K	Configurable	4K	up to 26	4	2	2	2	-	-	2	5	V	-	V	4	-	V	QFN33
NANO100LC2AN	32K	8K	Configurable	4K	up to 37	4	2	3	2	-	1	4	8	V	-	V	4	2	V	LQFP48
NANO100LD2AN	64K	8K	Configurable	4K	up to 37	4	2	3	2	-	1	4	8	V	-	V	4	2	V	LQFP48
NANO100LD3AN	64K	16K	Configurable	4K	up to 37	4	2	3	2	-	1	4	8	V	-	V	4	2	V	LQFP48
NANO100SD2AN	64K	8K	Configurable	4K	up to 51	4	2	3	2	-	1	8	8	V	V	V	4	2	V	LQFP64*
NANO100SD3AN	64K	16K	Configurable	4K	up to 51	4	2	3	2	-	1	8	8	V	V	V	4	2	V	LQFP64*

QFN33: 5x5mm ; LQFP48: 7x7mm ; LQFP64*: 7x7mm

Table 3-1 Nano100 Base Line Selection Table

3.2.2 NuMicro™ Nano120 USB Connectivity Line Selection Guide

Part No.	Flash (Kbytes)	SRAM (Kbytes)	Data Flash	ISP ROM (Kbytes)	I/O	Timer (32-bit)	Connectivity				I²S	PWM	12-bit ADC	RTC	EBI	IRC 10KHz 12MHz	PDMA	ISO-7816-3	ICP ISP IAP	Package
							UART	SPI	I²C	USB										
NANO120ZC2AN	32K	8K	Configurable	4K	up to 22	4	2	2	2	1	-	2	5	-	-	V	4	2	V	QFN33
NANO120ZD2AN	64K	8K	Configurable	4K	up to 22	4	2	2	2	1	-	2	5	-	-	V	4	2	V	QFN33
NANO120ZD3AN	64K	16K	Configurable	4K	up to 22	4	2	2	2	1	-	2	5	-	-	V	4	2	V	QFN33
NANO120LC2AN	32K	8K	Configurable	4K	up to 33	4	2	3	2	1	1	4	8	V	-	V	4	2	V	LQFP48
NANO120LD2AN	64K	8K	Configurable	4K	up to 33	4	2	3	2	1	1	4	8	V	-	V	4	2	V	LQFP48
NANO120LD3AN	64K	16K	Configurable	4K	up to 33	4	2	3	2	1	1	4	8	V	-	V	4	2	V	LQFP48
NANO120SD2AN	64K	8K	Configurable	4K	up to 47	4	2	3	2	1	1	8	8	V	V	V	4	2	V	LQFP64*
NANO120SD3AN	64K	16K	Configurable	4K	up to 47	4	2	3	2	1	1	8	8	V	V	V	4	2	V	LQFP64*

QFN33: 5x5mm ; LQFP48: 7x7mm ; LQFP64*: 7x7mm

Table 3-2 Nano120 USB Connectivity Line Selection Table

3.3 Pin Configuration

3.3.1 NuMicro™ Nano100 Pin Diagram

3.3.1.1 NuMicro™ Nano100 LQFP 100-pin

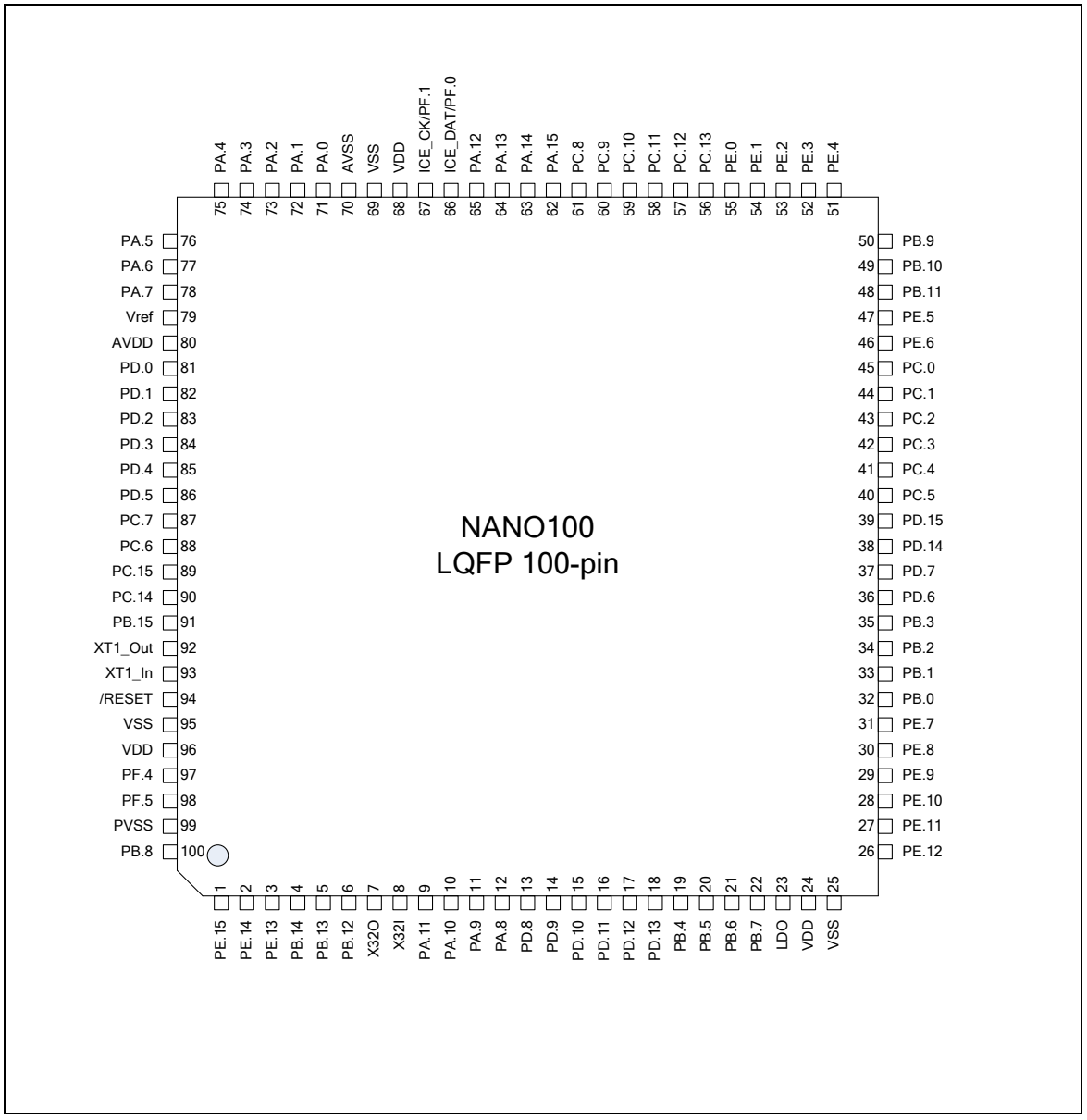


Figure 3-2 NuMicro™ Nano100 LQFP 100-pin Assignment

3.3.1.2 NuMicro™ Nano100 LQFP 64-pin

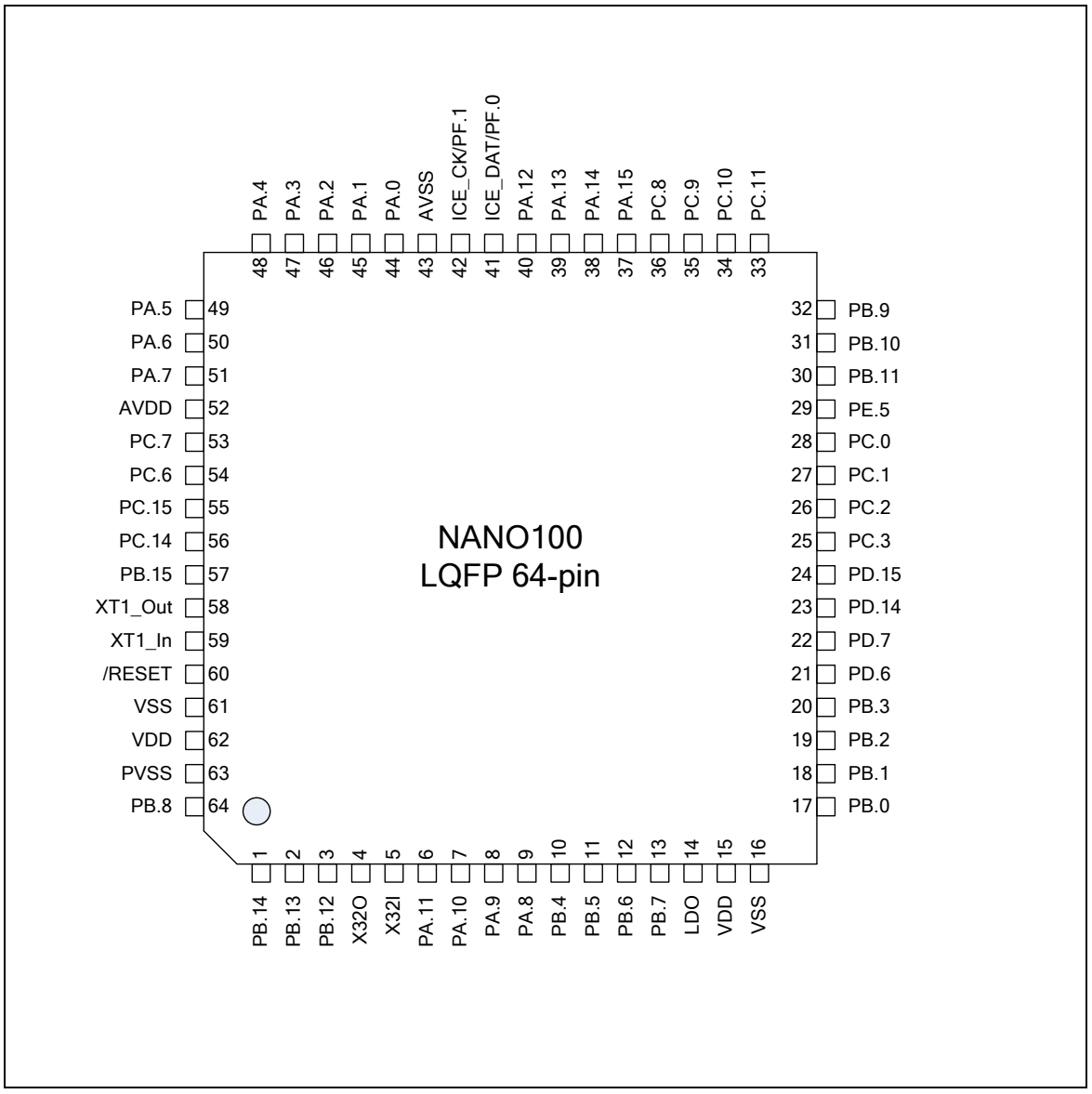


Figure 3-3 NuMicro™ Nano100 LQFP 64-pin Assignment

3.3.1.3 NuMicro™ Nano100 LQFP 48-pin

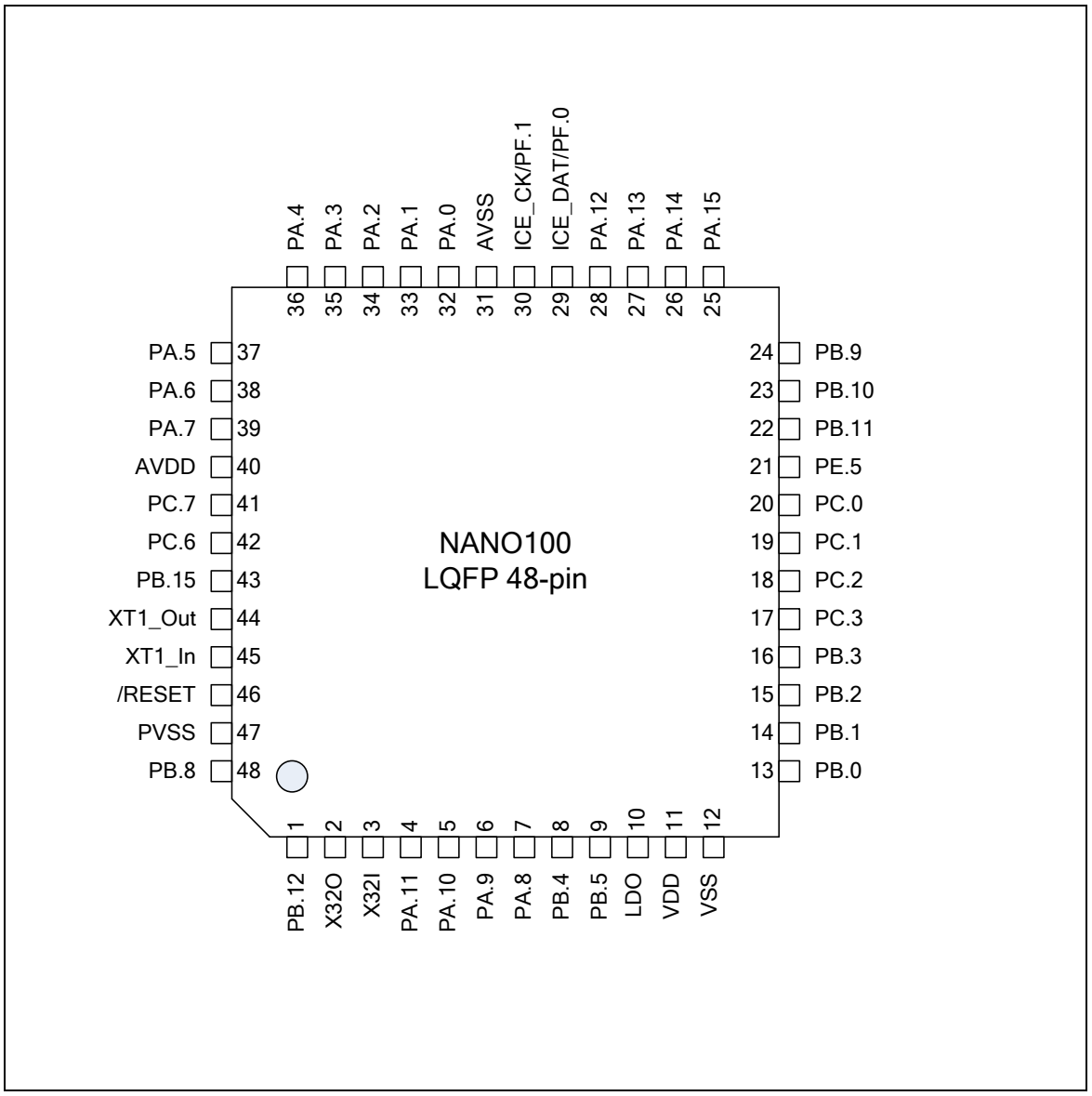


Figure 3-4 NuMicro™ Nano100 LQFP 48-pin Assignment

3.3.1.4 NuMicro™ Nano100 QFN 33-pin

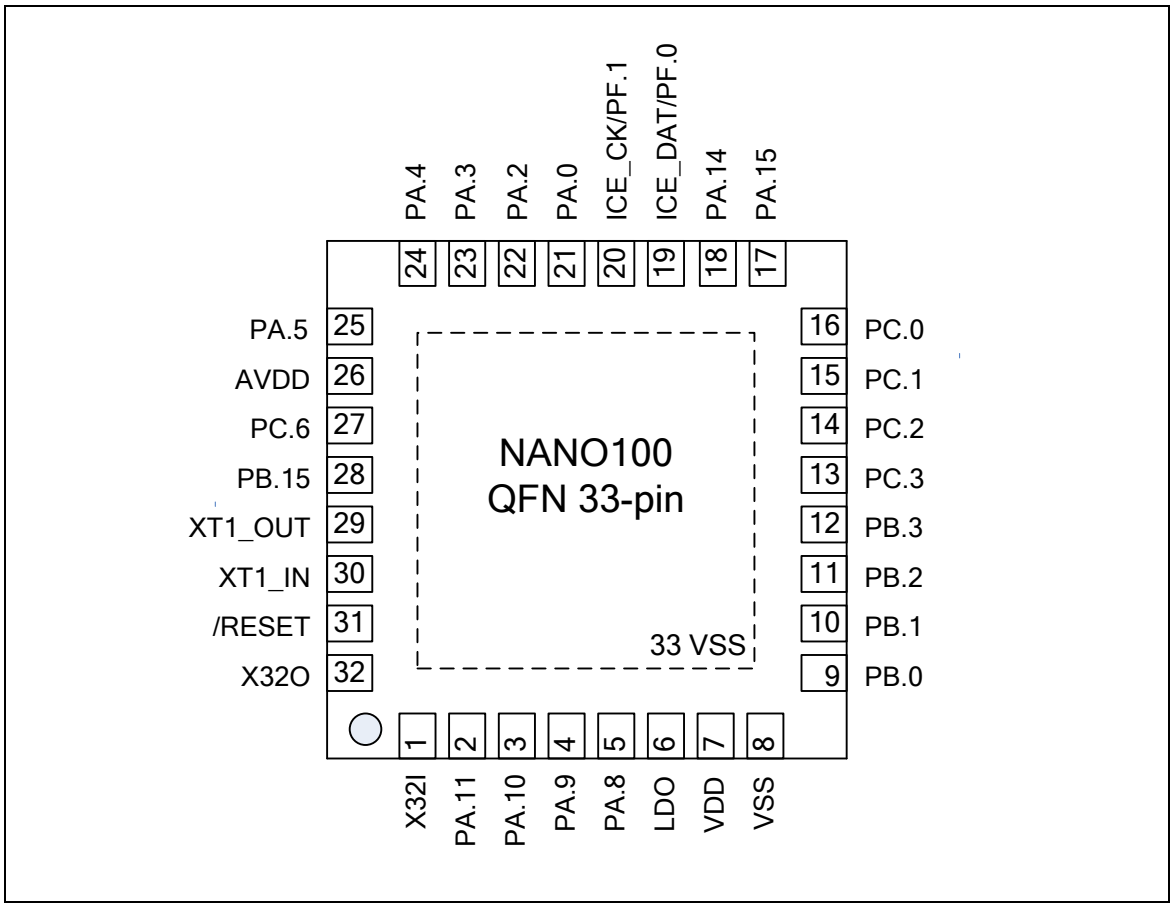


Figure 3-5 NuMicro™ Nano100 QFN 33-pin Assignment

3.3.2 NuMicro™ Nano120 Pin Diagram

3.3.2.1 NuMicro™ Nano120 LQFP 100-pin

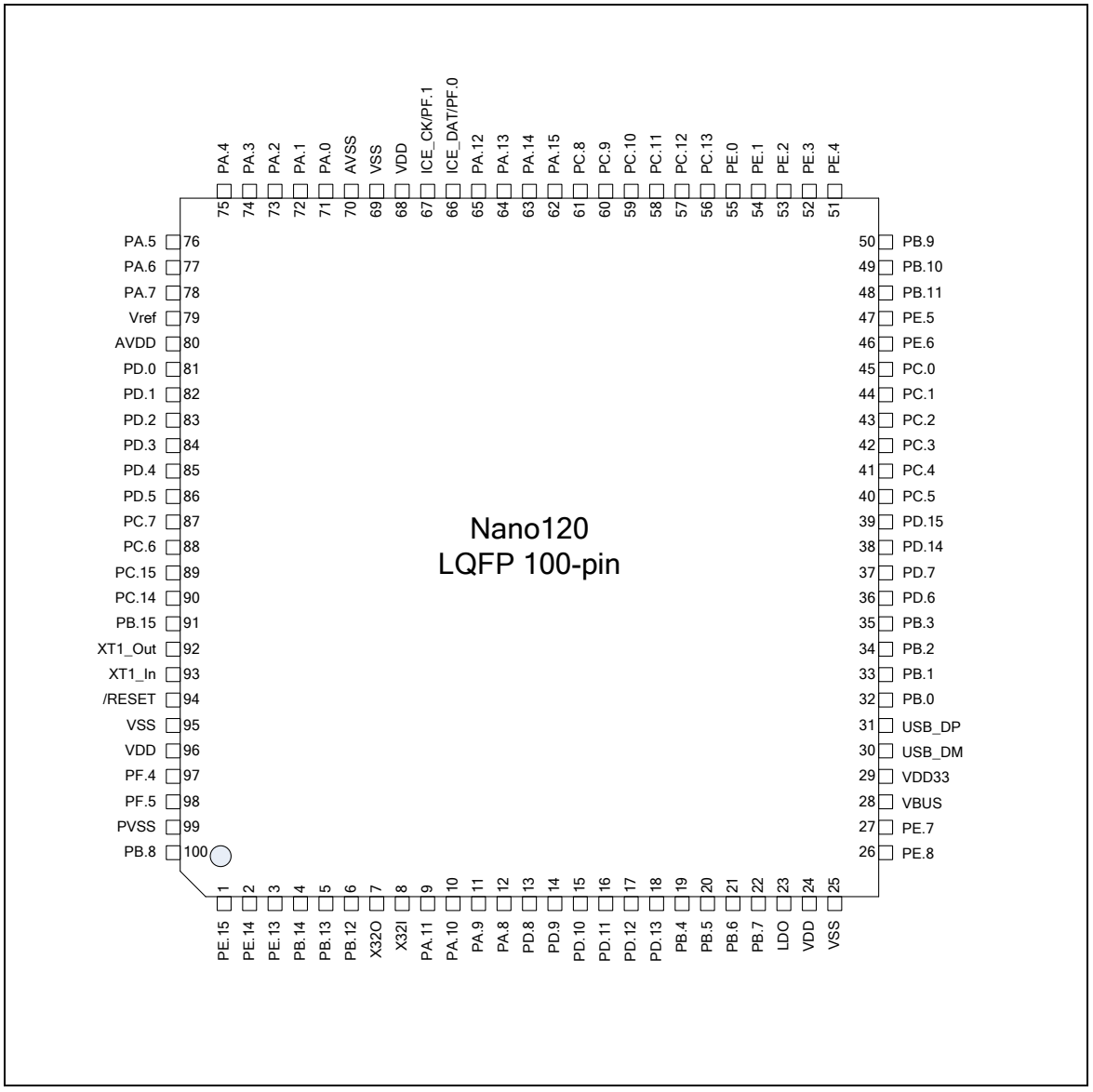


Figure 3-6 NuMicro™ Nano120 LQFP 100-pin Assignment

3.3.2.2 NuMicro™ Nano120 LQFP 64-pin

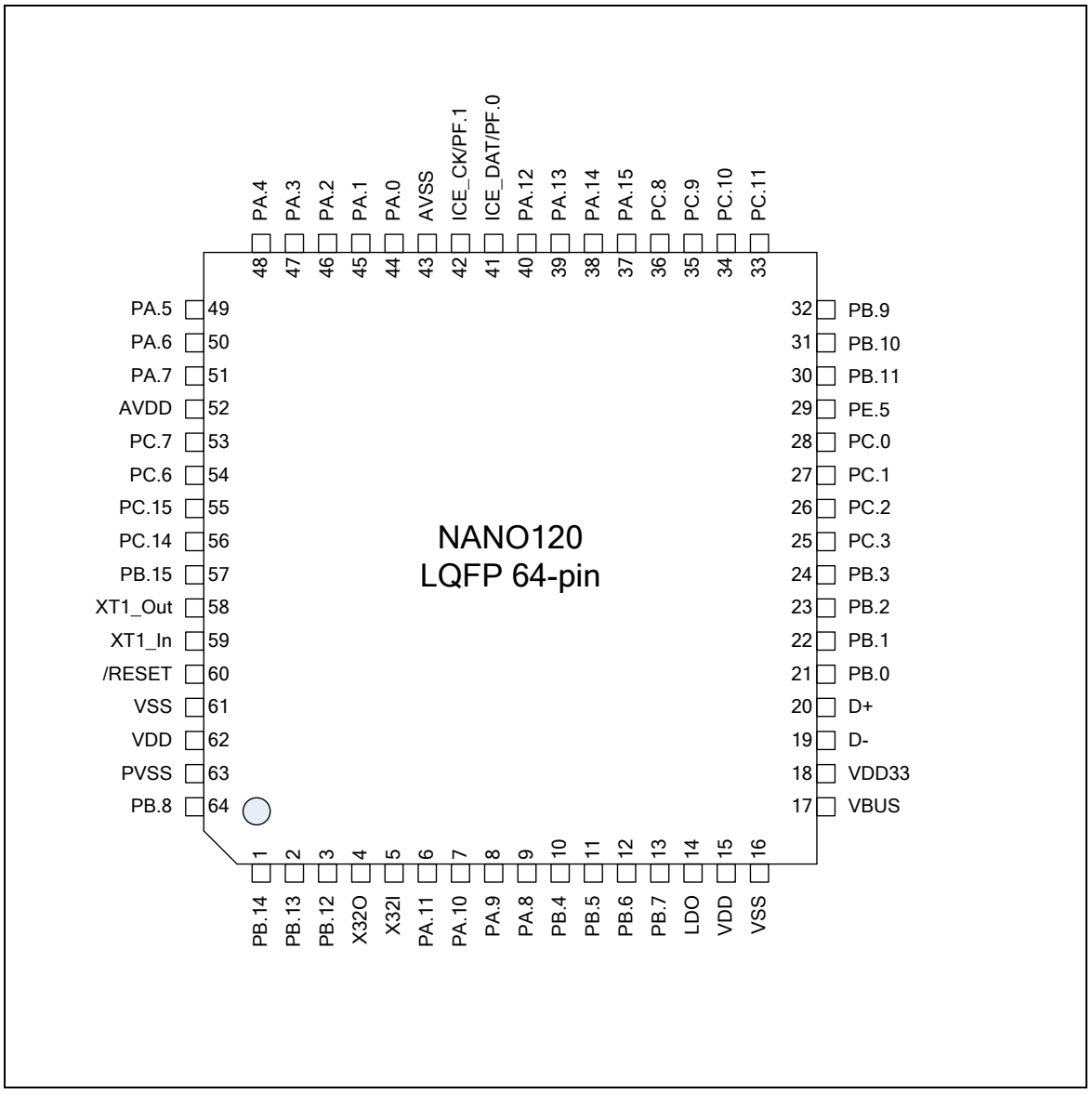


Figure 3-7 NuMicro™ Nano120 LQFP 64-pin Assignment

3.3.2.3 NuMicro™ Nano120 LQFP 48-pin

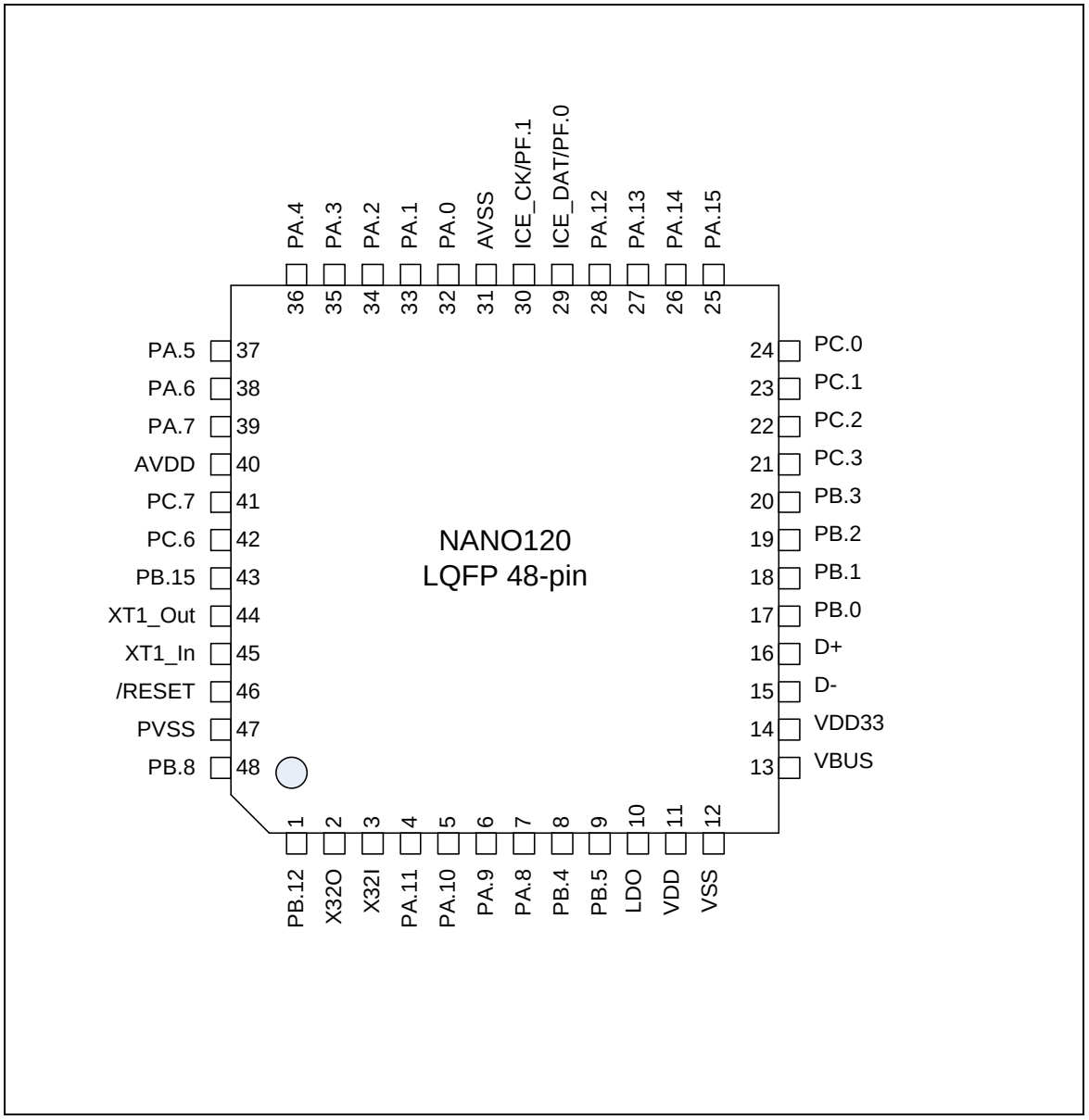


Figure 3-8 NuMicro™ Nano120 LQFP 48-pin Assignment

3.3.2.4 NuMicro™ Nano120 QFN 33-pin

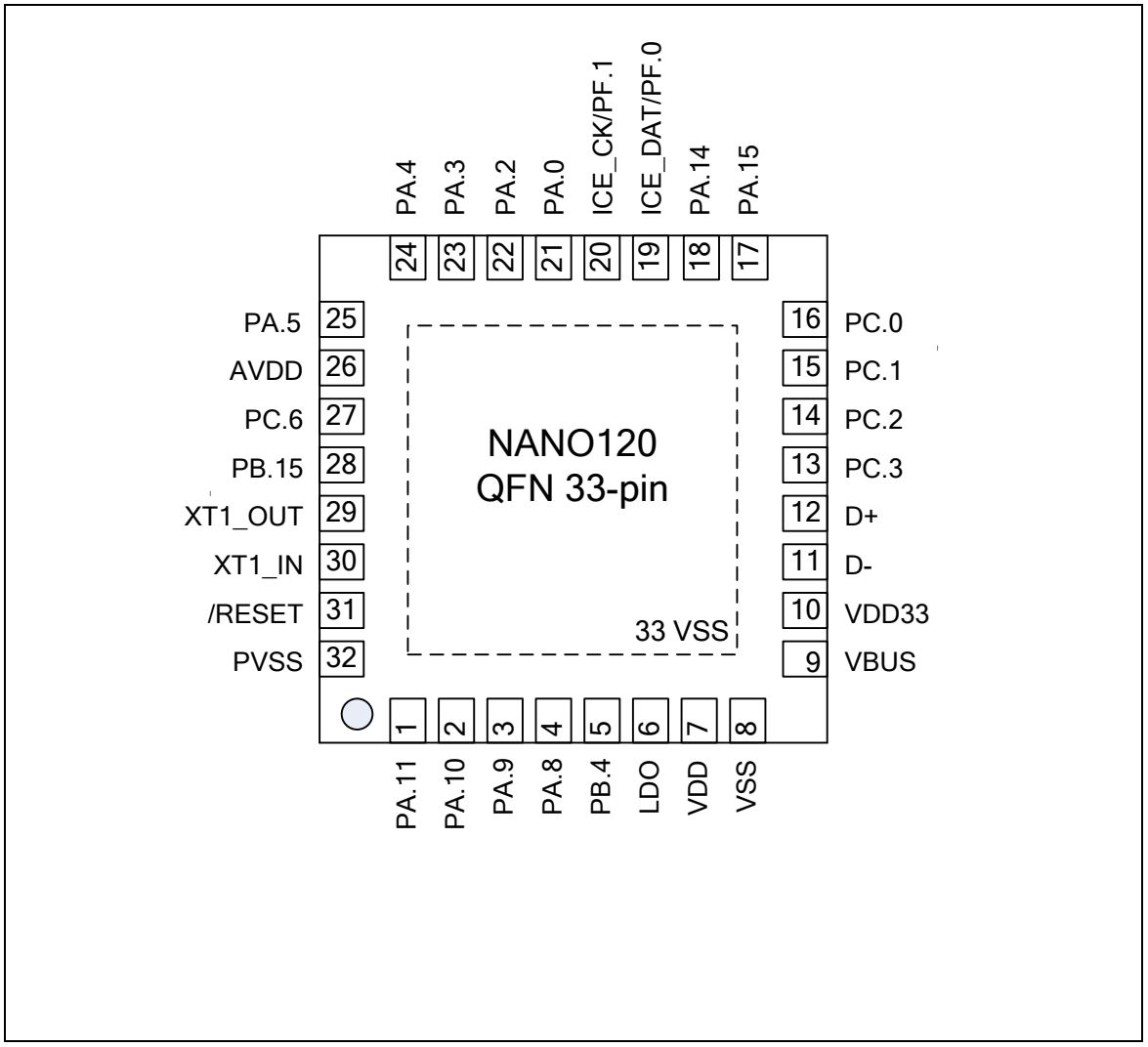


Figure 3-9 NuMicro™ Nano120 QFN 33-pin Assignment

3.4 Pin Description

3.4.1 NuMicro™ Nano100 Pin Description

Pin No.				Pin Name	Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
1				PE.15	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
2				PE.14	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
3				PE.13	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
4	1			PB.14	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				SPISS21	O	SPI2 2nd slave select pin
				nINT0	I	External interrupt0 input pin
5	2			PB.13	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				AD1	I/O	EBI Address/Data bus bit1
6	3	1		PB.12	I/O	Digital GPIO pin
				AD0	I/O	EBI Address/Data bus bit0
				CLKO	O	Frequency Divider output pin
7	4	2	32	X32O	O	External 32.768 kHz crystal output pin
8	5	3	1	X32I	I	External 32.768 kHz crystal input pin
9	6	4	2	PA.11	I/O	Digital GPIO pin
				I2C1SCK	I/O	I2C1 clock pin
				nRD	O	EBI read enable output pin
				SC0RST	O	SmartCard0 RST pin
				MOSI20	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
10	7	5	3	PA.10	I/O	Digital GPIO pin
				I2C1SDA	I/O	I2C1 data I/O pin
				nWR	O	EBI write enable output pin
				SC0PWR	O	SmartCard0 Power pin
				MISO20	I/O	SPI2 1st MISO (Master In, Slave Out) pin
11	8	6	4	PA.9	I/O	Digital GPIO pin

Pin No.				Pin Name	Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
				I2C0SCL	I/O	I2C0 clock pin
				SC0DAT	I/O	SmartCard0 DATA pin
				SPICLK2	O	SPI2 serial clock pin
12	9	7	5	PA.8	I/O	Digital GPIO pin
				I2C0SDA	I/O	I2C0 data I/O pin
				SC0CLK	O	SmartCard0 clock pin
				SPISS20	O	SPI2 1st slave select pin
13				PD.8	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
14				PD.9	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
15				PD.10	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
16				PD.11	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
17				PD.12	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
18				PD.13	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
19	10	8		PB.4	I/O	Digital GPIO pin
				RX1	I	UART1 Data receiver input pin
				SC0CD	I	SmartCard0 card detect pin
				SPISS20	O	SPI2 1st slave select pin
20	11	9		PB.5	I/O	Digital GPIO pin
				TX1	O	UART1 Data transmitter output pin
				SPICLK2	O	SPI2 serial clock pin
21	12			PB.6	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				RTSn1	O	UART1 Request to Send output pin
				ALE	O	EBI address latch enable output pin
				MISO20	I/O	SPI2 2nd MISO (Master In, Slave Out) pin

Pin No.				Pin Name	Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
22	13			PB.7	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				CTSn1	I	UART1 Clear to Send input pin
				nCS	O	EBI chip select enable output pin
				MOSI20	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
23	14	10	6	LDO	P	LDO output pin
24	15	11	7	VDD	P	Power supply for I/O ports and LDO source
25	16	12	8	VSS	P	Ground
26				PE.12	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
27				PE.11	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
28				PE.10	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
29				PE.9	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
30				PE.8	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
31				PE.7	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
32	17	13	9	PB.0	I/O	Digital GPIO pin
				RX0	I	UART0 Data receiver input pin
				MOSI10	I/O	SPI1 1st MOSI (Master Out, Slave In) pin
33	18	14	10	PB.1	I/O	Digital GPIO pin
				TX0	O	UART0 Data transmitter output pin
				MISO10	I/O	SPI1 1st MISO (Master In, Slave Out) pin
34	19	15	11	PB.2	I/O	Digital GPIO pin
				RTSn0	O	UART0 Request to Send output pin
				nWRL	O	EBI low byte write enable output pin
				SPICLK1	O	SPI1 serial clock pin
35	20	16	12	PB.3	I/O	Digital GPIO pin

Pin No.				Pin Name	Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
				CTSn0	I	UART0 Clear to Send input pin
				nWRH	O	EBI high byte write enable output pin
				SPISS10	O	SPI1 1st slave select pin
36	21			PD.6	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
37	22			PD.7	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
38	23			PD.14	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
39	24			PD.15	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
40				PC.5	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MOSI01	O	SPI0 2nd MOSI (Master Out, Slave In) pin
41				PC.4	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MISO01	I	SPI0 2nd MISO (Master In, Slave Out) pin
42	25	17	13	PC.3	I/O	Digital GPIO pin
				MOSI00	O	SPI0 1st MOSI (Master Out, Slave In) pin
				I2SDO	O	I2S data output
				SC1RST	O	SmartCard1 RST pin
43	26	18	14	PC.2	I/O	Digital GPIO pin
				MISO00	I	SPI0 1st MISO (Master In, Slave Out) pin
				I2SDI	I	I2S data input
				SC1PWR	O	SmartCard1 PWR pin
44	27	19	15	PC.1	I/O	Digital GPIO pin
				SPICLK0	I/O	SPI0 serial clock pin
				I2SBCLK	I/O	I2S bit clock pin
				SC1DAT	I/O	SmartCard1 DATA pin
45	28	20	16	PC.0	I/O	Digital GPIO pin
				SPISS00	I/O	SPI0 1st slave select pin

Pin No.				Pin Name	Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
				I2SLRCLK	I/O	I2S left right channel clock
				SC1CLK	O	SmartCard1 clock pin
46				PE.6	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
47	29	21		PE.5	I/O	Digital GPIO pin
				PWM1CH1	I/O	PWM1 Channel1 output
48	30	22		PB.11	I/O	Digital GPIO pin
				PWM1CH0	I/O	PWM1 Channel0 output
				TMR3	O	Timer3 external counter input
				MISO00	I/O	SPI0 1st MISO (Master In, Slave Out) pin
49	31	23		PB.10	I/O	Digital GPIO pin
				SPISS01	I/O	SPI0 2nd slave select pin
				TMR2	O	Timer2 external counter input
				MOSI00	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
50	32	24		PB.9	I/O	Digital GPIO pin
				SPISS11	I/O	SPI1 2nd slave select pin
				TMR1	O	Timer1 external counter input
				nINT0	I	External interrupt0 input pin
51				PE.4	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MOSI00	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
52				PE.3	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MISO00	I/O	SPI0 1st MISO (Master In, Slave Out) pin
53				PE.2	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				SPICLK0	O	SPI0 serial clock pin
54				PE.1	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				PWM1CH3	I/O	PWM1 Channel3 output
				SPISS00	O	SPI0 1st slave select pin

Pin No.				Pin Name	Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
55				PE.0	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				PWM1CH2	I/O	PWM1 Channel2 output
				I2SMCLK	O	I2S master clock output pin
56				PC.13	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MOSI11	O	SPI1 2nd MOSI (Master Out, Slave In) pin
				PWM1CH!	O	PWM1 Channel1 output
				SNOOPER	I	Snooper pin
				nINT0	I	External interrupt 0
				I2C0SCK	O	I2C0 clock pin
57				PC.12	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MISO11	I	SPI1 2nd MISO (Master In, Slave Out) pin
				PWM1CH0	O	PWM1 Channel0 output
				nINT0	I	External interrupt0 input pin
				I2C0SDA	I/O	I2C0 data I/O pin
58	33			PC.11	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				MOSI10	O	SPI1 1st MOSI (Master Out, Slave In) pin
				TX1	O	UART1 Data transmitter output pin
59	34			PC.10	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				MISO10	I	SPI1 1st MISO (Master In, Slave Out) pin
				RX1	I	UART1 Data receiver input pin
60	35			PC.9	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				SPICLK1	I/O	SPI1 serial clock pin
				I2C1SCK	I/O	I2C1 clock pin
61	36			PC.8	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.

Pin No.				Pin Name	Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
				SPISS10	I/O	SPI1 1st slave select pin
				MCLK	O	EBI external clock output pin
				I2C1SDA	I/O	I2C1 data I/O pin
62	37	25	17	PA.15	I/O	Digital GPIO pin
				PWM0CH3	I/O	PWM0 Channel3 output
				I2SMCLK	O	I2S master clock output pin
				TC3	I	Timer3 capture input
				TX0	O	UART0 Data transmitter output pin
63	38	26	18	PA.14	I/O	Digital GPIO pin
				PWM0CH2	I/O	PWM0 Channel2 output
				AD15	I/O	EBI Address/Data bus bit15
				TC2	I	Timer 2 capture input
				RX0	I	UART0 Data receiver input pin
64	39	27		PA.13	I/O	Digital GPIO pin
				PWM0CH1	I/O	PWM0 Channel1 output
				AD14	I/O	EBI Address/Data bus bit14
				TC1	I	Timer1 capture input
				I2C0SCK	I/O	I2C0 clock pin
65	40	28		PA.12	I/O	Digital GPIO pin
				PWM0CH0	I/O	PWM0 Channel0 output
				AD13	I/O	EBI Address/Data bus bit13
				TC0	I	Timer 0 capture input
				I2C0SDA	I/O	I2C0 data I/O pin
66	41	29	19	ICE_DAT	I/O	Serial Wired Debugger Data pin
				PF.0	I/O	Digital GPIO pin
				nINT0	I	External interrupt0 input pin
67	42	30	20	ICE_CK	I	Serial Wired Debugger Clock pin
				PF.1	I/O	Digital GPIO pin
				CLKO	O	Frequency Divider output pin
				nINT1	I	External interrupt1 input pin
68				VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit
69			33	VSS	P	Ground

Pin No.				Pin Name	Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
70	43	31		AVSS	**AP**	Ground Pin for analog circuit
71	44	32	21	PA.0	**I/O**	Digital GPIO pin
				ADC0	**AI**	ADC analog input0
72	45	33		PA.1	**I/O**	Digital GPIO pin
				ADC1	**AI**	ADC analog input1
				AD12	**I/O**	EBI Address/Data bus bit12
73	46	34	22	PA.2	**I/O**	Digital GPIO pin
				ADC2	**AI**	ADC analog input2
				AD11	**I/O**	EBI Address/Data bus bit11
				RX1	**I**	UART1 Data receiver input pin
74	47	35	23	PA.3	**I/O**	Digital GPIO pin
				ADC3	**AI**	ADC analog input3
				AD10	**I/O**	EBI Address/Data bus bit10
				TX1	**O**	UART1 Data transmitter output pin
75	48	36	24	PA.4	**I/O**	Digital GPIO pin
				ADC4	**AI**	ADC analog input4
				AD9	**I/O**	EBI Address/Data bus bit9
				I2C0SDA	**I/O**	I2C0 data I/O pin
76	49	37	25	PA.5	**I/O**	Digital GPIO pin
				ADC5	**AI**	ADC analog input5
				AD8	**I/O**	EBI Address/Data bus bit8
				I2C0SCK	**I/O**	I2C0 clock pin
77	50	38		PA.6	**I/O**	Digital GPIO pin
				ADC6	**AI**	ADC analog input6
				AD7	**I/O**	EBI Address/Data bus bit7
				TC3	**I**	Timer3 capture input
				PWM0CH3	**O**	PWM0 Channel3 output
78	51	39		PA.7	**I/O**	Digital GPIO pin
				ADC7	**AI**	ADC analog input7
				AD6	**I/O**	EBI Address/Data bus bit6
				TC2	**I**	Timer2 capture input
				PWM0CH2	**O**	PWM0 Channel2 output

Pin No.				Pin Name	Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
79				Vref	**AP**	Voltage reference input for ADC
80	52	40	26	AVDD	**AP**	Power supply for internal analog circuit
81				PD.0	**I/O**	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				RX1	**I**	UART1 Data receiver input pin
				SPISS20	**I/O**	SPI2 2nd slave select pin
				SC1CLK	**O**	SmartCard1 clock pin
82				PD.1	**I/O**	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				TX1	**O**	UART1 Data transmitter output pin
				SPICLK2	**I/O**	SPI2 serial clock pin
				SC1DAT	**I/O**	SmartCard1 DATA pin.
83				PD.2	**I/O**	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				RTSn1	**O**	UART1 Request to Send output pin
				I2SLRCLK	**I/O**	I2S left right channel clock
				MISO20	**I**	SPI2 1st MISO (Master In, Slave Out) pin
				SC1PWR	**O**	SmartCard1 Power pin
84				PD.3	**I/O**	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				CTSn1	**I**	UART1 Clear to Send input pin
				I2SBCLK	**I/O**	I2S bit clock pin
				MOSI20	**O**	SPI2 1st MOSI (Master Out, Slave In) pin
				SC1RST	**O**	SmartCard1 RST pin
85				PD.4	**I/O**	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				I2SDI	**I**	I2S data input
				MISO21	**I**	SPI2 2nd MISO (Master In, Slave Out) pin
				SC1CD	**I**	SmartCard1 card detect
86				PD.5	**I/O**	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.

Pin No.				Pin Name	Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
				I2SDO	O	I2S data output
				MOSI21	O	SPI2 2nd MOSI (Master Out, Slave In) pin
87	53	41		PC.7	I/O	Digital GPIO pin
				AD5	I/O	EBI Address/Data bus bit5
				TC1	I	Timer1 capture input
				PWM0CH1	O	PWM1 Channel1 output
88	54	42	27	PC.6	I/O	Digital GPIO pin
				AD4	I/O	EBI Address/Data bus bit4
				TC0	I	Timer 0 capture input
				SC1CD	I	SmartCard1 card detect pin
				PWM0CH0	O	PWM0 Channel0 output
89	55			PC.15	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				AD3	I/O	EBI Address/Data bus bit3
				TC0	I	Timer0 capture input
				PWM1CH2	O	PWM1 Channel1 output
90	56			PC.14	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				AD2	I/O	EBI Address/Data bus bit2
				PWM1CH3	I/O	PWM1 Channel3 output
91	57	43	28	PB.15	I/O	Digital GPIO pin
				nINT1	I	External interrupt1 input pin
				SNOOPER	I	Snooper pin
92	58	44	29	XT1_OUT	O	External 4~24 MHz crystal output pin
93	59	45	30	XT1_IN	I	External 4~24 MHz crystal input pin
94	60	46	31	nRESET	I	External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
95	61			VSS	P	Ground
96	62			VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit
97				PF.4	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.

Pin No.				Pin Name	Type	Description
LQFP 100-pin	LQFP 64-pin	LQFP 48-pin	QFN 33-pin			
				I2C0SDA	**I/O**	I2C0 data I/O pin
98				PF.5	**I/O**	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				I2C0SCK	**I/O**	I2C0 clock pin
99	63	47		PVSS	**P**	PLL Ground
100	64	48		PB.8	**I/O**	Digital GPIO pin
				ADCTRG	**I**	ADC external trigger input.
				TMR0	**I**	Timer0 external counter input
				nINT0	**I**	External interrupt0 input pin

Note: Pin Type: I = Digital Input; O = Digital Output; AI = Analog Input; AO = Analog Output; P = Power Pin; AP = Analog Power

3.4.2 NuMicro™ Nano120 Pin Description

Pin No.				Pin Name	Pin Type	Description
LQFP 100	LQFP 64	LQFP 48	QFN 33			
1				PE.15	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
2				PE.14	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
3				PE.13	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
4	1			PB.14	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				nINT0	I	External interrupt0 input pin
				SPISS21	O	SPI2 2nd slave select pin
5	2			PB.13	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				AD1	I/O	EBI Address/Data bus bit1
6	3	1		PB.12	I/O	Digital GPIO pin
				AD0	I/O	EBI Address/Data bus bit0
				CLKO	O	Frequency Divider output pin
7	4	2		X32O	O	External 32.768 kHz crystal output pin
8	5	3		X32I	I	External 32.768 kHz crystal input pin
9	6	4	1	PA.11	I/O	Digital GPIO pin
				I2C1SCK	I/O	I2C1 clock pin
				nRD	O	EBI read enable output pin
				SC0RST	O	SmartCard0 RST pin
				MOSI20	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
10	7	5	2	PA.10	I/O	Digital GPIO pin
				I2C1SDA	I/O	I2C1 data I/O pin
				nWR	O	EBI write enable output pin
				SC0PWR	O	SmartCard0 Power pin
				MISO20	I/O	SPI2 1st MISO (Master In, Slave Out) pin
11	8	6	3	PA.9	I/O	Digital GPIO pin
				I2C0SCL	I/O	I2C0 clock pin

Pin No.				Pin Name	Pin Type	Description
LQFP 100	LQFP 64	LQFP 48	QFN 33			
				SC0DAT	I/O	SmartCard0 DATA pin
				SPICLK2	O	SPI2 serial clock pin
12	9	7	4	PA.8	I/O	Digital GPIO pin
				I2C0SDA	I/O	I2C0 data I/O pin
				SC0CLK	O	SmartCard0 clock pin
				SPISS20	O	SPI2 1st slave select pin
13				PD.8	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
14				PD.9	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
15				PD.10	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
16				PD.11	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
17				PD.12	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
18				PD.13	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
19	10	8	5	PB.4	I/O	Digital GPIO pin
				RX1	I	UART1 Data receiver input pin
				SC0CD	I	SmartCard0 card detect pin
				SPISS20	O	SPI2 1st slave select pin
20	11	9		PB.5	I/O	Digital GPIO pin
				TX1	O	UART1 Data transmitter output pin
				SPICLK2	O	SPI2 serial clock pin
21	12			PB.6	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				RTSn1	O	UART1 Request to Send output pin
				ALE	O	EBI address latch enable output pin
				MISO20	I/O	SPI2 2nd MISO (Master In, Slave Out) pin

Pin No.				Pin Name	Pin Type	Description
LQFP 100	LQFP 64	LQFP 48	QFN 33			
22	13			PB.7	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				CTSn1	I	UART1 Clear to Send input pin
				nCS	O	EBI chip select enable output pin
				MOSI20	I/O	SPI2 1st MOSI (Master Out, Slave In) pin
23	14	10	6	LDO	P	LDO output pin
24	15	11	7	VDD	P	Power supply for I/O ports and LDO source
25	16	12	8	VSS	P	Ground
26				PE.8	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
27				PE.7	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
28	17	13	9	VBUS	USB	POWER SUPPLY: From USB Host or HUB.
29	18	14	10	VDD33	USB	Internal Power Regulator Output 3.3V Decoupling Pin
30	19	15	11	D-	USB	USB Differential Signal D-
31	20	16	12	D+	USB	USB Differential Signal D+
32	21	17		PB.0	I/O	Digital GPIO pin
				RX0	I	UART0 Data receiver input pin
				MOSI10	I/O	SPI1 1st MOSI (Master Out, Slave In) pin
33	22	18		PB.1	I/O	Digital GPIO pin
				TX0	O	UART0 Data transmitter output pin
				MISO10	I/O	SPI1 1st MISO (Master In, Slave Out) pin
34	23	19		PB.2	I/O	Digital GPIO pin
				RTSn0	O	UART0 Request to Send output pin
				nWRL	O	EBI low byte write enable output pin
				SPICLK1	O	SPI1 serial clock pin
35	24	20		PB.3	I/O	Digital GPIO pin
				CTSn0	I	UART0 Clear to Send input pin
				nWRH	O	EBI high byte write enable output pin
				SPISS10	O	SPI1 1st slave select pin

Pin No.				Pin Name	Pin Type	Description
LQFP 100	LQFP 64	LQFP 48	QFN 33			
36				PD.6	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
37				PD.7	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
38				PD.14	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
39				PD.15	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
40				PC.5	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MOSI01	O	SPI0 2nd MOSI (Master Out, Slave In) pin
41				PC.4	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MISO01	I	SPI0 2nd MISO (Master In, Slave Out) pin
42	25	21	13	PC.3	I/O	Digital GPIO pin
				MOSI00	O	SPI0 1st MOSI (Master Out, Slave In) pin
				I2SDO	O	I2S data output
				SC1RST	O	SmartCard1 RST pin
43	26	22	14	PC.2	I/O	Digital GPIO pin
				MISO00	I	SPI0 1st MISO (Master In, Slave Out) pin
				I2SDI	I	I2S data input
				SC1PWR	O	SmartCard1 PWR pin
44	27	23	15	PC.1	I/O	Digital GPIO pin
				SPICLK0	I/O	SPI0 serial clock pin
				I2SBCLK	I/O	I2S bit clock pin
				SC1DAT	I/O	SmartCard1 DATA pin
45	28	24	16	PC.0	I/O	Digital GPIO pin
				SPISS00	I/O	SPI0 1st slave select pin
				I2SLRCLK	I/O	I2S left right channel clock
				SC1CLK	O	SmartCard1 clock pin

Pin No.				Pin Name	Pin Type	Description
LQFP 100	LQFP 64	LQFP 48	QFN 33			
46				PE.6	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
47	29			PE.5	I/O	Digital GPIO pin
				PWM1CH1	I/O	PWM1 Channel1 output
48	30			PB.11	I/O	Digital GPIO pin
				TMR3	O	Timer3 external counter input
				PWM1CH0	I/O	PWM1 Channel0 output
				MISO00	I/O	SPI0 1st MISO (Master In, Slave Out) pin
49	31			PB.10	I/O	Digital GPIO pin
				SPISS01	I/O	SPI0 2nd slave select pin
				TMR2	O	Timer2 external counter input
				MOSI00	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
50	32			PB.9	I/O	Digital GPIO pin
				SPISS11	I/O	SPI1 2nd slave select pin
				TMR1	O	Timer1 external counter input
				nINT0	I	External interrupt0 input pin
51				PE.4	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MOSI00	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
52				PE.3	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MISO00	I/O	SPI0 1st MISO (Master In, Slave Out) pin
53				PE.2	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				SPICLK0	O	SPI0 serial clock pin
54				PE.1	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				PWM1CH3	I/O	PWM1 Channel3 output
				SPISS00	O	SPI0 1st slave select pin
55				PE.0	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.

Pin No.				Pin Name	Pin Type	Description
LQFP 100	LQFP 64	LQFP 48	QFN 33			
				PWM1CH2	I/O	PWM1 Channel2 output
				I2SMCLK	O	I2S master clock output pin
56				PC.13	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MOSI11	O	SPI1 2nd MOSI (Master Out, Slave In) pin
				PWM1CH!	O	PWM1 Channel1 output
				SNOOPER	I	Snooper pin
				nINT0	I	External interrupt 0 input pin
				I2C0SCK	O	I2C0 clock pin
57				PC.12	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				MISO11	I	SPI1 2nd MISO (Master In, Slave Out) pin
				PWM1CH0	O	PWM1 Channel 0 output
				nINT0	I	External interrupt 0 input pin
				I2C0SDA	I/O	I2C0 data I/O pin
58	33			PC.11	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				MOSI10	O	SPI1 1st MOSI (Master Out, Slave In) pin
				TX1	O	UART1 Data transmitter output pin
59	34			PC.10	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				MISO10	I	SPI1 1st MISO (Master In, Slave Out) pin
				RX1	I	UART1 Data receiver input pin
60	35			PC.9	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				SPICLK1	I/O	SPI1 serial clock pin
				I2C1SCK	I/O	I2C1 clock pin
61	36			PC.8	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				SPISS10	I/O	SPI1 1st slave select pin
				MCLK	O	EBI external clock output pin

Pin No.				Pin Name	Pin Type	Description
LQFP 100	LQFP 64	LQFP 48	QFN 33			
				I2C1SDA	I/O	I2C1 data I/O pin
62	37	25	17	PA.15	I/O	Digital GPIO pin
				PWM0CH3	I/O	PWM0 Channel3 output
				I2SMCLK	O	I2S master clock output pin
				TC3	I	Timer3 capture input
				TX0	O	UART0 Data transmitter output pin
63	38	26	18	PA.14	I/O	Digital GPIO pin
				PWM0CH2	I/O	PWM0 Channel2 output
				AD15	I/O	EBI Address/Data bus bit15
				TC2	I	Timer 2 capture input
				RX0	I	UART0 Data receiver input pin
64	39	27		PA.13	I/O	Digital GPIO pin
				PWM0CH1	I/O	PWM0 Channel1 output
				AD14	I/O	EBI Address/Data bus bit14
				TC1	I	Timer1 capture input
				I2C0SCK	I/O	I2C0 clock pin
65	40	28		PA.12	I/O	Digital GPIO pin
				PWM0CH0	I/O	PWM0 Channel0 output
				AD13	I/O	EBI Address/Data bus bit13
				TC0	I	Timer 0 capture input
				I2C0SDA	I/O	I2C0 data I/O pin
66	41	29	19	ICE_DAT	I/O	Serial Wired Debugger Data pin
				PF.0	I/O	Digital GPIO pin
				nINT0	I	External interrupt0 input pin
67	42	30	20	ICE_CK	I	Serial Wired Debugger Clock pin
				PF.1	I/O	Digital GPIO pin
				CLKO	O	Frequency Divider output pin
				nINT1	I	External interrupt1 input pin
68				VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit
69			33	VSS	P	Ground
70	43	31		AVSS	AP	Ground Pin for analog circuit
71	44	32	21	PA.0	I/O	Digital GPIO pin

Pin No.				Pin Name	Pin Type	Description
LQFP 100	LQFP 64	LQFP 48	QFN 33			
				ADC0	AI	ADC analog input0
72	45	33		PA.1	I/O	Digital GPIO pin
				ADC1	AI	ADC analog input1
				AD12	I/O	EBI Address/Data bus bit12
73	46	34	22	PA.2	I/O	Digital GPIO pin
				ADC2	AI	ADC analog input2
				AD11	I/O	EBI Address/Data bus bit11
				RX1	I	UART1 Data receiver input pin
74	47	35	23	PA.3	I/O	Digital GPIO pin
				ADC3	AI	ADC analog input3
				AD10	I/O	EBI Address/Data bus bit10
				TX1	O	UART1 Data transmitter output pin
75	48	36	24	PA.4	I/O	Digital GPIO pin
				ADC4	AI	ADC analog input4
				AD9	I/O	EBI Address/Data bus bit9
				I2C0SDA	I/O	I2C0 data I/O pin
76	49	37	25	PA.5	I/O	Digital GPIO pin
				ADC5	AI	ADC analog input5
				AD8	I/O	EBI Address/Data bus bit8
				I2C0SCK	I/O	I2C0 clock pin
77	50	38		PA.6	I/O	Digital GPIO pin
				ADC6	AI	ADC analog input6
				AD7	I/O	EBI Address/Data bus bit7
				TC3	I	Timer3 capture input
				PWM0CH3	O	PWM0 Channel3 output
78	51	39		PA.7	I/O	Digital GPIO pin
				ADC7	AI	ADC analog input7
				AD6	I/O	EBI Address/Data bus bit6
				TC2	I	Timer2 capture input
				PWM0CH2	O	PWM0 Channel2 output
79				Vref	AP	Voltage reference input for ADC
80	52	40	26	AVDD	AP	Power supply for internal analog circuit

Pin No.				Pin Name	Pin Type	Description
LQFP 100	LQFP 64	LQFP 48	QFN 33			
81				PD.0	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				RX1	I	UART1 Data receiver input pin
				SPISS20	I/O	SPI2 2nd slave select pin
				SC1CLK	O	SmartCard1 clock pin
82				PD.1	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				TX1	O	UART1 Data transmitter output pin
				SPICLK2	I/O	SPI2 serial clock pin
				SC1DAT	I/O	SmartCard1 DATA pin.
83				PD.2	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				RTSn1	O	UART1 Request to Send output pin
				I2SLRCLK	I/O	I2S left right channel clock
				MISO20	I	SPI2 1st MISO (Master In, Slave Out) pin
				SC1PWR	O	SmartCard1 Power pin
84				PD.3	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				CTSn1	I	UART1 Clear to Send input pin
				I2SBCLK	I/O	I2S bit clock pin
				MOSI20	O	SPI2 1st MOSI (Master Out, Slave In) pin
				SC1RST	O	SmartCard1 RST pin
85				PD.4	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				I2SDI	I	I2S data input
				MISO21	I	SPI2 2nd MISO (Master In, Slave Out) pin
				SC1CD	I	SmartCard1 card detect
86				PD.5	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				I2SDO	O	I2S data output
				MOSI21	O	SPI2 2nd MOSI (Master Out, Slave In) pin

Pin No.				Pin Name	Pin Type	Description
LQFP 100	LQFP 64	LQFP 48	QFN 33			
87	53	41		PC.7	I/O	Digital GPIO pin
				AD5	I/O	EBI Address/Data bus bit5
				TC1	I	Timer1 capture input
				PWM0CH1	O	PWM1 Channel1 output
88	54	42	27	PC.6	I/O	Digital GPIO pin
				AD4	I/O	EBI Address/Data bus bit4
				TC0	I	Timer 0 capture input
				SC1CD		SmartCard1 card detect pin
				PWM0CH0	O	PWM0 Channel0 output
89	55			PC.15	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				AD3	I/O	EBI Address/Data bus bit3
				TC0	I	Timer0 capture input
				PWM1CH2	O	PWM1 Channel1 output
90	56			PC.14	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP48 package.
				AD2	I/O	EBI Address/Data bus bit2
				PWM1CH3	I/O	PWM1 Channel3 output
91	57	43	28	PB.15	I/O	Digital GPIO pin
				nINT1	I	External interrupt1 input pin
				SNOOPER	I	Snooper pin
92	58	44	29	XT1_OUT	O	External 4~24 MHz crystal output pin
93	59	45	30	XT1_IN	I	External 4~24 MHz crystal input pin
94	60	46	31	nRESET	I	External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
95	61			VSS	P	Ground
96	62			VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit
97				PF.4	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				I2C0SDA	I/O	I2C0 data I/O pin

Pin No.				Pin Name	Pin Type	Description
LQFP 100	LQFP 64	LQFP 48	QFN 33			
98				PF.5	I/O	Digital GPIO pin User program must enable pull-up resistor in LQFP64 and LQFP48 package.
				I2C0SCK	I/O	I2C0 clock pin
99	63	47	32	PVSS	P	PLL Ground
100	64	48		PB.8	I/O	Digital GPIO pin
				ADCTRG	I	ADC external trigger input.
				TMR0	I	Timer0 external counter input
				nINT0	I	External interrupt0 input pin

Note: Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; AO= Analog Output; P=Power Pin; AP=Analog Power

4 BLOCK DIAGRAM

4.1 Nano100 Block Diagram

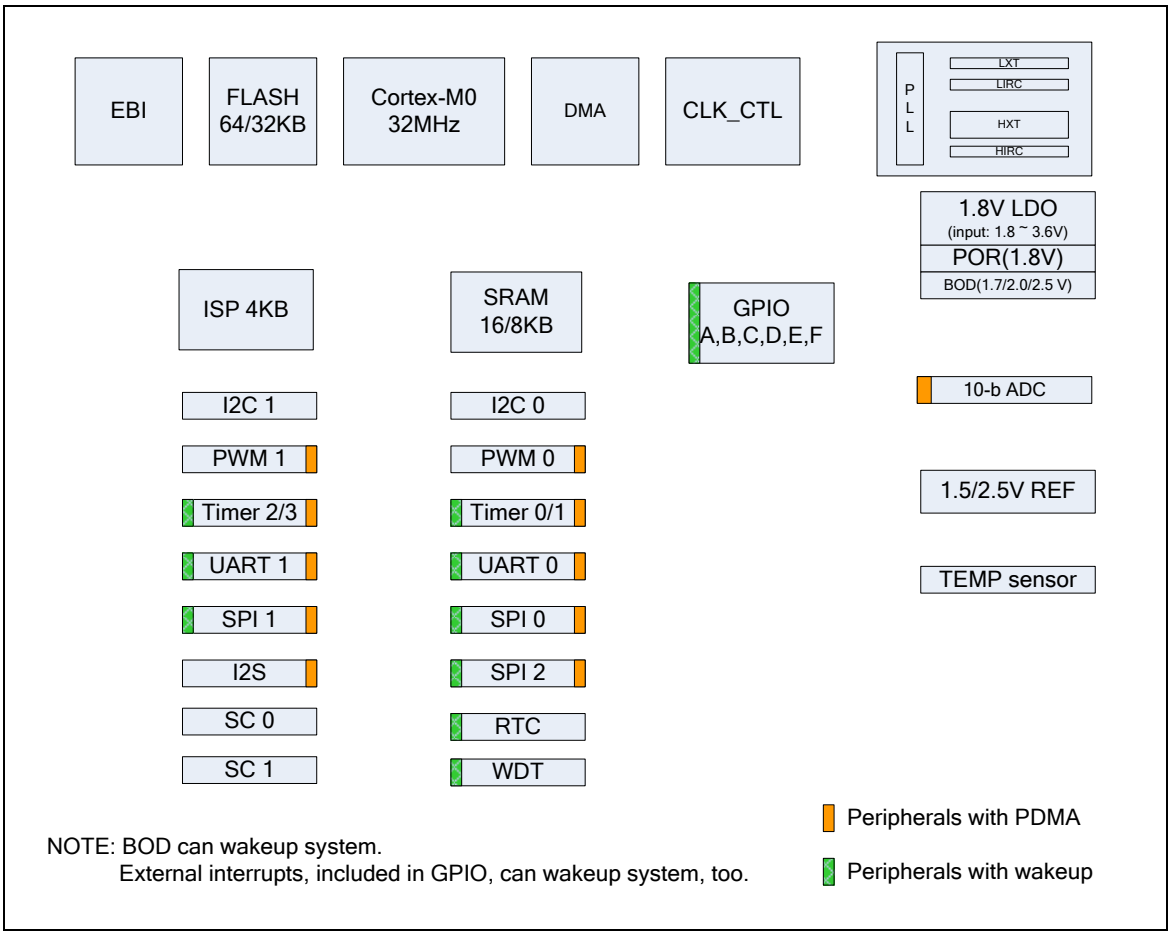


Figure 4-1 NuMicro™ Nano100 Block Diagram

4.2 Nano120 Block Diagram

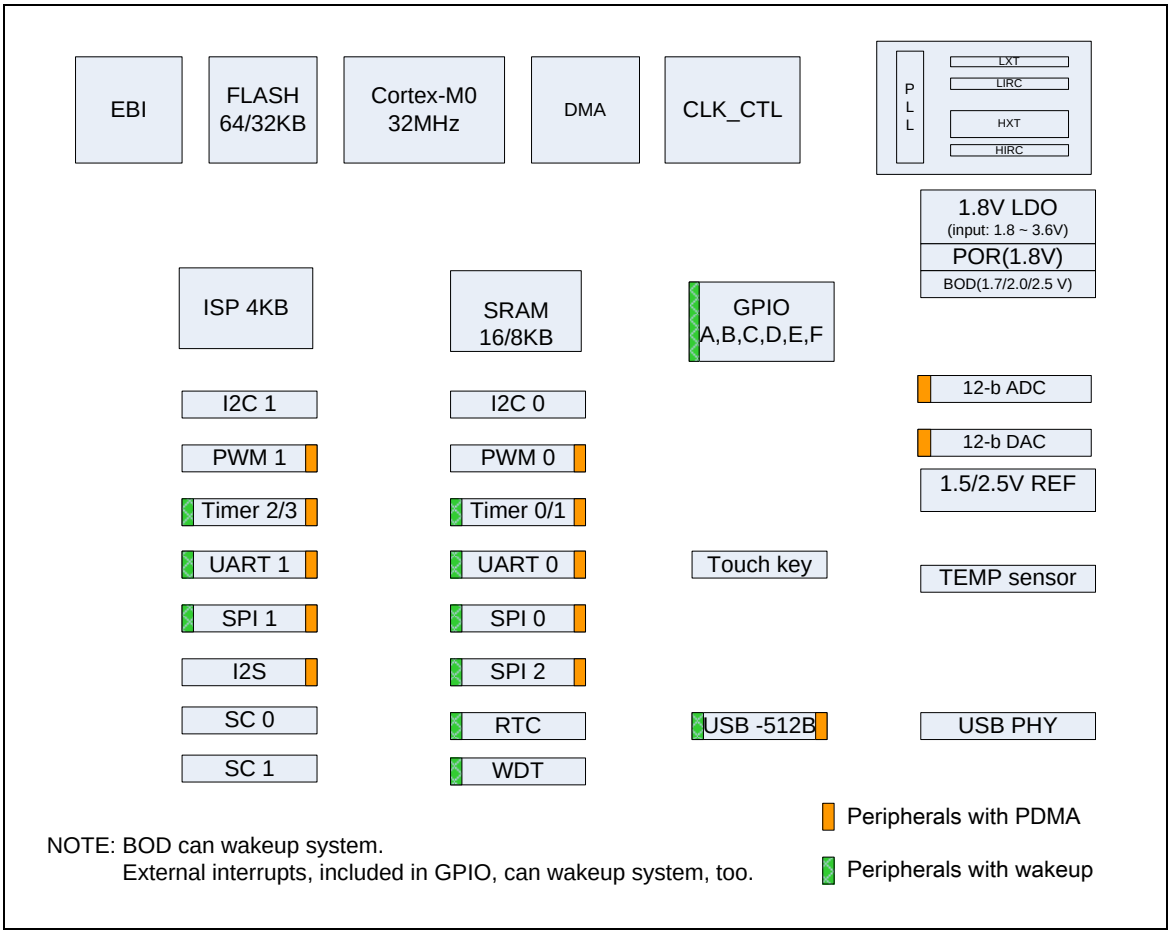


Figure 4-2 NuMicro™ Nano120 Block Diagram

5 FUNCTIONAL DESCRIPTION

5.1 ARM® Cortex™-M0 Core

5.1.1 Overview

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The following figure shows the functional controller of processor.

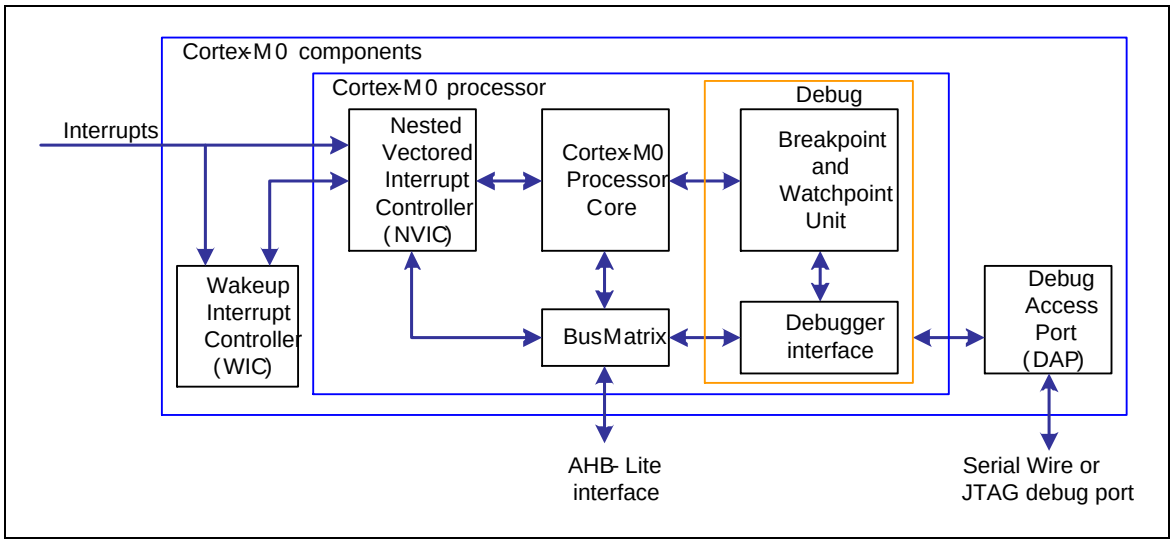


Figure 5-1 M0 Functional Block

5.1.2 Features

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - Supports little-endian data accesses
  - Capable of deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multi-cycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using Wait For Interrupt (WFI), Wait For Event

(WFE) instructions, or return from interrupt sleep-on-exit feature

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-Maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Wake-up Interrupt Controller (WIC), providing Ultra-low Power Sleep mode support
- Debug support:
  - Four hardware breakpoints
  - Two watch points
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface providing simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

5.2 Memory Organization

5.2.1 Overview

Nano100 provides 4G-byte addressing space. The memory locations assigned to each on-chip modules are shown in following. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip module. Nano100 series only supports little-endian data format.

5.2.2 Memory Map

The memory locations assigned to each on-chip controllers are shown in the following table.

Address Space	Token	Modules
Flash & SRAM Memory Space		
0x0000_0000 – 0x0000_FFFF	FLASH_BA	FLASH Memory Space (64KB)
0x2000_0000 – 0x2000_3FFF	SRAM_BA	SRAM Memory Space (16KB)
0x6000_0000 --- 0x6001_FFFF	EXTMEM_BA	External Memory Space(128KB)
AHB Modules Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Management Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	DMA_BA	DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_03FF	EBI_BA	External Bus Interface Control Registers
APB1 Modules Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watch-Dog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer 0 and Timer 1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I2C 0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI 0 with Master/Slave function Control Registers
0x4004_0000 – 0x4004_3FFF	PWM0_BA	PWM 0 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART 0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB FS device Controller Registers
0x400A_0000 – 0x400A_3FFF	Reserved	Reserved
0x400D_0000 – 0x400D_3FFF	SPI2_BA	SPI 2 with Master/Slave function Control Registers
0x400E_0000 – 0x400E_3FFF	ADC10_BA	12-bit Analog-Digital-Converter (ADC10) Control Registers
APB2 Modules Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer 2 and Timer 3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I2C 1 Interface Control Registers

0x4013_0000 – 0x4013_3FFF	SPI1_BA	SPI 1 with Master/Slave function Control Registers
0x4014_0000 – 0x4014_3FFF	PWM1_BA	PWM 1 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4019_0000 – 0x4019_3FFF	SC0_BA	Smart Card 0 Control Registers
0x401A_0000 – 0x401A_3FFF	I2S_BA	I2S Control Registers
0x401B_0000 – 0x401B_3FFF	SC1_BA	Smart Card 1 Control Registers
System Control Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

5.3 Nested Vectored Interrupt Controller (NVIC)

5.3.1 Overview

Cortex-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features:

5.3.2 Features

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "ARM® Cortex™-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

5.4 System Manager

5.4.1 Overview

System manager mainly controls the power modes, wake-up source, system resets and system memory map. It also provides information about product ID, chip reset, IP reset, and multi-function pin control.

5.4.2 Features

- Power modes and wake-up sources
- System resets
- System Memory Map
- System manager registers for :
  - Product ID
  - Chip and IP reset
  - Multi-functional pin control

5.5 Clock Controller

5.5.1 Overview

The clock controller generates clocks for the whole chip, including system clocks (CPU clock, HCLKx, and PCLKx) and all peripheral engine clocks. HCLKx means AHB bus clock for peripherals on AHB bus. PCLKx means APB bus clock for peripherals on APB bus. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a 4-bit clock divider. The chip will not enter power-down mode until CPU sets the power down enable bit (PD_EN(PWRCTL[6])) and CPU executes the WFI instruction. In the Power-down mode, clock controller turns off the external high frequency crystal, internal high frequency oscillator, and system clocks (CPU clock, HCLKx, and PCLKx) to reduce the power consumption to minimum.

5.5.2 Features

- Generates clocks for system clocks and all peripheral engine clocks
- Each peripheral engine clock can be turned on/off.
- High frequency crystal, internal high frequency oscillator, and system clocks will be turned off when chip is in Power-down mode.

5.6 FLASH Memory Controller (FMC)

5.6.1 Overview

This chip is equipped with 32KB/64KB on-chip embedded Flash EPROM for application program memory (APROM) that can be updated through ISP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip power on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, this chip also provides DATA Flash Region, the data flash is shared with original program memory and its start address is configurable and defined by user in Config1. The data flash size is defined by user application request.

5.6.2 Features

- AHB interface compatible
- Run up to 32 MHz with zero wait state for discontinuous address read access
- 32KB/64KB application program memory (APROM)
- 4KB in system programming (ISP) loader program memory (LDROM)
- Programmable data flash start address and memory size with 512 bytes page erase unit
- In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM

5.7 External Bus Interface

5.7.1 Overview

This chip is equipped with an external bus interface (EBI) to access external device. To save the connections between external device and this chip, EBI support address bus and data bus multiplex mode. Also, address latch enable (ALE) signal is used to differentiate the address and data cycle.

5.7.2 Features

- External devices with max. 64 Kbytes size (8-bit data width)/128 Kbytes (16-bit data width) supported
- Supports variable external bus base clock (MCLK)
- Supports 8-bit or 16-bit data width
- Supports variable data access time (tACC), address latch enable time (tALE) and address hold time (tAHD)
- Address bus and data bus multiplex mode supported to save the address pins
- Configurable idle cycle supported for different access condition: Write command finish (W2X), Read-to-Read (R2R), Read-to-Write (R2W)
- Supports PDMA and VDMA transfer

5.8 General Purpose I/O Controller

5.8.1 Overview

The NuMicro™ Nano100 series have up to 51 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 51 pins are arranged in 6 ports named with GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. Each one of the 51 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be independently software configured as input, output, and open-drain mode. Each I/O pin has a very weak individual pull-up resistor which is about 110 KΩ~300 KΩ for VDD from 1.8 V to 3.6 V.

5.8.2 Features

- Three I/O modes:
  - Schmitt trigger Input-only with high impendence
  - Push-pull output
  - Open-drain output
- I/O pin configured as interrupt source with edge/level setting
- Enabling the pin interrupt function will also enable the pin wake-up function

5.9 DMA Controller

5.9.1 Overview

The DMA controller contains a four-channel peripheral direct memory access (PDMA) controller and a one-channel video direct memory access (VDMA) controller that transfers data to and from memory or transfer data to and from peripherals.For VDMA channel (DMA CH0), it only supports block transfer from memory to memory. For PDMA channel (DMA CH1~CH4), there is one-word buffer as transfer buffer between the Peripherals APB devices and Memory. And for VDMA channel (DMA CH0), there is a two-word buffer.

User can stop the PDMA or VDMA operation by disable PDMACEN (PDMA_CSRx[0]) or VDMACEN(VDMA_CSR[0]), respectively. User can polling TD_IS (PDMA_ISRx[1] or VDMA_ISRx[1]) or enable TD_IE (PDMA_IERx[1] or VDMA_IERx[1]) and wait interrupt to check DMA transfer complete. The DMA controller can increase source or destination address, fixed or wrap around them as well.

5.9.2 Features

- Five channels: 1 VDMA channel and 4 PDMA channels. Each channel can support a unidirectional transfer.
- VDMA
  - Supports Memory-to-memory transfer
  - Supports block transfer with stride
  - Supports word/half-word/byte boundary address
  - Supports address direction: increment and decrement
- PDMA
  - Supports Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
  - Supports word boundary address
  - Supports word alignment transfer length in memory-to-memory mode
  - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
  - Supports word/half-word/byte transfer data width from/to peripheral
  - Supports address direction: increment, fixed, and wrap around
- AMBA AHB Master/Slave interface compatible, for data transfer and register read/write.
- Hardware round robin priority scheme.

5.10 Timer Controller

5.10.1 Overview

This chip is equipped with four timer modules including TIMER0, TIMER1, TIMER2 and TIMER3 (TIMER0/1 is at APB1 and TIMER2/3 is at APB2), which allow user to easily implement a counting scheme or timing control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generate an interrupt signal upon timeout, or provide the current value of count during operation.

5.10.2 Features

- Independent Clock Source for each Timer (TMRx_CLK, x= 0, 1,2,3)
- Time out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / 25 MHz) * (2^8) * (2^24), if TCLK = 25 MHz
- Internal 8-bit pre-scale counter
- Internal 24-bit up counter is readable through TDR (Timer Data Register)
- Supports One-shot, Periodic and Output Toggle Operation mode
- Supports external pin capture for interval measurement
- Supports external pin capture for timer counter reset
- Supports Inter-Timer trigger
- Supports Internal trigger event to ADC and PDMA

5.11 Pulse Width Modulation (PWM)

5.11.1 Overview

This chip has two PWM controllers, each controller has 4 independent PWM outputs, CH0~CH3, or as 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators.

Each of the two PWM outputs, (CH0, CH1), (CH2, CH3), share the same 8-bit prescaler, clock divider providing 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16). Each PWM output has independent 16-bit PWM down-count counter for PWM period control, and 16-bit comparators for PWM duty control. Each dead-zone generator has two outputs. The first dead-zone generator output is CH0 and CH1, and for the second dead-zone generator, the output is CH2 and CH3. The 2 sets of PWM controller total provide eight independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches 0. PWM interrupt will be asserted when both PWM interrupt source and its corresponding enable bit are active. Each PWM output can be configured as one-shot mode to produce only one PWM cycle signal or continuous mode to output PWM waveform continuously.

When DZEN01 (PWMx_CTL[4]) (x=0,1) is set, CH0 and CH1 perform complementary PWM paired function; the paired PWM timing, period, duty and dead-time are determined by PWM channel 0 timer and Dead-zone generator 0. Similarly, When DZEN23 (PWMx_CTL[5]) is set the complementary PWM pair of (CH2, CH3) is controlled by PWM channel 2.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be loaded into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at

PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM output is set as continuous mode, when the down counter reaches 0, it is reloaded with CN of PWMx_DUTYy (y=0~3) Register automatically then start decreases, repeatedly. If the PWM output is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse width modulation. The counter control logic changes the output level when down-counter value matches the value of compare register.

The alternate feature of the PWM is digital input capture function. If capture function is enabled the PWM output pin is switched as capture input pin. The capture channel 0 and PWM CH0 share one timer; and the capture channel 1 and PWM CH1 share one timer, and etc. Therefore user must setup the PWM timer before enabling capture feature. After capture feature of channel 0 is enabled, the capture always latches PWM CH0 timer value to Capture Rising Latch Register CRL (PWMx_CRL0[15:0]) when input channel has a rising transition and latches PWM CH0 timer value to Capture Falling Latch Register CFL (PWMx_CFL0[15:0]) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CRL_IE0 (PWMx_CAPINTEN[0]) for rising transition or CFL_IE0 (PWMx_CAPINTEN[1]) for falling transition. Whenever Capture rising event latched for channel 0, the PWM CH0 timer will be reload at this moment if the corresponding reload enable bit CAPRELOADREN0 (PWMx_CAPCTL[6]) is set.

The maximum captured frequency that PWM can capture is dominated by the capture interrupt latency. When capture interrupt occurs, software will do at least three steps, they are: Read PWMx_INTSTS to get interrupt source and Read PWMx_CRLy/PWMx_CFLy(y=0~3) to get capture value and finally write 1 to clear PWMx_INTSTS. If interrupt latency will take time T0 to finish, the capture signal mustn't transient during this interval. In this case, the maximum capture frequency will be 1/T0.

5.11.2 Features

5.11.2.1 PWM function:

- Two PWM controllers, each controller has 4 independent PWM outputs, CH0~CH3, or as 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators.
- Up to 8 PWM channels or 4 PWM paired channels.
- Up to 16 bits PWM counter width.
- PWM Interrupt request synchronous with PWM period.
- One-shot or Continuous mode.
- Four Dead-Zone generators

5.11.2.2 Capture Function:

- Timing control logic shared with PWM timer.
- 8 Capture input channels shared with 8 PWM output channels.
- Each channel supports one rising latch register CRL (PWMx_CRL0[15:0]), one falling latch register CFL (PWMx_CFL0[15:0]) and Capture interrupt flag CAPIF0 (PWMx_CAPINTSTS[0]) .
- Eight 16-bit counters for eight capture channels or four 32-bit counter for four capture channels when cascade is enabled:when CH01CASKEN (PWMx_CAPCTL[13]) is set ,the original 16-bit counter of channel 1 will combine with channel 0's 16-bit counter for channel 0 input capture counting and so does CH23CASKEN

(PWMx_CAPCTL[29]) for channel 2,3

- Supports PDMA transfer function for PWMx channel 0, 2

5.12 Watchdog Timer Controller

5.12.1 Overview

The purpose of Watchdog Timer is to perform a system reset after the software running into a problem. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up CPU from power-down mode. The watchdog timer includes an 18-bit free running counter with programmable time-out intervals.

5.12.2 Features

- 18-bit free running WDT counter for Watchdog timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^18) and the time-out interval is 104 ms ~ 26.316 s (if WDT_CLK = 10 kHz).
- Reset period = (1 / 10 kHz) * 63, if WDT_CLK = 10 kHz.

5.13 RTC

5.13.1 Overview

Real Time Clock (RTC) unit provides user the real time and calendar message. The Clock Source of RTC is from an external 32.768 kHz crystal connected at pins X32I and X32O (reference to pin Description) or from an external 32.768 kHz oscillator output fed at pin X32I. The RTC unit provides the time message (second, minute, hour) in Time Loading Register (TLR) as well as calendar message (day, month, year) in Calendar Loading Register (CLR). The data message is expressed in BCD format. This unit offers alarm function that user can preset the alarm time in Time Alarm Register (TAR) and alarm calendar in Calendar Alarm Register (CAR).

The RTC unit supports periodic Time Tick and Alarm Match interrupts. The periodic interrupt has 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (TTR[2:0]). When RTC counter in TLR and CLR is equal to alarm setting time registers TAR and CAR, the alarm interrupt flag (AIS(RTC_RIIR[0])) is set and the alarm interrupt is requested if the alarm interrupt is enabled (AIER(RTC_RIER[0])=1). The RTC Time Tick (if wake-up CPU function is enabled, (TWKE(RTC_TTR[3])) high)) and Alarm Match can cause CPU wake-up from idle or Power-down mode.

5.13.2 Features

- There is a time counter (second, minute, hour) and calendar counter (day, month, year) for user to check the time.
- Alarm register (second, minute, hour, day, month, year).
- 12-hour or 24-hour mode is selectable.
- Leap year compensation automatically.
- Day of week counter.
- Frequency compensate register (FCR).
- All time and calendar message is expressed in BCD code.
- Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt
- Supports wake-up CPU from power-down mode.
- Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers.

5.14 UART Controller

5.14.1 Overview

The UART Controller provides up to two channels of Universal Asynchronous Receiver/Transmitter (UART) modules and performs Normal Speed UART, and supports flow control function. The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU.

The UART controller also supports IrDA (SIR), LIN Master/Slave and RS-485 function modes.

5.14.2 Features

- Full duplex, asynchronous communications.
- Separate receiving / transmitting 16 bytes entry FIFO for data payloads.
- Supports hardware auto-flow control function (CTSn, RTSn) and programmable (CTSn, RTSn) flow control trigger level.
- Supports programmable baud rate generator for each channel.
- Supports auto-baud rate detect function.
- Supports programmable receiver buffer trigger level.
- Supports incoming data or CTSn to wake-up function.
- Supports 9 bit receiver buffer time-out detection function.
- All UART channels can be served by the PDMA controller.
- Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting DLY(UART_TMCTL[23:16]) register.
- Supports IrDA SIR function mode
- Supports LIN function mode.
- Supports RS-485 function mode.

5.15 Smart Card Host Interface (SC)

5.15.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

5.15.2 Features

- ISO-7816-3 T = 0, T = 1 compliant.
- EMV2000 compliant
- Up to two ISO-7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads.
- Programmable transmission clock frequency.
- Programmable receiver buffer trigger level.
- Programmable guard time selection (11 ETU ~ 267 ETU).
- A 24-bit and two 8 bit timers for Answer to Request (ATR) and waiting times processing.
- Supports auto inverse convention function.
- Supports transmitter and receiver error retry and error number limitation function.
- Supports hardware activation sequence process.
- Supports hardware warm reset sequence process.
- Supports hardware deactivation sequence process.
- Supports hardware auto deactivation sequence when detected the card removal.
- Supports UART mode
  - Half duplex, asynchronous communications.
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads.
  - Supports programmable baud rate generator for each channel.
  - Supports programmable receiver buffer trigger level.
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SC_EGTR register.
  - Programmable even, odd or no parity bit generation and detection.
  - Programmable stop bit, 1 or 2 stop bit generation.

5.16 I^2C

5.16.1 Overview

I^2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I^2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. Serial, 8-bit oriented bi-directional data transfers can be made up to 1 Mbps.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a

byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte.

A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL.

The controller's on-chip I^2C logic provides the serial interface that meets the I^2C bus standard mode specification. The I^2C controller handles byte transfers autonomously. Pull up resistor is needed for I^2C operation as these are open drain pins.

The I^2C controller is equipped with two slave address registers. The contents of the registers are irrelevant when I^2C is in Master mode. In the Slave mode, the seven most significant bits must be loaded with the user's own slave address. The I^2C hardware will react if the contents of I2CADDR are matched with the received slave address.

This controller supports the "General Call (GC)" function. If the GCALL (I2CSADDR[0]) bit is set this controller will respond to General Call address (00H). Clear GC bit to disable general call function. When GCALL bit is set and the I^2C is in Slave mode, it can receive the general call address which is equal to 00H after master sends general call address to the I^2C bus, then it will follow status of GC mode. If it is in Master mode, the ACK bit must be cleared when it sends general call address of 00H to the I^2C bus.

The I^2C-bus controller supports multiple address recognition with two address mask register. When the bit in the address mask register is set to one, it means the received corresponding address bit is don't-care. If the bit is set to 0, that means the received corresponding register bit should be exact the same as address register.

5.16.2 Features

- Supports two I^2C channels and both of them can acts as Master or Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- One built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows.
- Programmable clock divider allows versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (Two slave addresses with mask option)

5.17 SPI

5.17.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. It is used to perform a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI controller can be configured as a master or a slave device.

The SPI controller supports wake-up function. When this chip stays in power-down mode, it can be waked up chip by off-chip device.

This controller supports variable serial clock for special application and 2 data channel transfer mode to connect 2 off-chip slave devices. The SPI controller also supports PDMA function to access the data buffer.

5.17.2 Features

- Up to two sets of SPI controllers
- Supports Master (max. 16 MHz) or Slave (max. 6 MHz) mode operation
- Supports 1 bit data channel and 2 bit data channel transfer mode
- Configurable bit length of a transaction from 8 to 32 bits and configurable transaction number up to 2 of a transfer in burst mode, so the maximum bit length is 64 bits for each data transfer in burst mode
- Supports MSB first or LSB first transfer sequence
- Two slave select lines supported in Master mode
- Configurable byte or word suspend mode
- Supports byte re-ordering function
- Supports variable serial clock in Master mode
- Provide Dual FIFO buffers
- Supports wake-up function
- Supports PDMA transfer
- Supports 3-wires, no slave select signal, bi-direction interface

5.18 I²S

5.18.1 Overview

The audio controller consists of I²S protocol to interface with external audio CODEC. Two 8 word deep FIFO for receiving path and transmitting path respectively and is capable of handling 8-, 16-, 24-, 32-bit word sizes. PDMA controller handles the data movement between FIFO and memory.

5.18.2 Features

- Support Master mode and Slave mode
- Capable of handling 8-, 16-, 24- or 32-bit word sizes
- Supports monaural and stereo audio data
- Supports I²S and MSB justified data format
- Provides two 8-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Support PDMA transfer

5.19 USB

5.19.1 Overview

The USB controller is a USB 2.0 full-speed device controller. It is compliant with USB 2.0 full speed device specification and supports control/bulk/interrupt/isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There is an internal 512-byte SRAM as data buffer in this controller. For IN token or OUT token transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface. Users need to allocate the effective starting address of SRAM for each endpoint buffer through “buffer segmentation register (BUFSEG)”.

This device controller contains 6 configurable endpoints. Each endpoint can be configured as IN or OUT endpoint. The function address of the device and endpoint number in each endpoint shall be configured properly in advance for receiving or transmitting a data packet correctly. The transmitting/receiving length in each endpoint is defined in maximum payload register (MXPLD) and the handshakes between Host and Device are also handled by it.

There are four different interrupt events in this controller. They are the wake-up function, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USB_INTSTS) to acknowledge what kind of events occurring, and then check the related USB Endpoint Status Register (USB_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disable function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables the DRVSE0 bit (USB_DRVSE0), the USB controller will force USB_DP and USB_DM to level low and USB device function is disabled (disconnected). After disable the DRVSE0 bit, host will enumerate the USB device again.

Reference: Universal Serial Bus Specification Revision 2.0

5.19.2 Features

This Universal Serial Bus (USB) performs a serial interface with a single connector type for attaching all USB peripherals to the host system. Following is the feature listing of this USB.

- Compliant with USB 2.0 Full-Speed specification.
- Provide 1 interrupt vector with 4 different interrupt events (WAKEUP, FLDET, USB and BUS).
- Supports Control/Bulk/Interrupt/Isochronous transfer type.
- Supports suspend function when no bus activity existing for 3 ms.
- Provide 6 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types
- 512-byte SRAM buffer inside
- Provide remote wake-up capability.

5.20 Analog to Digital Converter (ADC)

5.20.1 Overview

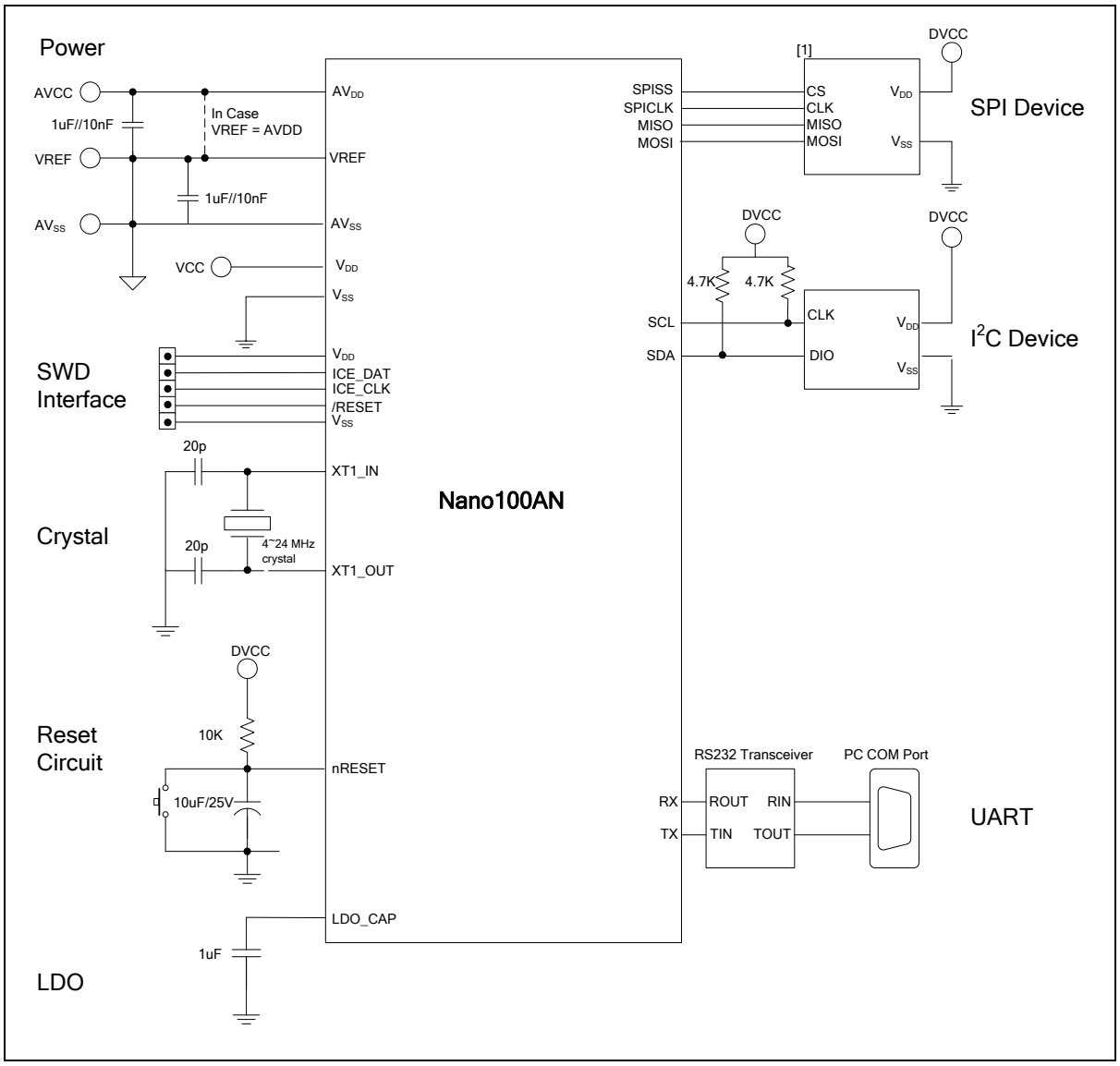
The Nano100 series contains one 12-bit successive approximation analog-to-digital converters (SAR A/D converter) with 8 external input channels and 1 internal channel. The A/D converter supports three operation modes: single, single-cycle scan and continuous scan mode, and can be started by software, external STADC/PB.8 pin, timer event start.

Note that the I/O pins used as ADC analog input pins must configure the Pin Function (PA_L_MFP) to ADC input and off digital function (GPIOA_OFFD) should be turned on before ADC function is enabled.

5.20.2 Features

- Analog input voltage range: 0~Vref (Max to 3.6V).
- 12-bit resolution and 8-bits accuracy is guaranteed.
- Up to 8 external analog input channels (channel0 ~ channel7), and 1 internal channel (channel10) converting four voltage sources (internal band-gap voltage, internal temperature sensor output, AVDD, and AVSS).
- Maximum ADC clock frequency is 16 MHz and each conversion is 21 clocks.
- Three operating modes
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Single-cycle scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel.
  - Continuous scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion.
- An A/D conversion can be started by
  - Software write 1 to ADST bit
  - External pin STADC
  - Selects one from four timer events (TMR0, TMR1, TMR2 and TMR3) that enable ADC and transfer AD results by PDMA
- Conversion results are held in data registers for each channel
- Supports data registers to hold conversion results for each channel.
- Supports A/D conversion End interrupt to indicate the end of A/D conversion.
- Supports two digital comparators to compare conversion result with a specified value.
- Supports digital comparator interrupt to indicate that conversion result meets setting condition.

6 APPLICATION CIRCUIT



7 ELECTRICAL CHARACTERISTIC

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD} V_{SS}	-0.3	+3.6	V
Input Voltage on five-volt tolerance pin	V_{IN}	V_{SS} -0.3	5.5	V
Input Voltage on any other pin without five-volt tolerance pin	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+85	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into VDD		-	150	mA
Maximum Current out of VSS		-	150	mA
Maximum Current sunk by a I/O pin		-	25	mA
Maximum Current sourced by a I/O pin		-	25	mA
Maximum Current sunk by total I/O pins		-	100	mA
Maximum Current sourced by total I/O pins		-	100	mA

Note: GPIO supports input 5V tolerance except ADC shared pins, PC.6 and PC.7.

7.2 DC Electrical Characteristics

(V_{DD}-V_{SS}=3.3V, T_A = 25°C, F_{OSC} = 32 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	1.8	-	3.6	V	V_{DD} =1.8V up to 32 MHz
Power Ground	V_{SS} AV_{SS}	-0.3	-		V	
LDO Output Voltage	V_{LDO1}	1.62	1.8	1.98	V	MCU operating in run or Idle mode
	V_{LDO2}		1.66		V	MCU operating in Power-down mode
Analog Operating Voltage	AV_{DD}		V_{DD}		V	
Operating Current Run Mode @ XTAL 12MHz, HCLK = 32 MHz	I_{DD1}		14		mA	V_{DD} = 3.6V@32MHz, enable all IP and PLL
	I_{DD2}		7.5		mA	V_{DD} = 3.6V@32MHz disable all IP and enable PLL
	I_{DD3}		12		mA	V_{DD} = 1.8V@32MHz enable all IP and PLL
	I_{DD4}		7		mA	V_{DD} = 1.8V@32MHz disable all IP and enable PLL
Operating Current Run Mode @ XTAL 12MHz, HCLK = 12MHz	I_{DD5}		5		mA	V_{DD} = 3.6V@12MHz, enable all IP and disable PLL
	I_{DD6}		2.5		mA	V_{DD} = 3.6V@12MHz, disable all IP and disable PLL
	I_{DD7}		4		mA	V_{DD} = 1.8V@12MHz, enable all IP and disable PLL
	I_{DD8}		2		mA	V_{DD} = 1.8V@12MHz, disable all IP and disable PLL
Operating Current Run Mode @ IRC 12MHz, HCLK = 12MHz	I_{DD9}		6		mA	V_{DD} = 3.6V@12MHz, enable all IP and disable PLL
	I_{DD10}		2.3		mA	V_{DD} = 3.6V@12MHz, disable all IP and disable PLL
	I_{DD11}		5.7		mA	V_{DD} = 1.8V@12MHz, enable all IP and disable PLL
	I_{DD12}		2.2		mA	V_{DD} = 1.8V@12MHz, disable all IP and disable PLL

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Current Run Mode @ XTAL 4MHz, HCLK = 4MHz	I_{DD13}		2.2		mA	V_{DD} = 3.6V@4MHz, enable all IP and disable PLL
	I_{DD14}		1.1		mA	V_{DD} = 3.6V@4MHz, disable all IP and disable PLL
	I_{DD15}		2		mA	V_{DD} = 1.8V@4MHz, enable all IP and disable PLL
	I_{DD16}		1		mA	V_{DD} = 1.8V@4MHz, disable all IP and disable PLL
Operating Current Run Mode @ XTAL 32.768 kHz, HCLK = 32.768 kHz	I_{DD17}		90		uA	V_{DD} = 3.6V@32.768 kHz enable all IP and disable PLL,
	I_{DD18}		80		uA	V_{DD} = 3.6V@32.768 kHz disable all IP and disable PLL
	I_{DD19}		75		uA	V_{DD} = 1.8V@32.768 kHz enable all IP and disable PLL
	I_{DD20}		72		uA	V_{DD} = 1.8V@32.768kHz disable all IP and disable PLL
Operating Current Run Mode @ IRC 10kHz, HCLK = 10kHz	I_{DD21}		80		uA	V_{DD} = 3.6V@10kHz enable all IP and disable PLL
	I_{DD22}		75		uA	V_{DD} = 3.6V@10kHz disable all IP and disable PLL
	I_{DD23}		67		uA	V_{DD} = 1.8V@10kHz enable all IP and disable PLL
	I_{DD24}		65		uA	V_{DD} = 1.8V@10kHz disable all IP and disable PLL
Operating Current Idle Mode @ XTAL 12MHz, HCLK = 32MHz	I_{IDLE1}		10.5		mA	V_{DD}= 3.6V@32MHz enable all IP and PLL,
	I_{IDLE2}		4.2		mA	V_{DD}=3.6V@32MHz disable all IP and enable PLL
	I_{IDLE3}		9		mA	V_{DD} = 1.8V@32MHz enable all IP and PLL
	I_{IDLE4}		4		mA	V_{DD} = 1.8V@32MHz disable all IP and enable PLL
Operating Current Idle Mode @ XTAL 12MHz, HCLK = 12MHz	I_{IDLE5}		3.3		mA	V_{DD} = 3.6V@12MHz, enable all IP and disable PLL
	I_{IDLE6}		0.7		mA	V_{DD} = 3.6V@12MHz, disable all IP and disable PLL
	I_{IDLE7}		3		mA	V_{DD} = 1.8V@12MHz, enable all IP and disable PLL

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{IDLE8}		0.7		mA	V_{DD} = 1.8V@12MHz, disable all IP and disable PLL
Operating Current Idle Mode @ IRC 12MHz, HCLK = 12MHz	I_{IDLE9}		4.5		mA	V_{DD} = 3.6V@12MHz, enable all IP and disable PLL
	I_{IDLE10}		0.7		mA	V_{DD} = 3.6V@12MHz, disable all IP and disable PLL
	I_{IDLE11}		4.2		mA	V_{DD} = 1.8V@12MHz, enable all IP and disable PLL
	I_{IDLE12}		0.7		mA	V_{DD} = 1.8V@12MHz, disable all IP and disable PLL
Operating Current Idle Mode @ XTAL 4MHz, HCLK = 4MHz	I_{IDLE13}		1.7		mA	V_{DD} = 3.6V@4MHz, enable all IP and disable PLL
	I_{IDLE14}		0.6		mA	V_{DD} = 3.6V@4MHz, disable all IP and disable PLL
	I_{IDLE15}		1		mA	V_{DD} = 1.8V@4MHz, enable all IP and disable PLL
	I_{IDLE16}		0.5		mA	V_{DD} = 1.8V@4MHz, disable all IP and disable PLL
Operating Current Idle Mode @ XTAL 32.768kHz, HCLK = 32.768kHz	I_{IDLE17}		85		uA	V_{DD} = 3.6V@ 32.768kHz enable all IP and disable PLL
	I_{IDLE18}		75		uA	V_{DD} = 3.6V@ 32.768kHz disable all IP and disable PLL
	I_{IDLE19}		70		uA	V_{DD} = 1.8V@ 32.768kHz enable all IP and disable PLL
	I_{IDLE20}		65		uA	V_{DD} = 1.8V@ 32.768kHz disable all IP and disable PLL
Operating Current Idle Mode @ IRC 10kHz, HCLK = 10kHz	I_{IDLE21}		80		uA	V_{DD} = 3.6V@ 10kHz enable all IP and disable PLL
	I_{IDLE22}		75		uA	V_{DD} = 3.6V@ 10kHz disable all IP and disable PLL
	I_{IDLE23}		65		uA	V_{DD} = 1.8V@ 10kHz enable all IP and disable PLL
	I_{IDLE24}		63		uA	V_{DD} = 1.8V@ 10kHz disable all IP and disable PLL
Standby Current Power-down Mode	I_{PWD1}		1.5		μA	V_{DD} = 3.6V, RTC OFF, all clock stop With RAM Retenstion, IO no loading

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
	I_{PWD2}		1.0		μA	V_{DD} = 1.8V, RTC OFF, all clock stop With RAM Retenstion, IO no loading
	I_{PWD3}		3		μA	V_{DD} = 3.6V, RTC ON, all clock stop except 32.768kHz With RAM Retenstion, IO no loading
	I_{PWD4}		2.5		μA	V_{DD} = 1.8V, RTC ON, all clock stop except 32.768kHz With RAM Retenstion, IO no loading
Input Pull Up Resistor PA, PB, PC, PD, PE, PF	R_{IN}		40		KΩ	V_{DD} = 3.3V
			98		KΩ	V_{DD} = 1.8V
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-0.1	-	+0.1	μA	V_{DD} = 3.3V, 0<V_{IN}<V_{DD}
Input Low Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IL1}		-	0.4V_{DD}	V	
Input High Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IH1}	0.6V_{DD}		5.5	V	ADC shared pins, PC.6 and PC.7 without Input 5V tolerance.
Hysteresis voltage of PA~PF (Schmitt input)	V_{HY}		0.2V_{DD}		V	
Input Low Voltage XT1[*2]	V_{IL2}	0	-	0.4		V_{DD} = 3.3V
Input High Voltage XT1[*2]	V_{IH2}	2.4	-	V_{DD} +0.2	V	V_{DD} = 3.3V
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.3	V	
Input High Voltage X32I[*2]	V_{IH4}	1.5	-	1.98	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	1.28	1.33	1.37	V	V_{DD} = 3.3V
Positive going threshold (Schmitt input), /RESET	V_{IHS}	1.75	1.98	2.25	V	V_{DD} = 3.3V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-10	-14	-	mA	V_{DD} = 3.3V, V_S = Vdd-0.7V
	I_{SR22}	-4.06	-6.5	-	mA	V_{DD} = 1.8V, V_S = Vdd-0.45V
Sink Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SK1}	16	19	-	mA	V_{DD} = 3.3V, V_S = 0.7V
	I_{SK1}	4.14	6.97	-	mA	V_{DD} = 1.8V, V_S = 0.45V

Note:

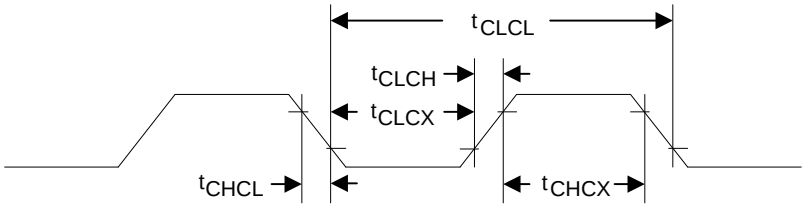
1. /RESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.

3. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.
4. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest VSS pin of the device. Also a 100nF bypass capacitor between LDO and VSS help suppressing output noise

7.3 AC Electrical Characteristics

7.3.1 External Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Clock High Time	t_{CHCX}	10	-		nS	
Clock Low Time	t_{CLCX}	10	-		nS	
Clock Rise Time	t_{CLCH}	2	-	15	nS	
Clock Fall Time	t_{CHCL}	2	-	15	nS	



7.3.2 External 4~24 MHz XTAL Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{HXTAL}	4	12	24	MHz	VDD = 1.8V ~ 3.6V
Temperature	T_{HXTAL}	-40	-	+85	°C	
Operating current	I_{HXTAL}		0.3		mA	VDD = 3.0V

7.3.2.1 *Typical Crystal Application Circuits*

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	Optional(Depend on crystal specification)		without

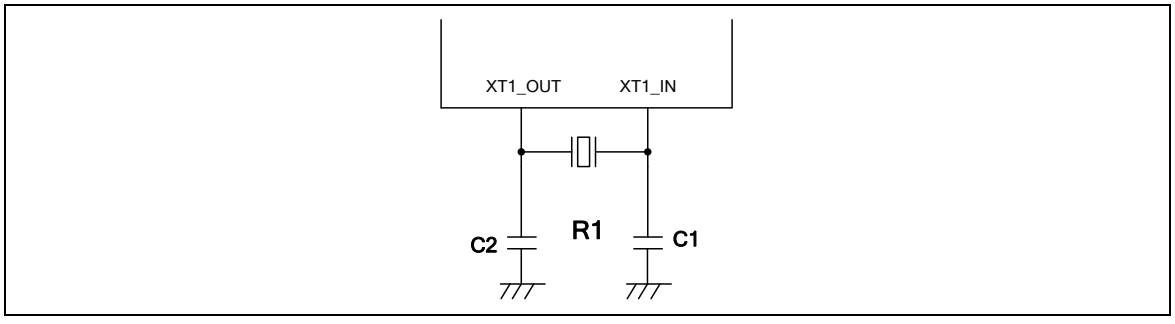


Figure 7-1 Typical Crystal Application Circuit

7.3.3 External 32.768 kHz Crystal

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	fL_{XTAL}		32.768		kHz	VDD = 1.8V ~ 3.6V
Temperature	TL_{XTAL}	-40	-	+85	°C	
Operating current	I_{HXTAL}		1.2		μA	VDD = 3.0V

7.3.4 Internal 12 MHz Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{HRC}		1.8		V	
Calibrated Internal Oscillator Frequency	F_{HRC}	11.88	12	12.12	MHz	25°C, V_{DD} = 3V
		10.8	12	13.2	MHz	-40°C~+85 °C, V_{DD} = 1.8V~3.6V
		11.88	12	12.12	MHz	-40°C~+85 °C, V_{DD} = 1.8V~3.6V Enable 32.768K crystal oscillator and set TRIM_SEL[1:0]=”10”
Operating current	I_{HRC}		TBD		mA	

Note: Internal oscillator operation voltage comes from LDO.

7.3.5 Internal 10 kHz Oscillator

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{LRC}		1.8		V	
Center Frequency	F_{LRC}	7	10	13	kHz	25°C, V_{DD} = 3V
		5	10	15	kHz	-40°C~+85 °C, V_{DD} = 1.8V~3.6V
Operating current	I_{LRC}		0.7		μA	V_{DD} = 3V

Note: Internal oscillator operation voltage comes from LDO.

7.4 Analog Characteristics

7.4.1 12-bit ADC

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV_{DD}	2.0		3.6	V	$AV_{DD} = V_{DD}$
Operating current	I_{ADC}		TBD		mA	$AV_{DD} = V_{DD} = 3.0V$
Resolution	R_{ADC}			12	Bit	
Reference voltage	V_{REF}	1.5		A_{VDD}	V	
Reference input current (Avg.)	I_{REF}		320		μA	
ADC input voltage	V_{IN}	0		V_{REF}	V	
Conversion time	T_{CONV}	1.25			μS	
Sampling Rate	F_{SPS}			800K	Hz	$V_{DD} = 3V$
Integral Non-Linearity Error	INL		±4	±8	LSB	
Differential Non-Linearity	DNL		-1~+4	-1~+8	LSB	
Gain error	E_G		±16		LSB	
Offset error	E_{OFFSET}		±4		LSB	
Absolute error	E_{ABS}		-	±16	LSB	
ADC Clock frequency	F_{ADC}	0.25		16	MHz	
Clock cycle	AD_{CYC}	21			Cycle	
Internal Capacitance	C_{IN}	-	3.2	-	pF	
Internal Resistance	R_{IN}	-	200	-	Ω	
Monotonic	-	Guaranteed			-	

7.4.2 Brown-out Detector

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{BOD}	1.8		3.6	V	
Quiescent current	I_{BOD}		1		μA	$AV_{DD} = 3.0V$, BOD enabled
BOD17 detection level	V_{B17dt1}	1.6	1.7	1.8	V	25°C
	V_{B17dt2}	1.5	1.7	1.9	V	-40~85°C
BOD20 detection level	V_{B20dt1}	1.9	2.0	2.1	V	25°C
	V_{B20dt2}	1.8	2.0	2.2	V	-40~85°C
BOD25 detection level	V_{B25dt1}	2.4	2.5	2.6	V	25°C
	V_{B25dt2}	2.2	2.5	2.8	V	-40~85°C

7.4.3 Power-On Reset

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Reset voltage	V_{POR}	-	1.6	-	V	
Quiescent current	I_{POR}	-	1	-	nA	LDO output > Reset voltage

7.4.4 Temperature Sensor

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Detection Temperature	T_{DET}	-40		+125	^{o}C	
Operating current	I_{TEMP}	-	5	-	μA	
Gain	V_{TG}	-	-1.64	-	mV/^{o}C	
Offset	V_{TO}	-	750	-	mV	Tempeature at 0 ^{o}C

Note: Internal operation voltage comes form LDO.

7.4.5 Internal Voltage Reference

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV_{DD}	1.8	-	3.6	V	
1.5V voltage reference	V_{REF1}	-	1.5	-	V	AV_{DD} >= 1.8V
2.5V voltage reference	V_{REF2}	-	2.5	-	V	AV_{DD} >= 2.8V
Stable Time	T_{REFTAB}	-	1	-	ms	
Operating current	I_{VREF}	-	30	-	μA	AV_{DD} = 3V

7.4.6 USB PHY Specifications

7.4.6.1 *USB PHY DC Electrical Characteristics*

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input high (driven)		2.0	-		V
V_{IL}	Input low			-	0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2	-		V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8	-	2.5	V
V_{SE}	Single-ended receiver threshold		0.8	-	2.0	V
	Receiver hysteresis			200		mV

V_{OL}	Output low (driven)		0	-	0.3	V
V_{OH}	Output high (driven)		2.8	-	3.6	V
V_{CRS}	Output signal cross voltage		1.3	-	2.0	V
R_{PU}	Pull-up resistor		1.425	-	1.575	kΩ
R_{PD}	Pull-down resistor		14.25	-	15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0	-	3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND		-	20	pF

*Driver output resistance doesn't include series resistor resistance.

7.4.6.2 *USB PHY Full-Speed Driver Elevtrical Characteristics*

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{FR}	Rise Time	C_L=50p	4	-	20	ns
T_{FF}	Fall Time	C_L=50p	4	-	20	ns
T_{FRFF}	Rise and fall time matching	$T_{FRFF}=T_{FR}/T_{FF}$	90	-	111.11	%

7.4.6.3 *USB PHY Power Dissipation*

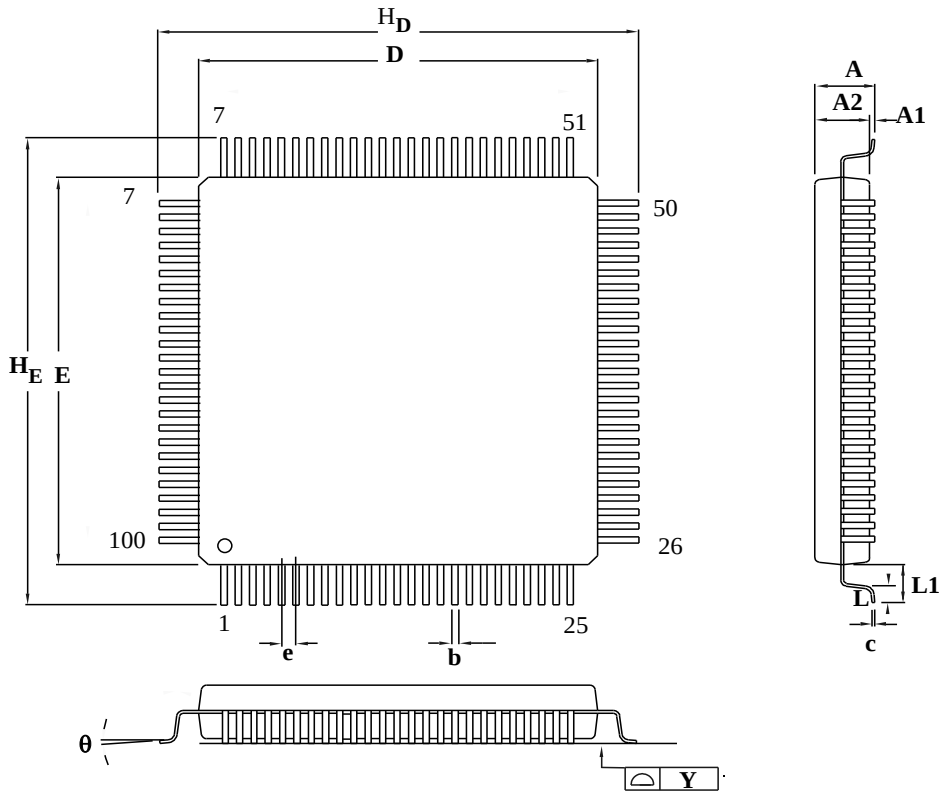
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{VDDREG} (Full Speed)	VDDD and VDDREG Supply Current (Steady State)	Standby		50		uA

7.4.6.4 *USB LDO DC Electrical Characteristics*

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VBUS				5		V
V33	Output voltage			3.3		V
Iop	Operation Current			100		uA

8 PACKAGE DIMENSIONS

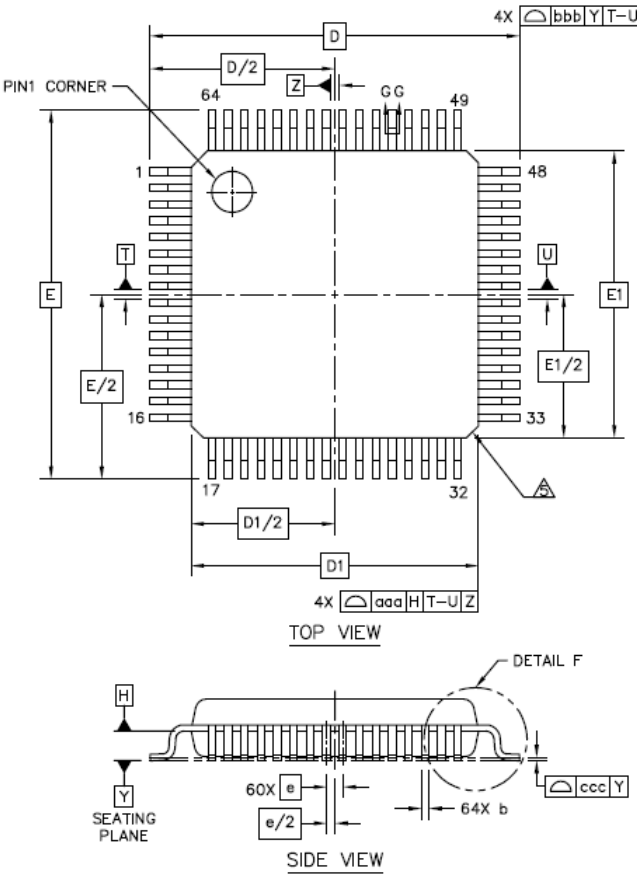
8.1 LQFP100 (14x14x1.4 mm footprint 2.0 mm)



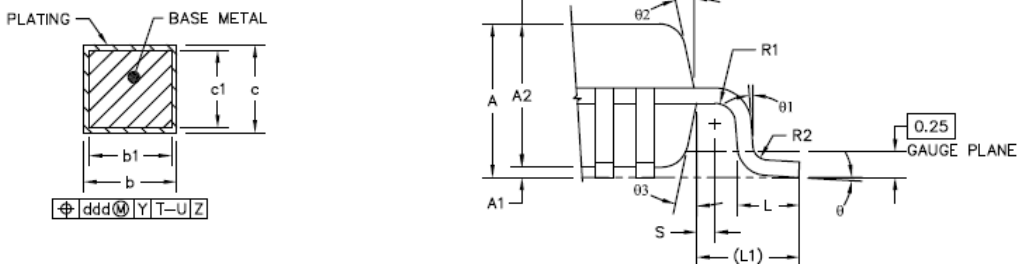
Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

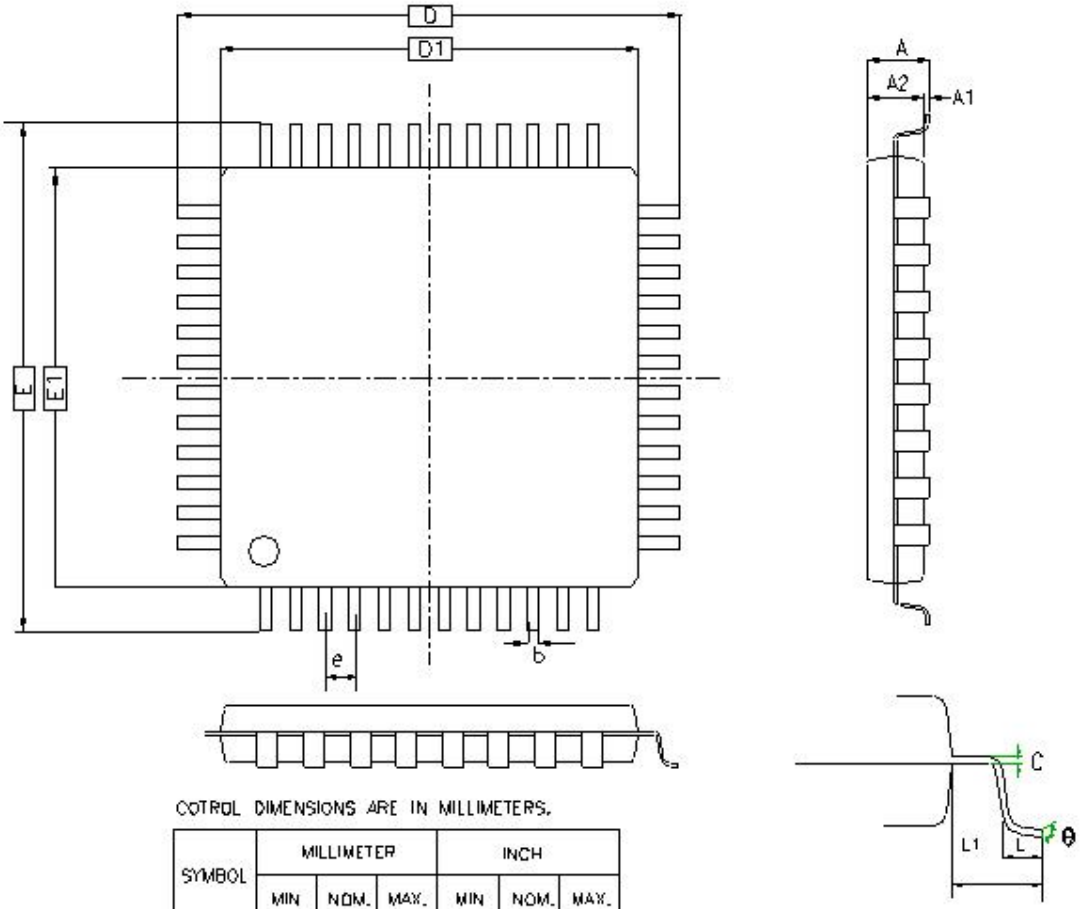
8.2 LQFP64 (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	9 BSC		
	Y	E	9 BSC		
BODY SIZE	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



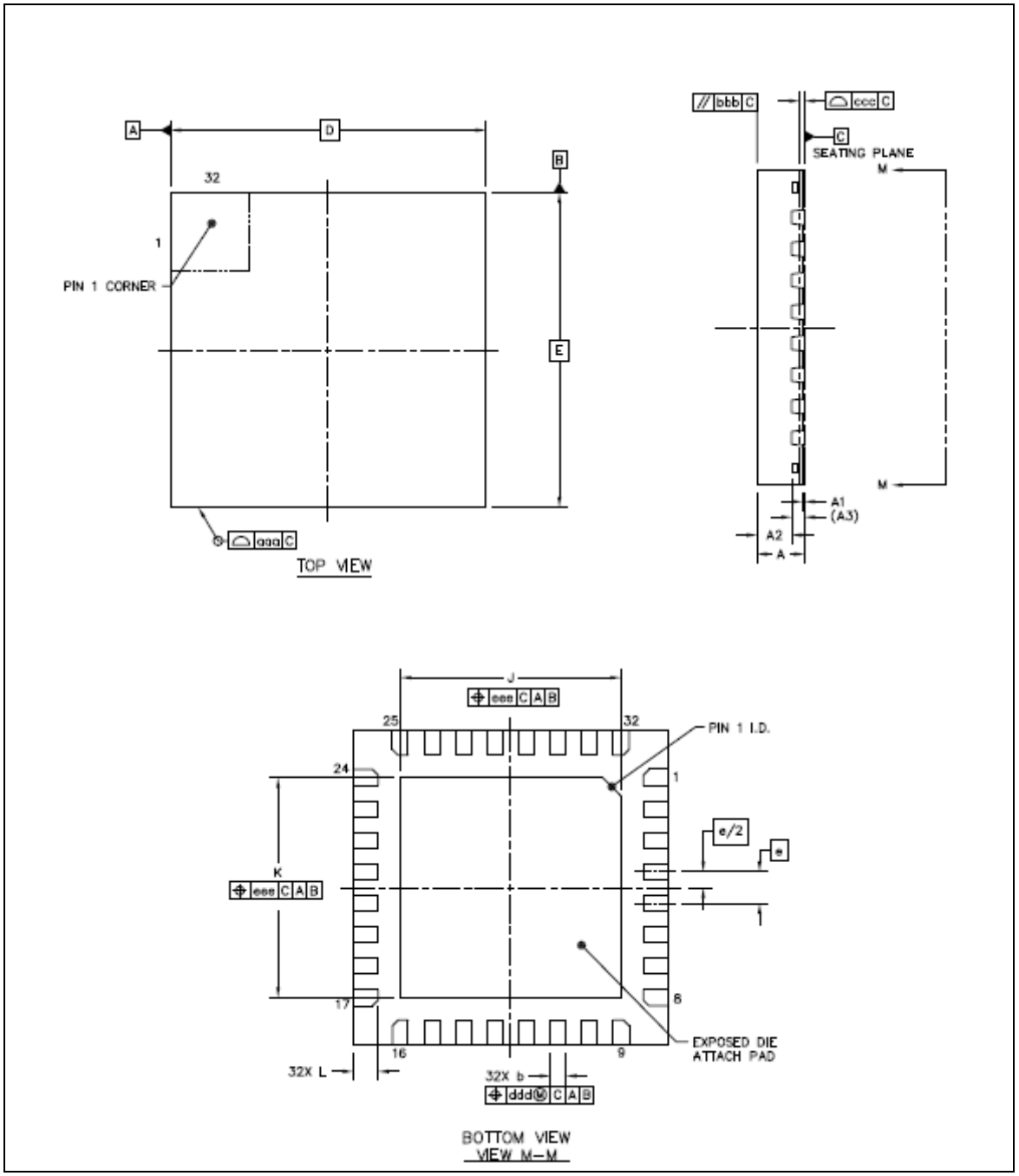
8.3 LQFP48 (7x7x1.4 mm footprint 2.0 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.280
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

8.4 QFN33 (5x5x0.8 mm footprint 0.5 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

9 REVISION HISTORY

Date	Revision	Description
2011.05.31	0.001	Initial release
2011.08.22	0.002	Modified the Electrical Characteristics section
2011.10.31	0.003	1. Changed the max SPI speed to 16 MHz 2. ADC pin without 5V tolerance 3. Modified the Electrical Characteristics section 4. Removed XT1_IN and XT1_OUT GPIO (PF.2/PF.3) shared function 5. Modified pin diagram and pin description 6. Removed timer continuous operation mode and UART wakeup function 7. Revised the product selection table 8. Fixed typos.
2011.12.31	0.004	1. Updated pin diagram and pin description 2. Updated the DC Electrical Characteristics section
2012.04.09	0.005	1. Removed UART1 shared function from pin-26 to pin-29 in NANO100 LQFP100 package 2. Added detailed description of “I2CINTSTS” register (I2Cx_BA + 0x04)
2013.06.27	0.006	1. Removed NANO110/NANO130 series information. 2. Updated Nano100 series selection code in section 3.1. 3. Updated Nano100 product selection guide in section 3.2. 4. Removed GPIOF[2] and GPIOF[3] of Multiple Function Port F in section 5.4.5. 5. Added a note “For GPIOF_PUEN, bits [15:6] and [3:2] are reserved” in section 5.8.6.
2013.07.30	0.007	1. Updated Nano100 product selection guide in section 3.2. 2. Added Nano100 QFN33 pin diagram and description in section 3.3.1.4 and 3.4.1.
2014.12.29	0.008	1. Updated Nano100 product selection guide in section 3.2. 2. Changed Timer0/1 Ch0/1 to Timer x (x=0, 1, 2, 3) in the Timer

		Controller section.
2015.03.31	1.00	1. Updated Electrical Characteristics TBD items in chapter 7. 2. Added Application Circuit in chapter 6. 3. Added a noto that “GPIO supports input 5V tolerance except ADC shared pins, PC.6 and PC.7” in section 7.1. 4. Updated the value of capacitor connected with LDO pin to be 1uF in section 7.2. 5. Updated external 4~24 MHz XTAL application circuit in section 7.3.4. 6. Updated 12-bit ADC characteristics in section 7.4.1. 7. Added Brown-out Detector characteristics in a full operating temperature range in section 7.4.2.

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