

High Performance, Single Synchronous Step-Up Controller

General Description

The uP6055 is a high-efficiency, single synchronous boost controller suitable for high power applications in Power Bank and E-Cigarette. The proprietary RCOT™ technology provides fast transient response and high noise immunity. It supports ceramic output capacitors. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 4V to 13V, and the conversion input voltage ranges is from 3V to 5.5V. The switching frequency is fixed 450kHz. It is available in a space saving VQFN3x3-16L package.

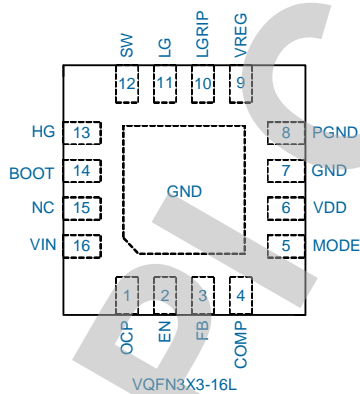
Ordering Information

Order Number	Package Type	Remark
uP6055PQAD	VQFN3x3-16L	
uP6055AQAD		

Note:

- (1) Please check the sample/production availability with uPI representatives.
- (2) uPI products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration



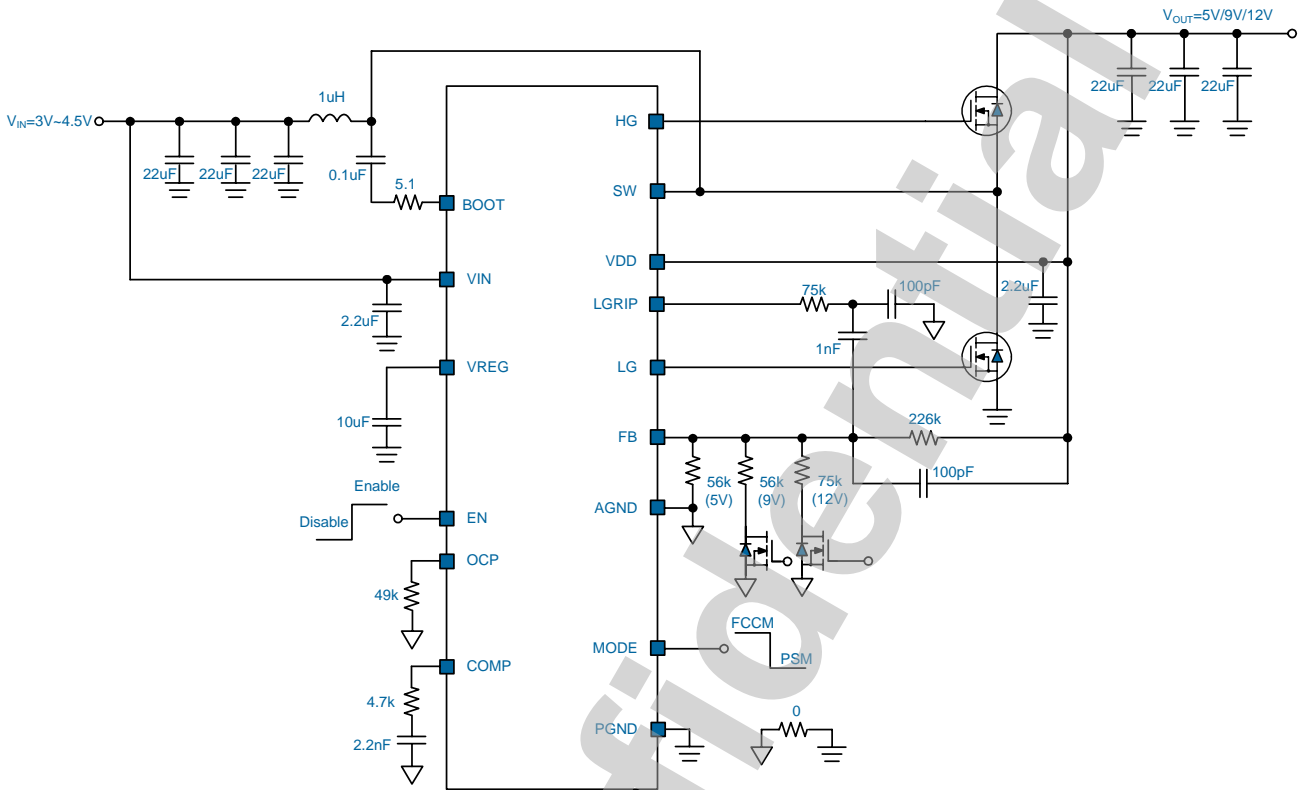
Features

- ❑ Wide Input Voltage Range: 3V to 5.5V
- ❑ Output Voltage Range: 4V to 13V
- ❑ Built-In 1% 1V Reference
- ❑ Built-In LDO Linear Voltage Regulator
- ❑ RCOT™ (Robust Constant On-Time) Control Architecture
- ❑ 450kHz Switching Frequency
- ❑ 4000ppm/°C $R_{DS(ON)}$ Current Sensing
- ❑ 8ms Soft Start
- ❑ Built-in OVP/UVP/OCP/OTP
- ❑ VQFN3x3-16L Package
- ❑ RoHS Compliant and Halogen Free

Applications

- ❑ Portable Charging Devices
- ❑ Power Bank
- ❑ I/O Supplies
- ❑ System Power Supplies

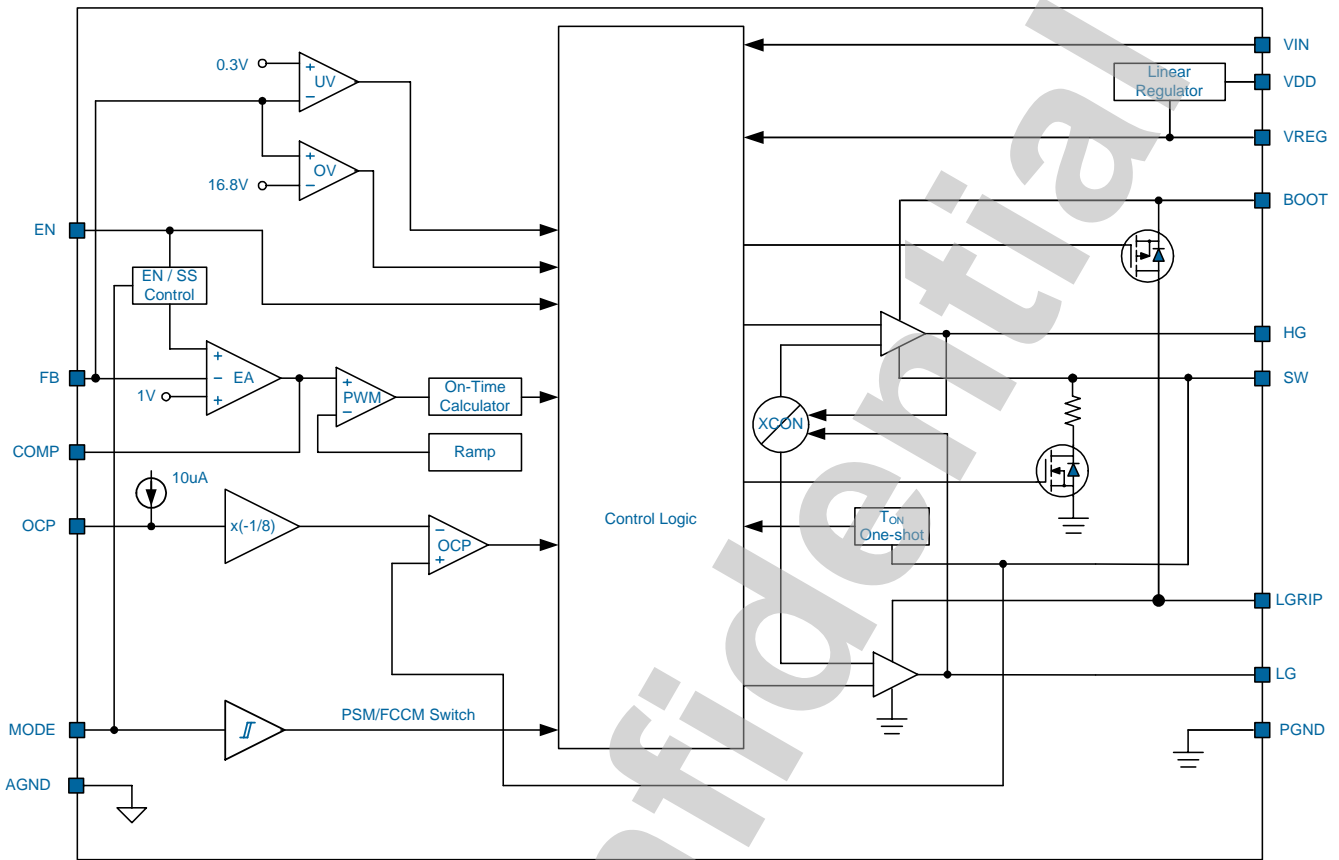
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	OCP	Over Current Protection Setting. Connect a resistor from this pin to GND to set the over current protection level.
2	EN	Chip Enable. Short to GND to disable the device.
3	FB	Feedback Input. This pin is the inverting input to the error amplifier. A resistor divider from output to GND is used to set regulator voltage.
4	COMP	Boost Controller Compensation. Connect a compensation network to ground.
5	MODE	Operation Mode Selection Pin for The Device in Light Load Condition. When this pin is connected to ground, the device works in Pulse-Skip mode. When this pin is pulled high, the device works in Force CCM mode.
6	VDD	Controller Power Supply Input. This pin provides bias voltage for the IC and powers the internal 5V linear regulators. Connect this pin to VOUT and bypass it with an R/C filter.
7	AGND	Signal Ground.
8	PGND	Controller Power GND Pin.
9	VREG	5V LDO Output and Gate Drive Supply Voltage Input.
10	LGRIP	Low Side Gate Driver Ripple Injection. Connect a series RC form LGRIP to GND and FB to compensate the control loop.
11	LG	Low Side Gate Driver Output. Connect this pin to an external lower MOSFET gate input.
12	SW	Switches Node. Connect this pin to the output inductor. Connect this pin to the source of the external upper MOSFET and the drain of the external lower MOSFET.
13	HG	High Side Gate Driver Output. Connect this pin to external upper MOSFET gate input.
14	BOOT	Bootstrap Supply for the Floating Upper MOSFET Gate Driver. Connect the bootstrap capacitor C_{BOOT} between BOOT pin and the SW pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET. Ensure that C_{BOOT} is placed near the IC.
15	NC	Not internally connected.
16	VIN	Power Supply Input. Input voltage that supplies current to the output voltage.

Functional Block Diagram



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Functional Description

The uP6055 implements a unique RCOT_{TM} control topology for the synchronous boost. The RCOT_{TM} supports extremely low ESR output capacitors and makes the design easier and robust. The output voltage ranges from 4V to 13V. The conversion input voltage ranges from 3V up to 5.5V.

Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

The uP6055 has a MODE pin to select between Force CCM and Pulse-Skip for light load conditions. The strong gate drivers allow low R_{DS(ON)} FETs for high-current applications.

Enable and Soft Start

When the EN pin voltage rises above the enable threshold voltage (typically 1.8V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 5V at the VREG pin. In the second phase, an internal DAC starts ramping up the reference voltage from 0V to 1V. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

On-Time Control and Frequency

The uP6055 does not have a dedicated oscillator that determines switching frequency. However, the device runs with pseudo-constant frequency by feed-forwarding the input and output voltages into its on-time one-shot timer. The RCOT_{TM} control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage. This makes the switching frequency fairly constant in steady state conditions over wide input voltage range.

The off-time is modulated by a PWM comparator. The FB node voltage (the mid-point of resistor divider) is compared to the internal 1V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a set signal to terminate the off-time (turn off the low-side MOSFET and turn on high-side MOSFET). The set signal is valid if the inductor current level is below the OCP threshold, otherwise the off-time is extended until the current level falls below the threshold.

Light Load Condition in Pulse-Skip Operation

While the MODE pin is connected to ground, uP6055 automatically reduces the switching frequency at light load conditions to maintain high efficiency. This reduction of the frequency is achieved smoothly and without increasing VOUT ripples or load regulation. As the load current is further decreased, it takes longer time to discharge the output capacitor to the level than requires the next ON cycle.

The transition pin from discontinuous to continuous conduction mode can be calculated as:

$$I_{OUT} = \frac{1}{2 \times f_{OSC} \times L_{OUT}} \times \frac{V_{IN}^2}{V_{OUT}} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

Over Current Limit

the uP6055 monitors the inductor peak current by low side MOSFET R_{DS(ON)} when it turns on. The over current limit is triggered once the sensing current level is higher than V_{OCSET}. When triggered, the over current limit will keep low side MOSFET off even the voltage loop commands it to turn on.

The output voltage will decrease if the load continuously demands more current than current limit level and consequently causes V_{OUT} to decrease faster until UVP occurs and shuts down the uP6055.

The peak current limit threshold is set by connecting a resistor from OCP to GND. The OCP pin will source a 10uA current and create a voltage drop across R_{OCP} as the V_{OCSET}. V_{OCSET} = 10uA × R_{OCP}. When the voltage drop across the low side MOSFET equals the voltage across the setting resistor, the peak current limit will be activated.

The voltage across LX and GND pins is compared with V_{OCSET} for current limit. The peak current limit level is calculated as:

$$I_{PEAK_LIM} = \frac{V_{OCSET}}{8 \times R_{DS(ON)}} + \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the peak-to-peak inductor ripple current at steady state.

Over Voltage/Under Voltage Protection

The uP6055 monitors output voltage to detect over voltage and under voltage. When the output voltage becomes higher than 16.8V, the OVP is triggered, low side MOSFET is off and the high side MOSFET is on. When the feedback voltage is lower than 0.3V, the UVP is triggered, then high side MOSFET and low side MOSFET are latched. This function is enabled after 13.5ms following EN has become high.

UVLO Protection

The uP6055 uses VIN under voltage lockout protection (UVLO). When the VIN voltage is lower than the UVLO threshold voltage, the switch mode power supply shuts off. This is non-latch protection.

Over Temperature Protection

The uP6055 monitors the temperature of itself. If the temperature exceeds typical 130°C, the uP6055 will be turned off. This is the non-latch protection. It will be recovered once temperature is lower than 100°C.

Absolute Maximum Rating

(Note 1)

Supply Voltage, VDD	-----	-0.3V to +26V
SW Pin Voltage to GND	-----	-0.3V to (VOUT+ -0.3V)
BOOT Pin Voltage	-----	$V_{SW} - 0.3V$ to $V_{SW} + 6V$
HG Pin Voltage	-----	$V_{SW} - 0.3V$ to $V_{SW} + 6V$
LG Pin Voltage	-----	-0.3V to +6V
VIN and VREG Pin Voltage	-----	-0.3V to +6V
Other Pins to GND	-----	-0.3V to +6V
Storage Temperature Range	-----	-55°C to +150°C
Lead Temperature (Soldering, 10 sec)	-----	260°C
ESD Rating (Note 2)		
HBM (Human Body Mode)	-----	2kV
MM (Machine Mode)	-----	200V

Thermal Information

Package Thermal Resistance (Note 3)

VQFN3x3-16L θ_{JA}	-----	68°C/W
VQFN3x3-16L θ_{JC}	-----	6°C/W
Power Dissipation, P_D @ $T_A = 25^\circ C$		
VQFN3x3-16L	-----	1.47W

Recommended Operation Conditions

(Note 4)

Input Voltage, V_{IN}	-----	3V to 5.5V
Output Voltage, V_{OUT}	-----	4V to 13V
Operating Junction Temperature Range	-----	-40°C to +125°C
Operating Ambient Temperature Range	-----	-40°C to +85°C

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at $T_A = 25^\circ C$ on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

($V_{DD} = 5V, T_A = 25^\circ C$, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Power Supply						
VIN UVLO Threshold	$V_{UVLOVIN}$	Rising	2.83	2.9	2.97	V
		Hysteresis	0.15	0.2	0.25	V
VIN Supply Current	I_{VIN}	$V_{EN} = 5V, V_{FB} = 1.1V, I_{OUT} = \text{No Load}$	--	360	--	μA
VDD Supply Current	I_{VDD}	$V_{EN} = 5V, V_{FB} = 1.1V, I_{OUT} = \text{No Load}$	--	0.6	1	mA
VIN Shutdown Current	I_{VIN_SD}	$V_{EN} = 0V, I_{OUT} = \text{No Load}$	--	--	10	μA
VDD Shutdown Current	I_{VDD_SD}	$V_{EN} = 0V, I_{OUT} = \text{No Load}$	--	--	1	μA
Internal Reference Voltage						
Feedback Voltage	V_{FB}	CCM condition, $T_A = 25^\circ C$	0.99	1	1.01	V
FB Input Current	I_{FB}	$V_{FB} = 1V, T_A = 25^\circ C$	--	0.01	0.2	μA
Output Drivers						
Upper Switch Resistance	R_{HGATE}	Source, $I_{HGATE} = -150mA$	1.2	2	3	Ω
		Sink, $I_{HGATE} = -150mA$	0.6	1	1.8	
Lower Switch Resistance	R_{LGATE}	Source, $I_{LGATE} = -150mA$	0.6	1	2.2	Ω
		Sink, $I_{LGATE} = -150mA$	0.4	0.7	1.2	
Dead Time	T_D	HGATE-off to LGATE-on	7	17	30	ns
		LGATE-off to HGATE-on	10	22	35	
VFB of VOUT Discharge	V_{FB_DIS}	VOUT discharge	--	1.1	--	V
		Hysteresis	--	0.05	--	
Duty and Frequency Control						
Minimum Off-time	T_{OFF_MIN}		--	700	--	ns
Minimum On-Time	T_{ON_MIN}	$V_{IN} = 3.8V, V_{OUT} = 5V$	--	240	--	ns
Frequency	F_{SW}		--	450	--	kHz
Soft Start						
Soft Start Time	T_{SS}	From VEN high to VOUT = 95%	--	8	--	ms
Logic Threshold						
EN Pin Threshold Voltage	V_{EN}	Enable	1.8	--	--	V
		Disable	--	--	0.5	
On-Time	T_{ON}	$R_{RT} = \text{open}, f_{LX} = 450kHz$ $V_{IN} = 3.7V, V_{OUT} = 9V, I_{OUT} = \text{No Load}$	--	1.22	--	μs
EN Input Current	I_{EN}	$V_{EN} = 5V$	--	--	1	μA
Protection: Current Sense						
OCP Source Current	I_{CS}	$V_{OCP} = 1V$	9	10	11	μA
		Temp coef	--	4000	--	ppm/ $^\circ C$

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection: UVP and OVP						
OVP Threshold Voltage	V_{OVP}	VDD	15.8	16.8	17.8	V
UVP Threshold Voltage	V_{UVP}	FB	--	0.3	--	V
UVP Propagation Delay Time	T_{UVPDEL}		--	3.3	--	ms
Output UVP Delay Time	T_{UVPEN}	From Enable to UVP Workable	--	13.5	--	ms
VREG LDO Voltage						
LDO Output Voltage	V_{REG}		4.625	5.0	5.375	V
LDO Output Current	I_{REG}		--	--	50	mA
LDO Drop Out Voltage	V_{DROP}	VDD = 4.5V, $I_{REG} = 20mA$	--	300	--	mV
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SDN}	Shutdown Temperature	--	130	--	°C
		Hysteresis	--	30	--	

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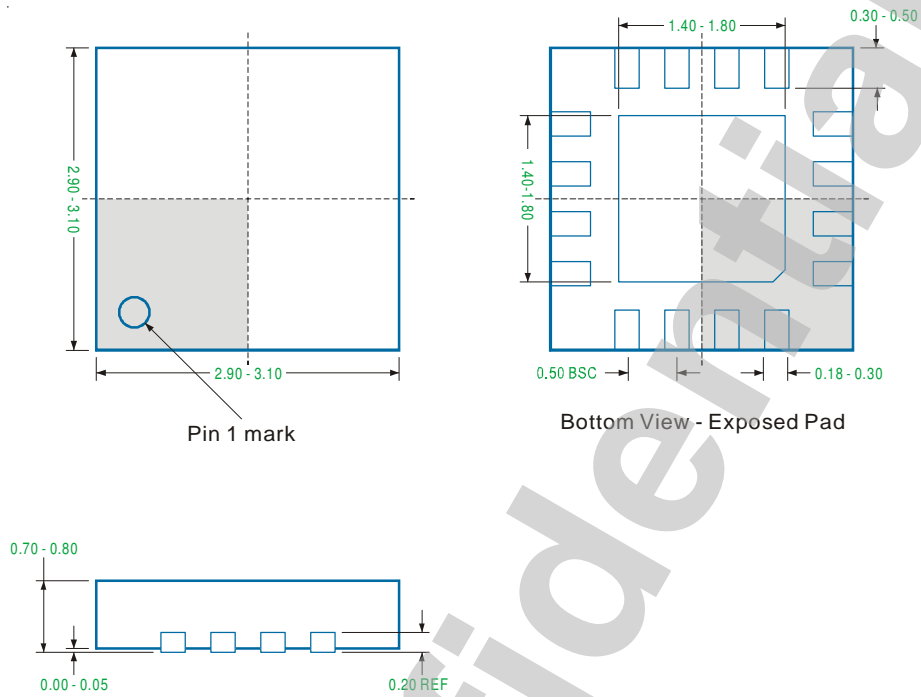
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VQFN3x3 - 16L



Note

1. Package Outline Unit Description:

BSC: Basic. Represents theoretical exact dimension or dimension target

MIN: Minimum dimension specified.

MAX: Maximum dimension specified.

REF: Reference. Represents dimension for reference use only. This value is not a device specification.

TYP: Typical. Provided as a general value. This value is not a device specification.

2. Dimensions in Millimeters.

3. Drawing not to scale.

4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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