0.5 Micron Sea of Gates

Introduction

The MG2 series is a 0.5 micron, array based, CMOS product family. Several arrays up to 700k cells cover all system integration needs. The MG2 is manufactured using SCMOS3/2, a 0.5 micron drawn, 3 metal layers CMOS process.

The MG2 series base cell architecture provides high routability of logic with extremely dense compiled memories : RAM, DPRAM and FIFO. ROM can be generated using synthesis tools. For instance, the largest array is capable of integrating 128K bits of DPRAM with 128K bits of ROM and over 300,000 random gates.

Accurate control of clock distribution can be achieved by PLL hardware and CTS (Clock Tree Synthesis) software. New noise prevention techniques are applied in the array and in the periphery : Three or more independent supplies, internal decoupling, customisation dependent supply routing, noise filtering, skew controlled I/Os, low swing differential I/Os, all contribute to improve the noise immunity and reduce the emission level.

The MG2 is supported by an advanced software environment based on industry standards linking proprietary and commercial tools. Cadence, Mentor, Synopsys and VHDL are the reference front end tools. Floor planning associated with timing driven layout provides a short back end cycle.

The MG2 family continues the TEMIC offering in array based commercial, industrial and military circuits.

Features

- Full Range of Matrices up to 700k Cells
- 0.5 µm Drawn CMOS, 3 Metal Layers, Sea of Gates
- RAM, DPRAM, FIFO Compilers
- Library Optimised for Synthesis, Floor Plan & Automatic Test Generation (ATG)
- High Speed Performances :
  - 200 ps Typical Gate Delay @5 V
  - typical 625 MHz Toggle Frequency @5 V and 360 MHz @3.3 V
- High System Frequency Skew Control :
  - 250 MHz PLL for Clock Generation
  - Clock Tree Synthesis Software
- 3 & 5 Volts Operation; Single or Dual Supply Modes
- Low Power Consumption :
  - 0.6 µW/Gate/MHz @3 V
  - 2.2 µW/Gate/MHz @5 V
- Integrated Power on Reset
- Matrices With a max of 582 full programmable Pads
- Standard 3, 6, 12 and 24mA I/Os
- Versatile I/O Cell : Input, Output, I/O, Supply, Oscillator
- CMOS/TTL/PCI Interface
- ESD (2 kV) And Latch-up Protected I/O
- High Noise & EMC Immunity :
  - I/O with Slew Rate Control
  - Internal Decoupling
  - Signal Filtering between Periphery & Core
  - Application Dependent Supply Routing & Several
- Wide Range of Packages Including PGA, CQFP, PLCC PQFP, BGA, SSOP ...
- Delivery in Die Form
- Advanced CAD Support : Floor Plan, Proprietary Delay Models, Timing Driven Layout, Power Management
- Cadence, Mentor, Vital & Synopsys Reference Platforms
- EDIF & VHDL Reference Formats
- Available In Commercial, Industrial and Military Quality Grades
- Special Versions on Radiation Tolerant Process: see MG2RT and MG2RTP specification.
- QML Q

Product Outline

Type*	Total cells	Max. usable cells**	Total pads	Maximum programmable I/Os	Die dimension (µm) with scribe line	Die area (mm^2) with scribe line
MG2000	987	790	43	20	1770.08x1860.04	3.29
MG2001	1320	1056	47	24	1850.06x1970.03	3.64
MG2002	2310	1848	55	32	2060.07x2150.03	4.43
MG2004	4823	3858	71	48	2520.09x2420.07	6.10
MG2010	10564	8451	95	72	3060.08x3010.03	9.21
MG2015	15810	12648	111	88	3440.03x3380.09	11.63
MG2022	22000	17600	127	104	3840.10x3760.04	14.44
MG2044*	44616	35693	171	148	4890.08x4790.06	23.42
MG2055	55014	44011	187	164	5440.09x5340.07	29.05
MG2091*	91464	73171	235	212	6550.09x6480.08	42.45
MG2140*	140322	112258	285	262	7550.14x7700.08	58.14
MG2194*	193800	155040	331	308	8680.10x8740.08	75.86
MG2265*	264375	211500	384	362	9860.10x9850.13	97.12
MG2360*	361680	289344	435	412	11290.15x11360.11	128.26
MG2480*	481143	384914	507	484	12970.16x12900.16	167.32
MG2590	592977	474382	561	538	14020.18x14180.18	198.81
MG2700*	698523	558818	605	582	15100.17x15250.19	230.28

** to be used when ceramic package requested*
*** The max. number of usable gates is application dependent*

Libraries

The MG2 cell library has been designed to take full advantage of the features offered by both logic and test synthesis tools.

Design testability is assured by the full support of SCAN, JTAG (IEEE 1149) and BIST methodologies.

More complex macro functions are available in VHDL, as example : I2C, UART, Timer, ...

Block Generators

Block generators are used to create a customer specific simulation model and metallisation pattern for regular functions like RAM, DPRAM & FIFO. The basic cell architecture allows one bit per cell for RAM and DPRAM. The main characteristics of these generators are summarised below.

Function	Maximum Size (bits)	bits/word	Typical characteristics (16k bits) @5V	
			access time (ns)	Used cells
RAM	36 k	1-36	8	20 k
DPRAM	36 k	1-36	8.6	23 k
FIFO	36 k	1-36	9.2	23 k

I/O buffer interfacing

I/O Fexibility

All I/O buffers may be configured as input, output, bi-directional, oscillator or supply. A level translator is located close to each buffer.

Inputs

Input buffers with CMOS or TTL thresholds are non inverting and feature versions with and without hysteresis. The CMOS and TTL input buffers may incorporate pull-up or pull down terminators. For special purposes, a buffer allowing direct input to the matrix core is available.

Outputs

Several kinds of CMOS and TTL output drivers are offered : fast buffers with 3, 6, 12 and 24 mA drive at 5V, low noise buffers with 12 mA drive at 5V.

Clock generation & PLL

Clock generation

TEMIC offers 4 different types of oscillators : low power 32KHz crystal oscillator (up to Industrial Range), high frequency crystal oscillator and 2 RC oscillators. For all devices, the mark-space ratio is better than 40/60 and the start-up time less than 10 ms.

PLL

Two independent PLL devices are located in upper left and lower right corners. Each may be used for the following functions :

– Synchronisation of an internal clock on a reference system clock.
– Skew control : the internal clock transitions are synchronous with the reference clock.
– Frequency synthesis : two frequency dividers are included in each PLL. One divides the reference clock frequency F0 by a factor M and the other divides the internal clock frequency F by N. The internal clock frequency is :

$F = F0 * N / M$

Both M and N can take values from 1 to 16.

The maximum frequency at the PLL input after division by M is 40 MHz.

The maximum internal clock frequency is 250 MHz at 5 V and 150 MHz at 3 V ; the minimum frequency is 20 MHz.

Each PLL corner block has 5 dedicated pads : 2 VDD, 2 VSS and a filtering I/O connected to an RC network.

A power mode decreases consumption of the circuit and external divider can be added in the feedback digital path.

A PLL lock indication status is available without any additional filtering circuitry.

Note: For additional information, see 'MG2 / Phase Locked Loop" Rev 1.0, 15 Oct. 96.

Power supply & noise protection

The speed and density of the SCMOS3/2RT technology causes large switching current spikes for example either when :

16 high current output buffers switch simultaneously,

or

10% of the 700 000 gates are switching within a window of 1ns .

Sharp edges and high currents cause some parasitic elements in the packaging to become significant. In this frequency range, the package inductance and series resistance should be taken into account. It is known that an inductor slows down the settling time of the current and causes voltage drops on the power supply lines. These drops can affect the behaviour of the circuit itself or disturb the external application (ground bounce).

In order to improve the noise immunity of the MG core matrix, several mechanisms have been implemented inside the MG arrays. Two kinds of protection have been added : one to limit the I/O buffer switching noise and the other to protect the I/O buffers against the switching noise coming from the matrix.

I/O Buffers switching protection

Three features are implemented to limit the noise generated by the switching current :

- The power supplies of the input and output buffers are separated.
- The rise and fall times of the output buffers can be controlled by an internal regulator.
- A design rule concerning the number of buffers connected on the same power supply line has been imposed.

Matrix switching current protection

This noise disturbance is caused by a large number of gates switching simultaneously. To allow this without impacting the functionality of the circuit, three new features have been added :

- Decoupling capacitors are integrated directly on the silicon to reduce the power supply drop.
- A power supply network has been implemented in the matrix. This solution reduces the number of parasitic elements such as inductance and resistance and constitutes an artificial VDD and Ground plane. One mesh of the network supplies approximately 150 cells.
- A low pass filter has been added between the matrix and the input to the output buffer. This limits the transmission of the noise coming from the ground or the VDD supply of the matrix to the external world via the output buffers.

Power consumption

The power consumption of an MG2 array is due to three factors : leakage (P1), core (P2) and I/O (P3) consumption.

$P = P1 + P2 + P3$

Leakage (Standby) Power Consumption

The consumption due to leakage currents is defind as :

$P1 = (VDD – VSS) * I_{CCSB} * N_{CELL}$

Where I_{CCSB} is the leakage current through a polarised basic gate and N_{CELL} is the number of used cells.

Core Power Consumption

The power consumption due to the switching of cells in the core of the matrix is defind as:

$P2 = N_{CELL} * P_{GATE} * C_{ACTIVITY} * F$

Where N_{CELL} is the number of used cells, F the data toggling frequency, which is equal to half the clock frequency for random data and P_{GATE} is the power consumption per cell.

$P_{GATE} = P_{CA} + P_{CO}$

ACTIVITY is the fraction of the total number of cells toggling per cycle.

Capacitance Power

$P_{CA} = C * (VDD – VSS)^2/2$

C is the total output capacitance and may be expressed as the sum of the drain capacitance of the driver, the wiring capacitance and the gate capacitance of the inputs.

Worst case value : PCA # 1.8 µW/gate/MHz @ 5 V

Commutation Power

$P_{CO} = (VDD – VSS) * I_{dsohm}$

Where I_{dsohm} is the current flowing into the driver between supply and ground during the commutation. I_{dsohm} is about 15 % of the Pmos saturation currrent. Worst case value : Pco # 0.7 µW/gate/MHz @ 5 V

I/O Power Consumption

The power consumption due to the I/Os is :

$P3 = Ni * C_O * (VDD – VSS)^2 * Fi/2$

With Ni equals to the number of buffers running at Fi and C_O is the output capacitance.

Note : If a signal is a clock, Fi = F, if it is a data with random values, Fi = F/4.

Power Consumption Example @ 5V

Matrix	**MG2265**
Used gates (70 %)	185 k
Frequency	40 MHz
Standby Power	
Iccsb (125°C)	1 nA
$P1 = (VDD – VSS) * I_{CCSB} * N_{CELL}$	1 mW
Core Power	
Power Consumption per Cell	1.96 µW/Gate/MHz
$C_{activity}$	20 %
$P2 = N_{CELL} * P_{GATE} * C_{activity} * F$	1449 mW
I/O Power	
Total Number of Buffers	364
Number of Outputs and I/O Buffers	100
Output Capacitance	50 pF
$P3 = Ni * C_O * (VDD – VSS)^2 * Fi/2$	625 mW
Total Power	
P = P1 + P2 + P3	2.07 W

Packaging

TEMIC offers a wide range of packaging options which are listed below :

Package Type	Pins min/max*	Lead spacing (inch**)	Dimension (inch**)
DQFP	100 128	0.0256 0.0315	0.546x0.782 1.102^2
PLCCJ	28 84	0.050 0.050	0.453^2 0.653^2
PQFP	44 304	0.0315 0.0197	0.389^2 1.26^2
TQFP	32 100	0.0394 0.0315	0.394^2 0.551^2
VQFP	44 208	0.0197 0.0197	0.390^2 0.787^2
SSOP	16/64	0.0256	0.209x0.244
PSO	8 28	0.050 0.050	0.153x0.194 0.705x0.295
MLCC	68 84	0.050 0.050	0.950^2 1.150^2
MQFP	100 352	0.0256 0.020	0.787x0.551 1.889^2
CQPF	44 100	0.050	0.650^2
MPGA	176 391	0.10 100	1.5^2 2.0^2
BGA	169 352	100 0.10	1.5^2 2.0^2

* Please contact TEMIC Local Design Centers to check the availability of the use matrix and the plan package.
** To get the linear values in milimeters, multiply by 25.4

Design flows & tools

Design Flows and modes

A generic design flow for an MG2 array is sketched here beside.

A top down design methodology is proposed which starts with high level system description and is refined in successive design steps. At each step, structural verification is performed which includes the following tasks :

- Gate level logic simulation and comparison with high level simulation results.
- Design and test rule check.
- Power consumption analysis.
- Timing analysis (only after floor plan).

The main design stages are :

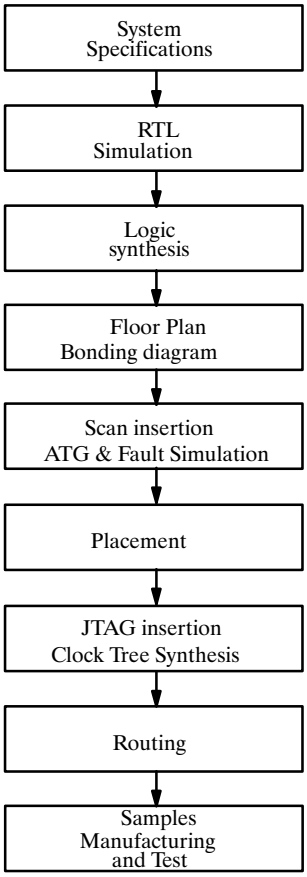
- System specification, preferably in VHDL form.
- Functional description at RTL level.
- Logic synthesis.
- Floor planning and bonding diagram generation.
- Test/Scan insertion, ATG and/or fault simulation.
- Physical cell placement, JTAG insertion and clock tree synthesis.
- Routing

To meet the various requirements of designers, several interface levels between the customer and TEMIC are possible.

For each of the possible design modes a review meeting is required for data transfer from the user to TEMIC. In all cases the final routing and verifications are performed by TEMIC.

The design acceptance is formalised by a design review which authorises TEMIC to proceed with sample manufacturing.

MG2 Design Flow



Design tool and design kits (DK)

The basic content of a design kit is described in the table below.

The interface formats to and from TEMIC rely on IEEE or industry standard :

– VHDL for functional descriptions

– VHDL or EDIF for netlists

– Tabular, log or .CAP for simulation results

– SDF (VITAL format) and SPF for backannotation

– LEF and DEF for physical floor plan information

The design kit supported for several commercial tools is outlined in the table below.

Design Kit Support	VHDL	Gate
Cadence	*	*
Mentor	*	*
Synopsys	*	*
Vital	*	*
Viewlogic	*	

Design kit Description

Design Tool or library	TEMIC Software Name
Design manual & libraries	
VHDL library for blocks	
Synthesis library	
Gate level simulation library	
Design rules analyser	STAR
Power consumption analyser	COMET
Floor plan library	
Timing analyser library	
Package & bonding software	PIM
Scan path & JTAG insertion	MISS
ATG & fault simulation library	

Operating characteristics

Absolute Maximum Ratings

Ambient temperature under bias (TA)
Commercial . . . . . 0°C to +70°C
Junction temperature . . . . . TJ < TA + 20°C
Storage temperature . . . . . –65 to +150°C
TTL/CMOS :
Supply voltage VDD . . . . . –0.5 V to +6 V
I/O voltage . . . . . –0.5 V to VDD + 0.5 V
Stresses above those listed may cause permanent damage to the device. Explosure to absolute maximum rating conditions for extended period may affect device reliability.

DC Characteristics

Specified at VDD = +5 V +/– 10 %

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIL	Input LOW voltage CMOS input TTL input	 0 0		 1.5 0.8	 V	
VIH	Input HIGH voltage CMOS input TTL input	 3.5 2.2		 VDD VDD	 V	
VOL	Output low voltage TTL			 0.4	 V	IOL = –12, 6, 3 mA*
VOH	Output high voltage CMOS TTL	 3.9 2.4			 V	IOH = –12, 6, 3 mA*
VT+	Schmitt trigger positive threshold CMOS input TTL input			 3.6 1.6	 V	
VT–	Schmitt trigger negative threshold CMOS input TTL input	 1.2 1.0			 V	
Delta V	CMOS hysteresis 25ºC/5V TTL hysteresis 25ºC/5V		 1.9 0.6		 V	
IL	Input leakage No pull up/down Pull up Pull down	 –55 79	 +/–1 –69 125	 +/–5 –120 330	 µA µA µA	
IOZ	3-State Output Leakage current		+/–1	+/–5	µA	
IOS	Output Short circuit current IOSN IOSP			 48 36	 mA mA	BOUT12 VOUT = 4.5V VOUT = VSS
ICCSB	Leakage current per cell		1.0	10.0	nA	military
ICCOP	Operating current per cell		0.39	0.53	µA/MHz	

* According buffer: Bout12, Bout6, Bout3, VDD = 4.5V

DC Characteristics

Specified at VDD = +3 V – 10%

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VIL	Input LOW voltage LVCMOS input LVTTL input	 0 0		 0.3VDD 0.8	 V	
VIH	Input HIGH voltage LVCMOS input LVTTL input	 0.7VDD 2.0		 VDD VDD	 V	
VOL	Output LOW voltage TTL			 0.4	 V	IOL = –6, 3, 1.5 mA*
VOH	Output HIGH voltage TTL	 2.4			 V	IOH = –4, 2, 1 mA*
VT+	Schmitt trigger positive threshold LVCMOS input LVTTL input			 2.2 1.2	 V	
VT–	Schmitt trigger negative threshold LVCMOS input LVTTL input	 0.9 0.8			 V	
Delta V	CMOS hysteresis 25ºC/5V TTL hysteresis 25ºC/5V		 0.8 0.2		 V	
IL	Input leakage No pull up/down Pull up Pull down	 –20 32	 24 42	 +/–1 –60 150	 µA µA µA	
IOZ	3–State Output Leakage current			+/–1	µA	
IOS	Output Short circuit current IOSN IOSP			 24 12	 mA mA	BOUT12 VOUT = VDD VOUT = VSS
ICCSB	Leakage current per cell		0.02	0.3	nA	commercial
			0.06	0.7	nA	industrial
			0.6	5	nA	military
ICCOP	Operating current per cell		0.2	0.3	µA/MHz	

* According buffer: Bout12, Bout6, Bout3

AC Characteristics

TJ = 25°C, Process typical (all values in ns)

Buffer	Description	Load	Transition	VDD	
				5V	3V
BOUT12	Output buffer with 12 mA drive	60pf	Tplh	3.18	4.67
			Tphl	2.35	3.33

Cell	Description	Load	Transition	VDD	
				5V	3V
BINCMOS	CMOS input buffer	15 fan	Tplh	0.75	1.12
			Tphl	0.7	0.98
BINTTL	TTL input buffer	16 fan	Tplh	0.88	1.29
			Tphl	0.65	1.03
INV	Inverter	12 fan	Tplh	0.54	0.85
			Tphl	0.39	0.49
NAND2	2 – input NAND	12 fan	Tplh	0.57	0.89
			Tphl	0.49	0.67
FDFF	D flip–flop, Clk to Q	8 fan	Tplh	0.86	1.30
			Tphl	0.73	1.08
			Ts	0.44	1.06
			Th	0.00	0.00