
HB56UW472EJN Series, HB56UW464EJN Series

HB56UW472EJN
32 MB Unbuffered EDO DRAM DIMM
4-Mword × 72-bit, 4 k Refresh, 1-Bank Module
(18 pcs of 4 M × 4 Components)

HB56UW464EJN
32 MB Unbuffered EDO DRAM DIMM
4-Mword × 64-bit, 4 k Refresh, 1-Bank Module
(16 pcs of 4 M × 4 Components)

HITACHI

ADE-203-718C (Z)
Rev.3.0
Nov. 1997

Description

The HB56UW472EJN, HB56UW464EJN belong to 8 Byte DIMM (Dual In-line Memory Module) family, and have been developed as an optimized main memory solution for 4 and 8 Byte processor applications. The HB56UW472EJN is a 4M × 72 dynamic RAM module, mounted 18 pieces of 16-Mbit DRAM (HM51W16405) sealed in SOJ package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56UW464EJN is a 4M × 64 dynamic RAM module, mounted 16 pieces of 16-Mbit DRAM (HM51W16405) sealed in SOJ package and 1 pieces of serial EEPROM (24C02) for Presence Detect (PD). The HB56UW472EJN, HB56UW464EJN offer Extended Data Out (EDO) Page Mode as a high speed access mode. An outline of the HB56UW472EJN, HB56UW464EJN is 168-pin socket type package (dual lead out). Therefore, the HB56UW472EJN, HB56UW464EJN make high density mounting possible without surface mount technology. The HB56UW472EJN, HB56UW464EJN provide common data inputs and outputs. Decoupling capacitors are mounted on the module board.

Features

- 168-pin socket type package (Dual lead out)
 - Outline: 133.35 mm (Length) × 25.40 mm (Height) × 9.00 mm (Thickness)
 - Lead pitch: 1.27 mm
- Single 3.3 V (±0.3 V) supply

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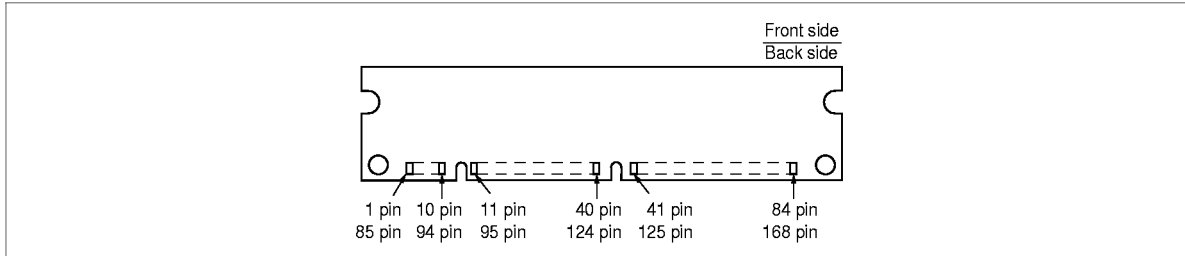
- High speed
 - Access time : $t_{\text{RAC}} = 50/60/70\text{ns}$ (max)
: $t_{\text{CAC}} = 13/15/18\text{ns}$ (max)
- Low power dissipation
 - Active mode: 5.83/5.18/4.54 W (max) (HB56UW472EJN Series)
: 5.18/4.61/4.03 W (max) (HB56UW464EJN Series)
 - Standby mode (TTL): 129.6 mW (max) (HB56UW472EJN Series)
(TTL): 115.2 mW (max) (HB56UW464EJN Series)
(CMOS): 6.48 mW (max) (L-version) (HB56UW472EJN Series)
(CMOS): 5.76 mW (max) (L-version) (HB56UW464EJN Series)
- JEDEC standard outline unbuffered 8-byte DIMM
- EDO page mode capability
- Refresh period
 - 4096 refresh cycles : 64 ms
: 128 ms (L-version)
- 4 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
 - Hidden refresh
 - Self refresh (L-version)

Ordering Information

Type No.	Access time	Package	Contact pad
HB56UW472EJN-5	50 ns	168-pin dual lead out socket type	Gold
HB56UW472EJN-6	60 ns		
HB56UW472EJN-7	70 ns		
HB56UW472EJN-5L	50 ns		
HB56UW472EJN-6L	60 ns		
HB56UW472EJN-7L	70 ns		
HB56UW464EJN-5	50 ns		
HB56UW464EJN-6	60 ns		
HB56UW464EJN-7	70 ns		
HB56UW464EJN-5L	50 ns		
HB56UW464EJN-6L	60 ns		
HB56UW464EJN-7L	70 ns		

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Pin Arrangement



Pin Arrangement

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V _{SS}	43	V _{SS}	85	V _{SS}	127	V _{SS}
2	DQ0	44	$\overline{\text{OE2}}$	86	DQ32	128	NC
3	DQ1	45	$\overline{\text{RAS2}}$	87	DQ33	129	NC
4	DQ2	46	$\overline{\text{CAS2}}$	88	DQ34	130	$\overline{\text{CAS6}}$
5	DQ3	47	$\overline{\text{CAS3}}$	89	DQ35	131	$\overline{\text{CAS7}}$
6	V _{CC}	48	$\overline{\text{WE2}}$	90	V _{CC}	132	NC
7	DQ4	49	V _{CC}	91	DQ36	133	V _{CC}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2 (NC)* ³	94	DQ39	136	CB6 (NC)* ⁷
11	DQ8	53	CB3 (NC)* ⁴	95	DQ40	137	CB7 (NC)* ⁸
12	V _{SS}	54	V _{SS}	96	V _{SS}	138	V _{SS}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V _{CC}	101	DQ45	143	V _{CC}
18	V _{CC}	60	DQ20	102	V _{CC}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0 (NC)* ¹	63	NC	105	CB4 (NC)* ⁵	147	NC
22	CB1 (NC)* ²	64	V _{SS}	106	CB5 (NC)* ⁶	148	V _{SS}
23	V _{SS}	65	DQ21	107	V _{SS}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55

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Pin Arrangement (cont)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
26	V _{CC}	68	V _{SS}	110	V _{CC}	152	V _{SS}
27	$\overline{\text{WE0}}$	69	DQ24	111	NC	153	DQ56
28	$\overline{\text{CAS0}}$	70	DQ25	112	$\overline{\text{CAS4}}$	154	DQ57
29	$\overline{\text{CAS1}}$	71	DQ26	113	$\overline{\text{CAS5}}$	155	DQ58
30	$\overline{\text{RAS0}}$	72	DQ27	114	NC	156	DQ59
31	$\overline{\text{OE0}}$	73	V _{CC}	115	NC	157	V _{CC}
32	V _{SS}	74	DQ28	116	V _{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V _{SS}	120	A7	162	V _{SS}
37	A8	79	NC	121	A9	163	NC
38	A10	80	NC	122	A11	164	NC
39	NC	81	NC	123	NC	165	SA0
40	V _{CC}	82	SDA	124	V _{CC}	166	SA1
41	V _{CC}	83	SCL	125	NC	167	SA2
42	NC	84	V _{CC}	126	NC	168	V _{CC}

Notes: 1. CB0: HB56UW472EJN, NC: HB56UW464EJN
 2. CB1: HB56UW472EJN, NC: HB56UW464EJN
 3. CB2: HB56UW472EJN, NC: HB56UW464EJN
 4. CB3: HB56UW472EJN, NC: HB56UW464EJN
 5. CB4: HB56UW472EJN, NC: HB56UW464EJN
 6. CB5: HB56UW472EJN, NC: HB56UW464EJN
 7. CB6: HB56UW472EJN, NC: HB56UW464EJN
 8. CB7: HB56UW472EJN, NC: HB56UW464EJN

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Pin Description

Pin name	Function
A0 to A11	Address input Row address: A0 to A11 Column address: A0 to A9 Refresh address: A0 to A11
DQ0 to DQ63	Data-in/data-out
$\overline{\text{RAS0}}$, $\overline{\text{RAS2}}$	Row address strobe
$\overline{\text{CAS0}}$ to $\overline{\text{CAS7}}$	Column address strobe
$\overline{\text{WE0}}$, $\overline{\text{WE2}}$	Read/Write enable
$\overline{\text{OE0}}$, $\overline{\text{OE2}}$	Output enable
SDA	Serial data for PD
SCL	Serial clock for PD
SA0 to SA2	Serial address for PD
CB0 to CB7* ¹	Check bit
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Note: 1. This function is supported only HB56UW472EJN Series.

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Serial PD Matrix*¹

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128 byte
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	0	1	0	02	EDO
3	Number of row addresses bits	0	0	0	0	1	1	0	0	0C	12
4	Number of column addresses bits	0	0	0	0	1	0	1	0	0A	10
5	Number of banks	0	0	0	0	0	0	0	1	01	1
6	Module data width (HB56UW472EJN)	0	1	0	0	1	0	0	0	48	72
	(HB56UW464EJN)	0	1	0	0	0	0	0	0	40	64
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTL
9	RAS access time -5/-5L	0	0	1	1	0	0	1	0	32	$t_{RAC} = 50 \text{ ns}$
	-6/-6L	0	0	1	1	1	1	0	0	3C	$t_{RAC} = 60 \text{ ns}$
	-7/-7L	0	1	0	0	0	1	1	0	46	$t_{RAC} = 70 \text{ ns}$
10	CAS access time -5/-5L	0	0	0	0	1	1	0	1	0D	$t_{CAC} = 13 \text{ ns}$
	-6/-6L	0	0	0	0	1	1	1	1	0F	$t_{CAC} = 15 \text{ ns}$
	-7/-7L	0	0	0	1	0	0	1	0	12	$t_{CAC} = 18 \text{ ns}$
11	Module configuration type (HB56UW472EJN)	0	0	0	0	0	0	1	0	02	ECC
	(HB56UW464EJN)	0	0	0	0	0	0	0	0	00	Non parity
12	Refresh rate/type -5/-6/-7	0	0	0	0	0	0	0	0	00	Normal (15.625 μs)
	-5L/-6L/-7L	1	0	0	0	0	0	1	1	83	Self refresh (31.3 μs)
13	DRAM width	0	0	0	0	0	1	0	0	04	4M $\times$ 4
14	Error checking DRAM width (HB56UW472EJN)	0	0	0	0	0	1	0	0	04	4M $\times$ 4
	(HB56UW464EJN)	0	0	0	0	0	0	0	0	00	—
15 to 31	Reserved for future offerings	0	0	0	0	0	0	0	0	00	
32 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future offerings
62	SPD data revision code	0	0	0	0	0	0	0	1	01	Rev.1

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Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
63	Checksum for bytes 0 to 62 (HB56UW472EJN-5)	0	0	1	1	0	1	0	0	34	
	(HB56UW472EJN-6)	0	1	0	0	0	0	0	0	40	
	(HB56UW472EJN-7)	0	1	0	0	1	1	0	1	4D	
	(HB56UW472EJN-5L)	1	0	1	1	0	1	1	1	B7	
	(HB56UW472EJN-6L)	1	1	0	0	0	0	1	1	C3	
	(HB56UW472EJN-7L)	1	1	0	1	0	0	0	0	D0	
	(HB56UW464EJN-5)	0	0	1	0	0	1	1	0	26	
	(HB56UW464EJN-6)	0	0	1	1	0	0	1	0	32	
	(HB56UW464EJN-7)	0	0	1	1	1	1	1	1	3F	
	(HB56UW464EJN-5L)	1	0	1	0	1	0	0	1	A9	
	(HB56UW464EJN-6L)	1	0	1	1	0	1	0	1	B5	
	(HB56UW464EJN-7L)	1	1	0	0	0	0	1	0	C2	
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	×	*2 (ASCII-8bit code)
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	1	1	0	36	6
77	Manufacturer's part number	0	1	0	1	0	1	0	1	55	U
78	Manufacturer's part number	0	1	0	1	0	1	1	1	57	W
79	Manufacturer's part number	0	0	1	1	0	1	0	0	34	4
80	Manufacturer's part number (HB56UW472EJN)	0	0	1	1	0	1	1	1	37	7
	(HB56UW464EJN)	0	0	1	1	0	1	1	0	36	6
81	Manufacturer's part number (HB56UW472EJN)	0	0	1	1	0	0	1	0	32	2
	(HB56UW464EJN)	0	0	1	1	0	1	0	0	34	4
82	Manufacturer's part number	0	1	0	0	0	1	0	1	45	E
83	Manufacturer's part number	0	1	0	0	1	0	1	0	4A	J
84	Manufacturer's part number	0	1	0	0	1	1	1	0	4E	N
85	Manufacturer's part number	0	1	0	1	1	1	1	1	5F	—
86	Manufacturer's part number -5/-5L	0	0	1	1	0	1	0	1	35	5
	-6/-6L	0	0	1	1	0	1	1	0	36	6
	-7/-7L	0	0	1	1	0	1	1	1	37	7

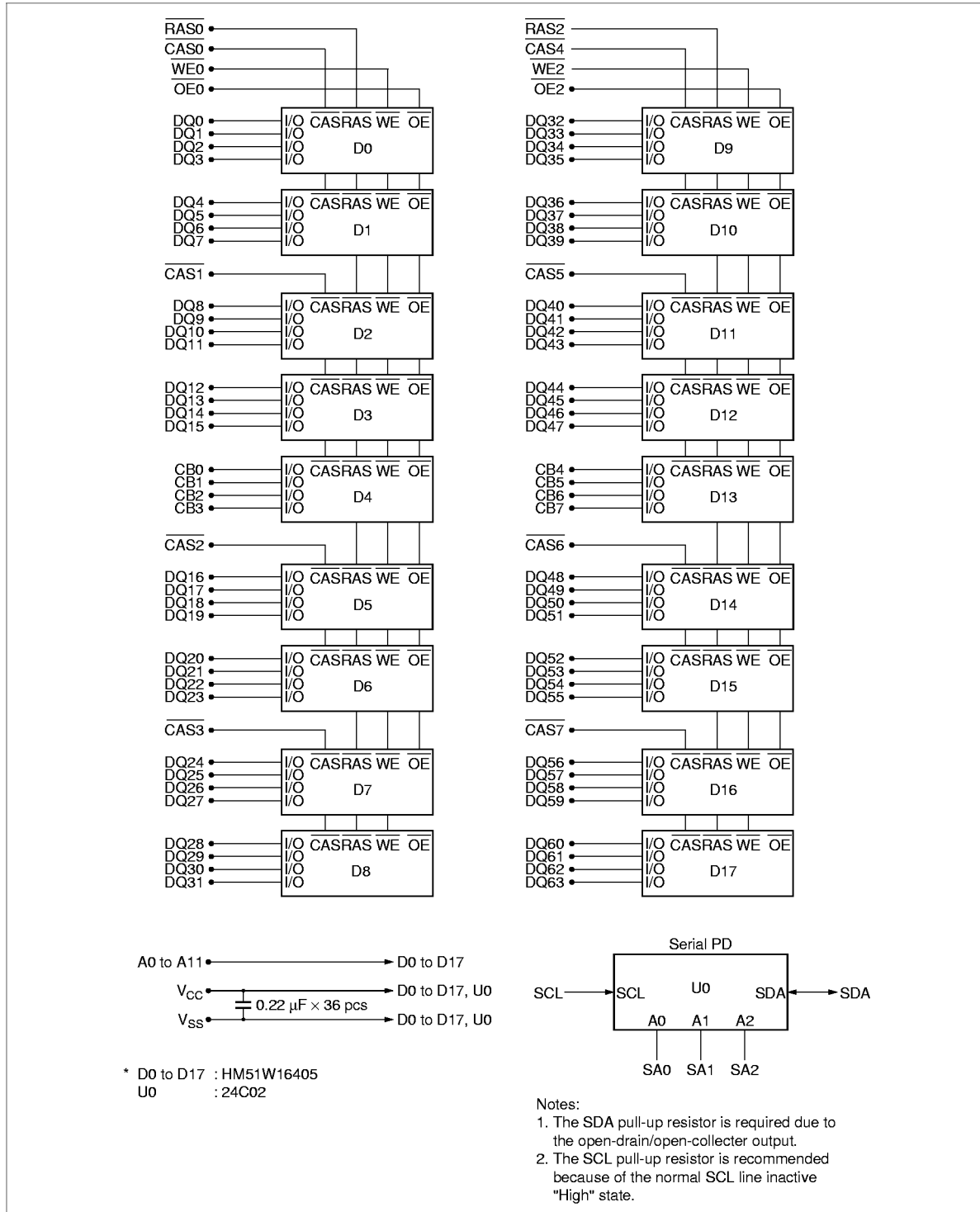
HB56UW472EJN Series, HB56UW464EJN Series

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
87	Manufacturer's part number -5/-6/-7	0	0	1	0	0	0	0	0	20	(Space)
	-5L/-6L/-7L	0	1	0	0	1	1	0	0	4C	L
88	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	×	Year code (binary) ^{*3}
94	Manufacturing date	×	×	×	×	×	×	×	×	×	Weak code (binary) ^{*4}
95 to 98	Assembly serial number	^{*5}									
99 to 125	Manufacturer specific data	^{*6}									
126	Reserved	0	0	0	0	0	0	0	0	00	Not use
127	Reserved	0	0	0	0	0	0	0	0	00	Not use

- Notes: 1. All serial PD data are not protected. 0: Serial data, "driven Low", 1: Serial data, "driven High"
2. Byte 72 is manufacturing location code. (ex: In case of Japan, byte72 is 4Ah. 4Ah shows "J" on ASCII code.)
3. Byte 93 (Manufacturing date-year code) ex: 61h shows year '97. 62h shows year '98.
4. Byte 94 (Manufacturing date-week code) ex: 0Bh shows week 11. 24h shows week 36.
5. Byte 95 through 98 are assembly serial number.
6. All bits of 99 through 125 are not defined ("1" or "0").

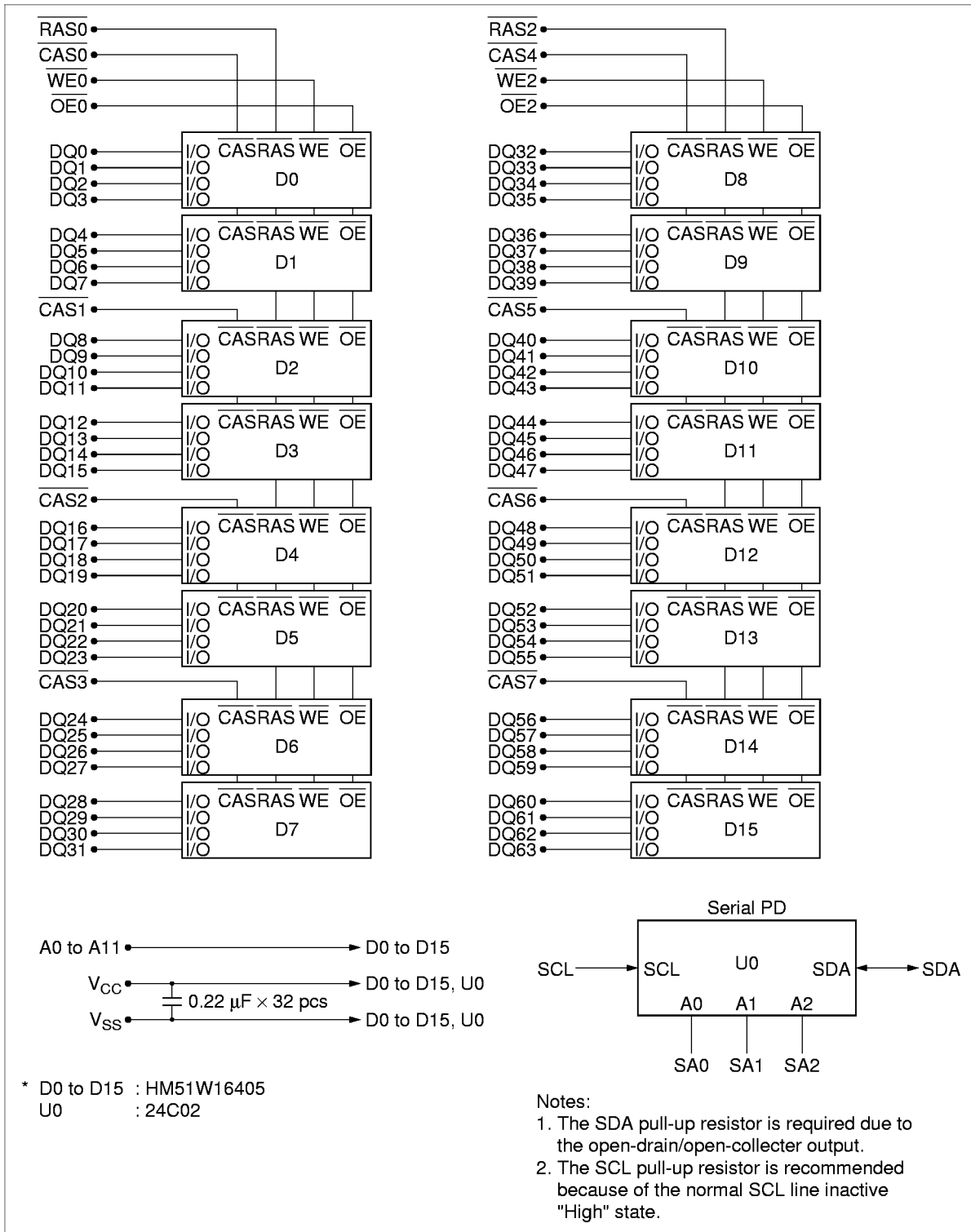
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Block Diagram (HB56UW472EJN)



HB56UW472EJN Series, HB56UW464EJN Series

Block Diagram (HB56UW464EJN)



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +4.6	V
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V
Short circuit output current	I_{out}	50	mA
Power dissipation (HB56UW472EJN)	P_t	18	W
Power dissipation (HB56UW464EJN)	P_t	16	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	
	V_{CC}	3.0	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V	1
Input low voltage	V_{IL}	−0.3	—	0.8	V	1

Note: 1. All voltage referred to V_{SS} .

HB56UW472EJN Series, HB56UW464EJN Series

DC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = 0 \text{ V}$) (HB56UW472EJN)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	1620	—	1440	—	1260	mA	$t_{RC} = \min$	1, 2
Standby current	I_{CC2}	—	36	—	36	—	36	mA	TTL interface $\overline{RAS}, \overline{CAS} = V_{IH}$ Dout = High-Z	
		—	18	—	18	—	18	mA	CMOS interface $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	1.8	—	1.8	—	1.8	mA	CMOS interface $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z	
$\overline{RAS}$ -only refresh current	I_{CC3}	—	1620	—	1440	—	1260	mA	$t_{RC} = \min$	2
Standby current	I_{CC5}	—	90	—	90	—	90	mA	$\overline{RAS} = V_{IH}, \overline{CAS} = V_{IL}$ Dout = enable	1
$\overline{CAS}$ -before- $\overline{RAS}$ refresh current	I_{CC6}	—	1620	—	1440	—	1260	mA	$t_{RC} = \min$	
EDO page mode current	I_{CC7}	—	1440	—	1260	—	1170	mA	$t_{HPC} = \min$	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	5.4	—	5.4	—	5.4	mA	CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 31.3 \mu\text{s}$ $t_{RAS} \leq 0.3 \mu\text{s}$	
Self refresh mode current (L-version)	I_{CC11}	—	3.6	—	3.6	—	3.6	mA	CMOS interface $\overline{RAS}, \overline{CAS} \leq 0.2 \text{ V}$ Dout = High-Z	
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \text{ V} \leq V_{in} \leq 4.6 \text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \text{ V} \leq V_{out} \leq 4.6 \text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

HB56UW472EJN Series, HB56UW464EJN Series

DC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = 0 \text{ V}$) (HB56UW464EJN)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	—	1440	—	1280	—	1120	mA	$t_{RC} = \min$	1, 2
Standby current	I_{CC2}	—	32	—	32	—	32	mA	TTL interface $\overline{RAS}, \overline{CAS} = V_{IH}$ Dout = High-Z	
		—	16	—	16	—	16	mA	CMOS interface $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z	
Standby current (L-version)	I_{CC2}	—	1.6	—	1.6	—	1.6	mA	CMOS interface $\overline{RAS}, \overline{CAS} \geq V_{CC} - 0.2 \text{ V}$ Dout = High-Z	
$\overline{RAS}$ -only refresh current	I_{CC3}	—	1440	—	1280	—	1120	mA	$t_{RC} = \min$	2
Standby current	I_{CC5}	—	80	—	80	—	80	mA	$\overline{RAS} = V_{IH}, \overline{CAS} = V_{IL}$ Dout = enable	1
$\overline{CAS}$ -before- $\overline{RAS}$ refresh current	I_{CC6}	—	1440	—	1280	—	1120	mA	$t_{RC} = \min$	
EDO page mode current	I_{CC7}	—	1280	—	1120	—	1040	mA	$t_{HPC} = \min$	1, 3
Battery backup current (Standby with CBR refresh) (L-version)	I_{CC10}	—	4.8	—	4.8	—	4.8	mA	CMOS interface Dout = High-Z CBR refresh: $t_{RC} = 31.3 \mu\text{s}$ $t_{RAS} \leq 0.3 \mu\text{s}$	
Self refresh mode current (L-version)	I_{CC11}	—	3.2	—	3.2	—	3.2	mA	CMOS interface $\overline{RAS}, \overline{CAS} \leq 0.2 \text{ V}$ Dout = High-Z	
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \text{ V} \leq V_{in} \leq 4.6 \text{ V}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \text{ V} \leq V_{out} \leq 4.6 \text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = -2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	0	0.4	V	Low Iout = 2 mA	

- Notes: 1. I_{CC} depends on output load condition when the device is selected, I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

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Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V) (HB56UW472EJN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{II}	—	110	pF	1
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{I2}	—	83	pF	1
Input capacitance ($\overline{\text{CAS}}$)	C _{I3}	—	41	pF	1
I/O capacitance (DQ, CB)	C _{I/O}	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{\text{CAS}} = V_{\text{IH}}$ to disable Dout.

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V) (HB56UW464EJN)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C _{II}	—	100	pF	1
Input capacitance ($\overline{\text{RAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	C _{I2}	—	76	pF	1
Input capacitance ($\overline{\text{CAS}}$)	C _{I3}	—	34	pF	1
I/O capacitance (DQ)	C _{I/O}	—	20	pF	1, 2

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $\overline{\text{CAS}} = V_{\text{IH}}$ to disable Dout.

AC Characteristics (Ta = 0 to 70°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) *¹, *², *¹⁸, *¹⁹

Test Conditions

- Input rise and fall times: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

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Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84	—	104	—	124	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	—	40	—	50	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	—	10	—	13	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	70	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10000	10	10000	13	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	8	—	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	8	—	10	—	13	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	37	14	45	14	52	ns	3
$\overline{RAS}$ to column address delay time	t_{RAD}	10	25	12	30	12	35	ns	4
$\overline{RAS}$ hold time	t_{RSH}	10	—	13	—	13	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	35	—	40	—	45	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	13	—	15	—	18	—	ns	5
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	0	—	ns	6
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	0	—	ns	6
Transition time (rise and fall)	t_T	2	50	2	50	2	50	ns	7
Refresh period (4,096 cycles)	t_{REF}	—	64	—	64	—	64	ms	
Refresh period (4,096 cycles) (L-version)	t_{REF}	—	128	—	128	—	128	ms	

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Read Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	50	—	60	—	70	ns	8, 9
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	13	—	15	—	18	ns	9, 10, 17
Access time from address	t_{AA}	—	25	—	30	—	35	ns	9, 11, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	—	13	—	15	—	18	ns	9, 21
Read command setup time	t_{RCS}	0	—	0	—	0	—	ns	
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	12
Read command hold time from $\overline{\text{RAS}}$	t_{RCHR}	50	—	60	—	70	—	ns	
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	5	—	5	—	5	—	ns	12
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	25	—	30	—	35	—	ns	
Column address to $\overline{\text{CAS}}$ lead time	t_{CAL}	15	—	18	—	23	—	ns	
$\overline{\text{CAS}}$ to output in low-Z	t_{CLZ}	0	—	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	3	—	ns	22
Output data hold time from $\overline{\text{OE}}$	t_{OHO}	3	—	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	13	—	15	—	15	ns	13, 22
Output buffer turn-off to $\overline{\text{OE}}$	t_{OEZ}	—	13	—	15	—	15	ns	13
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	13	—	15	—	18	—	ns	5
Output data hold time from $\overline{\text{RAS}}$	t_{OHR}	3	—	3	—	3	—	ns	22
Output buffer turn-off time to $\overline{\text{RAS}}$	t_{OFR}	—	13	—	15	—	15	ns	22
Output buffer turn-off to $\overline{\text{WE}}$	t_{WEZ}	—	13	—	15	—	15	ns	
$\overline{\text{WE}}$ to Din delay time	t_{WED}	13	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ to Din delay time	t_{RDD}	13	—	15	—	18	—	ns	
$\overline{\text{RAS}}$ next $\overline{\text{CAS}}$ delay time	t_{RNCD}	50	—	60	—	70	—	ns	

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Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	—	0	—	0	—	ns	14
Write command hold time	t_{WCH}	8	—	10	—	13	—	ns	
Write command pulse width	t_{WP}	8	—	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8	—	10	—	13	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8	—	10	—	13	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	0	—	ns	15
Data-in hold time	t_{DH}	8	—	10	—	13	—	ns	15

Read-Modify-Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	111	—	135	—	161	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	67	—	79	—	92	—	ns	14
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	—	34	—	40	—	ns	14
Column address to $\overline{WE}$ delay time	t_{AWD}	42	—	49	—	57	—	ns	14
$\overline{OE}$ hold time $\overline{WE}$	t_{OEHL}	13	—	15	—	18	—	ns	

Refresh Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	8	—	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	8	—	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	—	5	—	5	—	ns	

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EDO Page Mode Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EDO page mode cycle time	t_{HPC}	20	—	25	—	30	—	ns	20
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	—	100000	ns	16
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	30	—	35	—	40	ns	9, 17
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	30	—	35	—	40	—	ns	
Output data hold time from $\overline{CAS}$ low	t_{DOH}	3	—	3	—	3	—	ns	9, 17
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	8	—	10	—	13	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	30	—	35	—	40	—	ns	

EDO Page Mode Read-Modify-Write Cycle

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
EDO page mode read-modify-write cycle time	t_{HPRWC}	57	—	68	—	79	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	45	—	54	—	62	—	ns	14

Self Refresh Mode (L-version)

Parameter	Symbol	50 ns		60 ns		70 ns		Unit	Notes
		Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ pulse width (Self refresh)	t_{RASS}	100	—	100	—	100	—	μs	
$\overline{RAS}$ precharge time (Self refresh)	t_{RPS}	90	—	110	—	130	—	ns	
$\overline{CAS}$ hold time (Self refresh)	t_{CHS}	-50	—	-50	—	-50	—	ns	

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- Notes: 1. AC measurements assume $t_T = 2 \text{ ns}$.
2. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
 3. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{\text{RCD}} \geq t_{\text{RAD}} (\text{max}) + t_{\text{AA}} (\text{max}) - t_{\text{CAC}} (\text{max})$, then access time is controlled exclusively by t_{CAC} .
 4. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA} .
 5. Either t_{OED} or t_{CDD} must be satisfied.
 6. Either t_{DZO} or t_{DZC} must be satisfied.
 7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
 8. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}} (\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}} (\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
 10. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}} (\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \geq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$.
 11. Assumes that $t_{\text{RAD}} \geq t_{\text{RAD}} (\text{max})$ and $t_{\text{RCD}} + t_{\text{CAC}} (\text{max}) \leq t_{\text{RAD}} + t_{\text{AA}} (\text{max})$.
 12. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 13. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 14. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} , and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}} \geq t_{\text{WCS}} (\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}} (\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$, and $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$ or $t_{\text{CWD}} \geq t_{\text{CWD}} (\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}} (\text{min})$ and $t_{\text{CPW}} \geq t_{\text{CPW}} (\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 15. These parameters are referred to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 16. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in EDO page mode cycles.
 17. Access time is determined by the longest among t_{AA} , t_{CAC} and t_{CPA} .
 18. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device. After $\overline{\text{RAS}}$ is reset, if $t_{\text{OEH}} \geq t_{\text{CWL}}$, the DQ pin will remain open circuit (high impedance); $t_{\text{OEH}} < t_{\text{OEH}}$, invalid data will be out at each DQ.
 19. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 20. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{\text{RAS}}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{\text{CAS}}$ cycle ($t_{\text{CAS}} + t_{\text{CP}} + 2t_T$) becomes greater than the specified t_{HPC} (min) value. The value of $\overline{\text{CAS}}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
 21. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{\text{CC}} / V_{\text{SS}}$ line noise, which causes to degrade V_{IH} min./ V_{IL} max level.
 22. Data output turns off and becomes high impedance from later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ between t_{OHR} and t_{OH} , and between t_{OFR} and t_{OFF} .
 23. Please do not use t_{RASS} timing, $10 \mu\text{s} \leq t_{\text{RASS}} \leq 100 \mu\text{s}$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{\text{RASS}} \geq 100 \mu\text{s}$, then $\overline{\text{RAS}}$ precharge time should use t_{RPS} instead of t_{RP} .

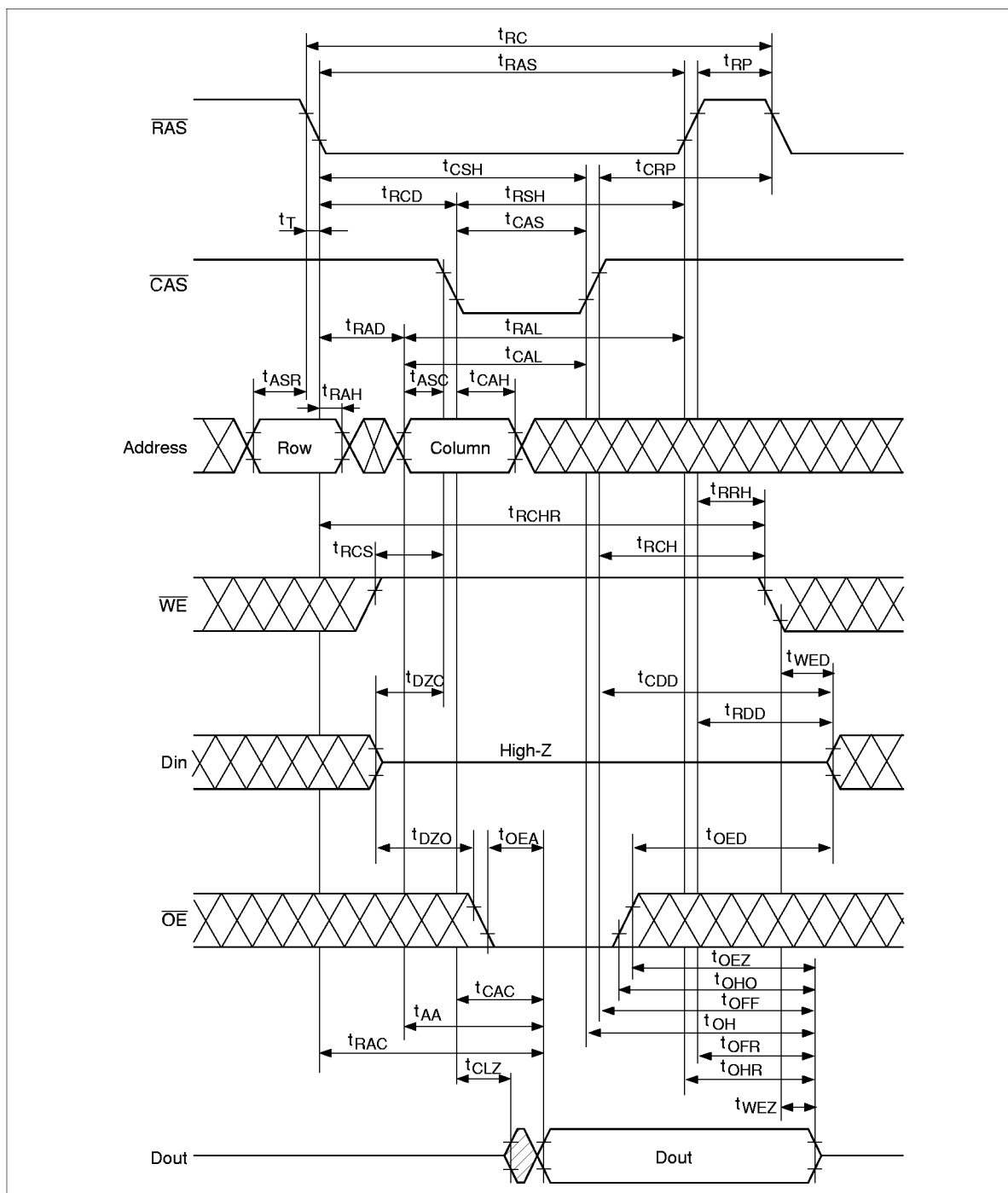
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24. If you use distributed CBR refresh mode with 15.6 μ s interval in normal read/write cycle, CBR refresh should be executed within 15.6 μ s immediately after exiting from and before entering into self refresh mode.
25. If you use $\overline{\text{RAS}}$ only refresh or CBR burst refresh mode in normal read/write cycle, 4096 of distributed CBR refresh with 15.6 μ s interval should be executed within 64 ms immediately after exiting from and before entering into the self refresh mode.
26. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
27. XXX: H or L (H: $V_{\text{IH}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IH}}(\text{max})$, L: $V_{\text{IL}}(\text{min}) \leq V_{\text{IN}} \leq V_{\text{IL}}(\text{max})$)
/////: Invalid Dout
When the address, clock and input pins are not described on timing waveforms, their pins must be applied V_{IH} or V_{IL} .

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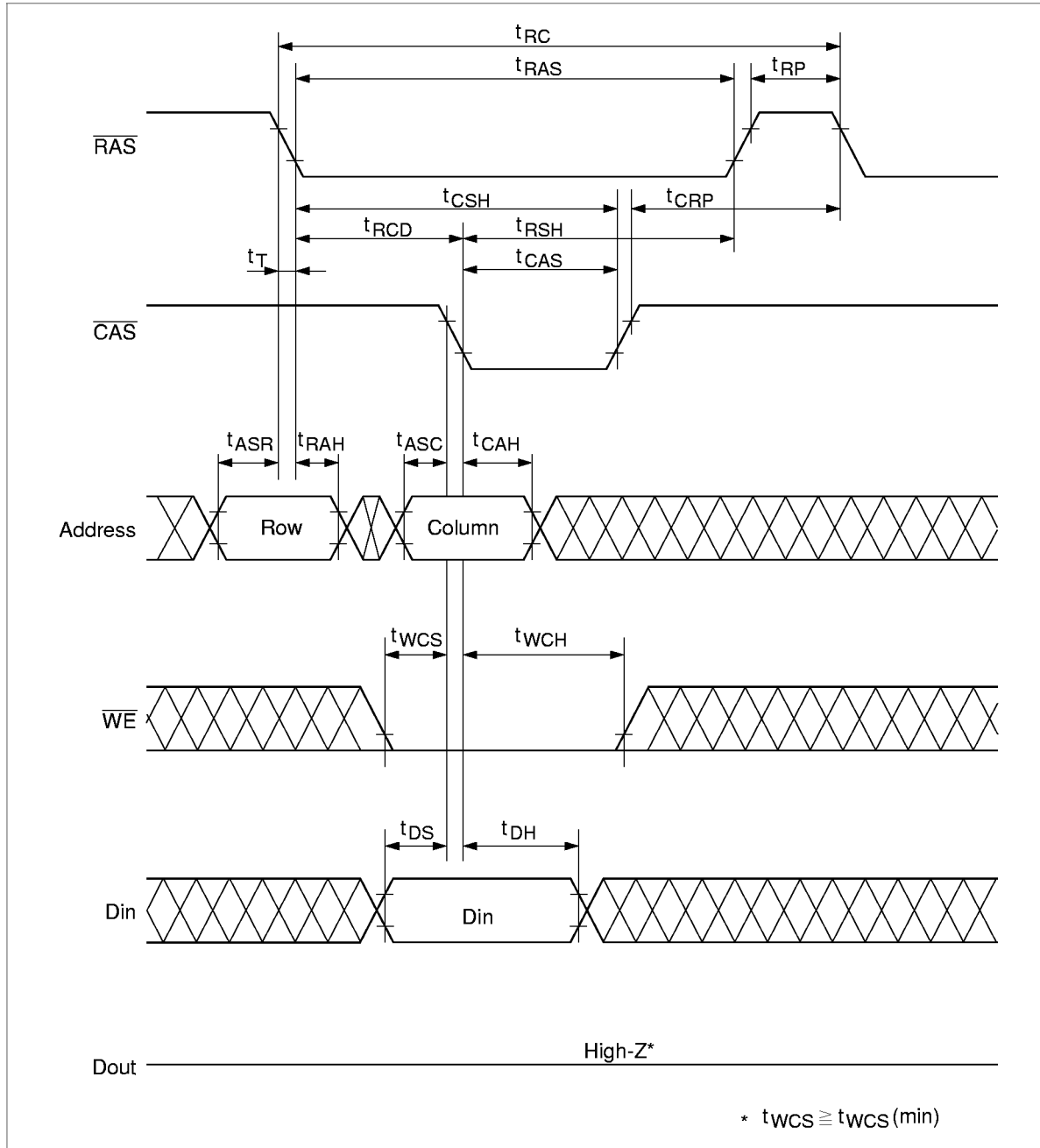
Timing Waveforms*²⁷

Read Cycle



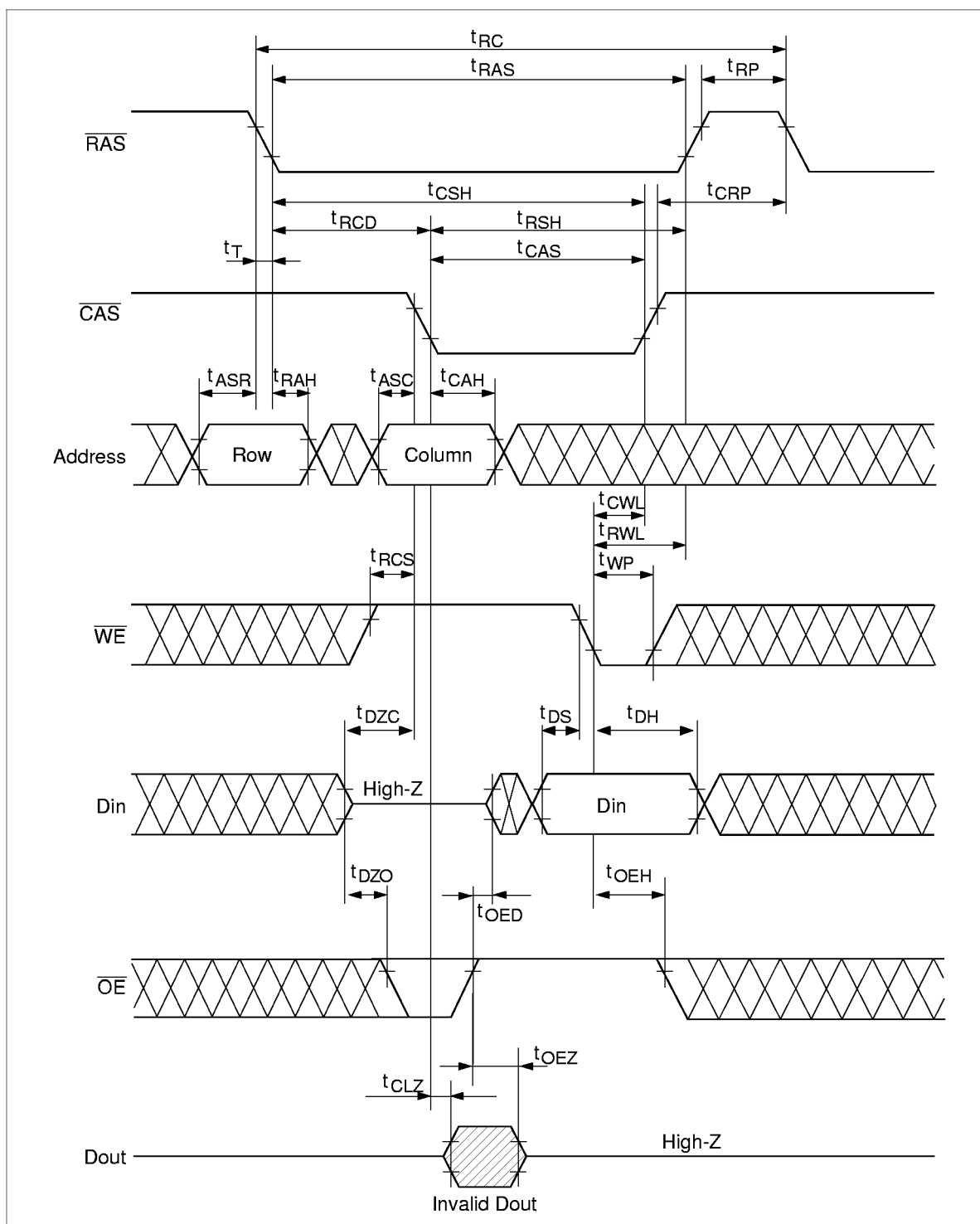
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Early Write Cycle



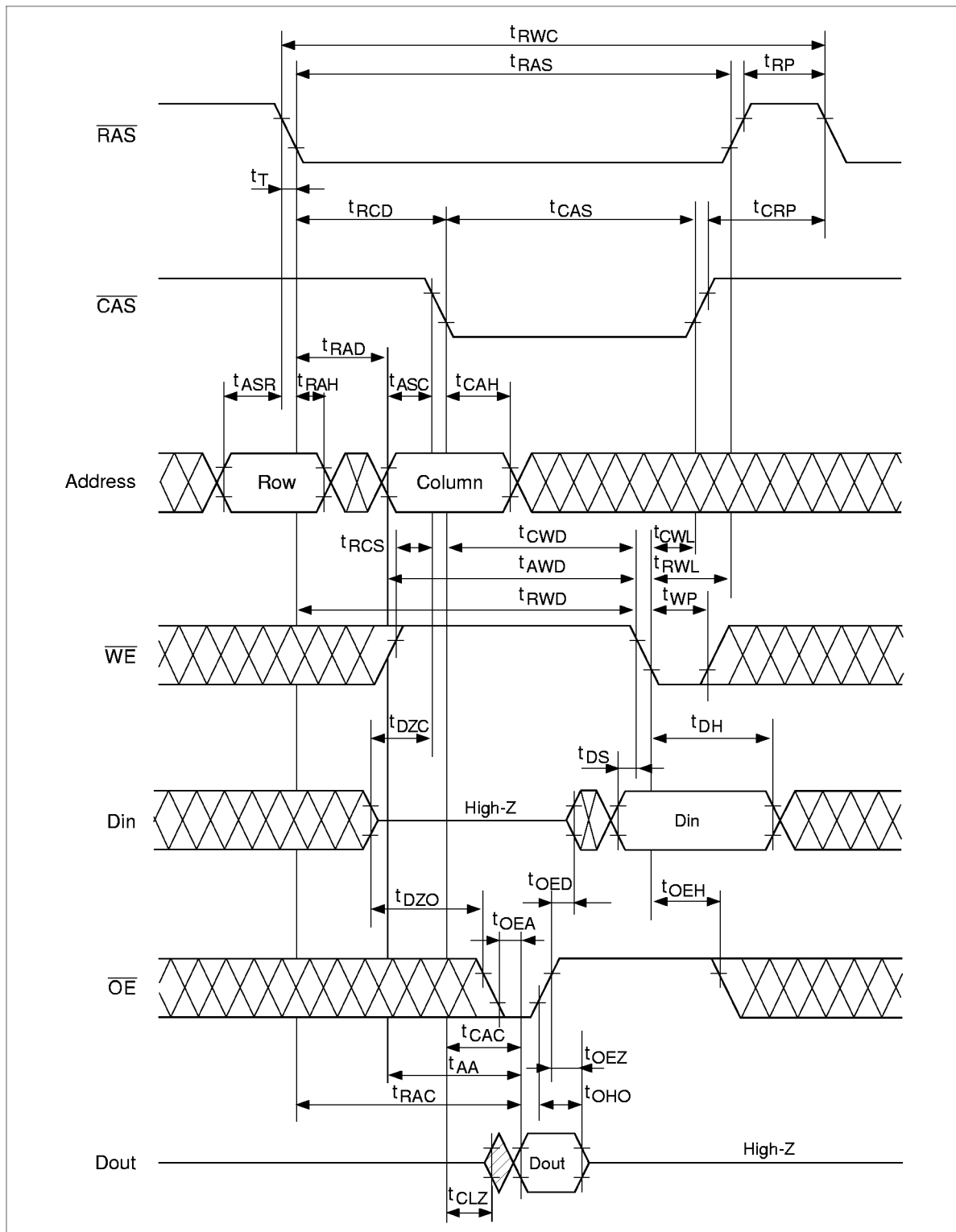
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Delayed Write Cycle*18



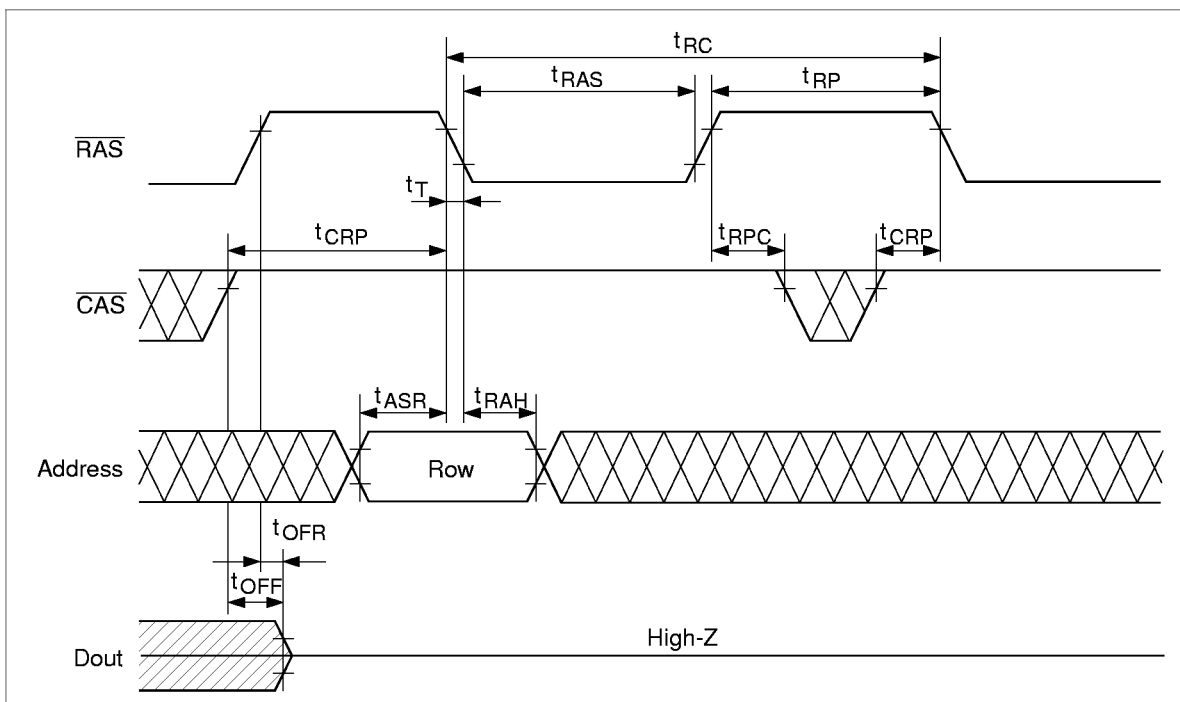
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Read-Modify-Write Cycle*18



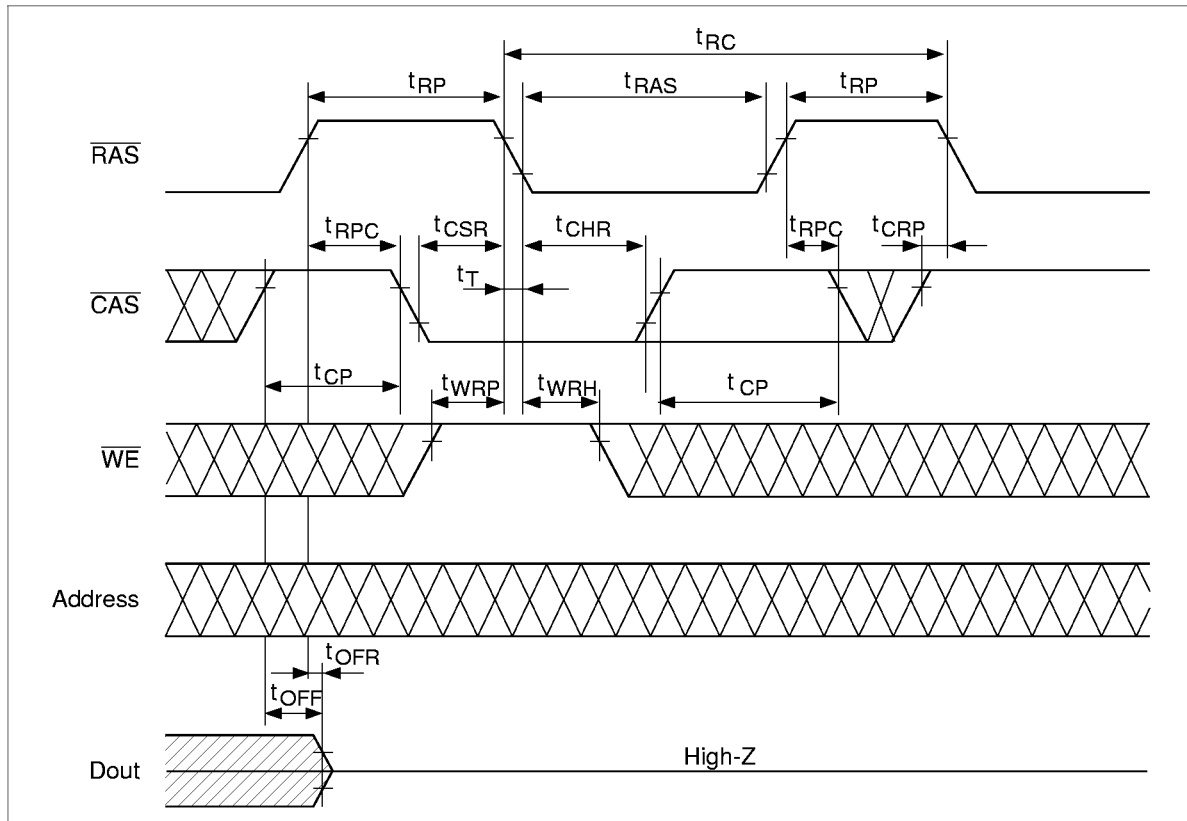
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$\overline{\text{RAS}}$ -Only Refresh Cycle

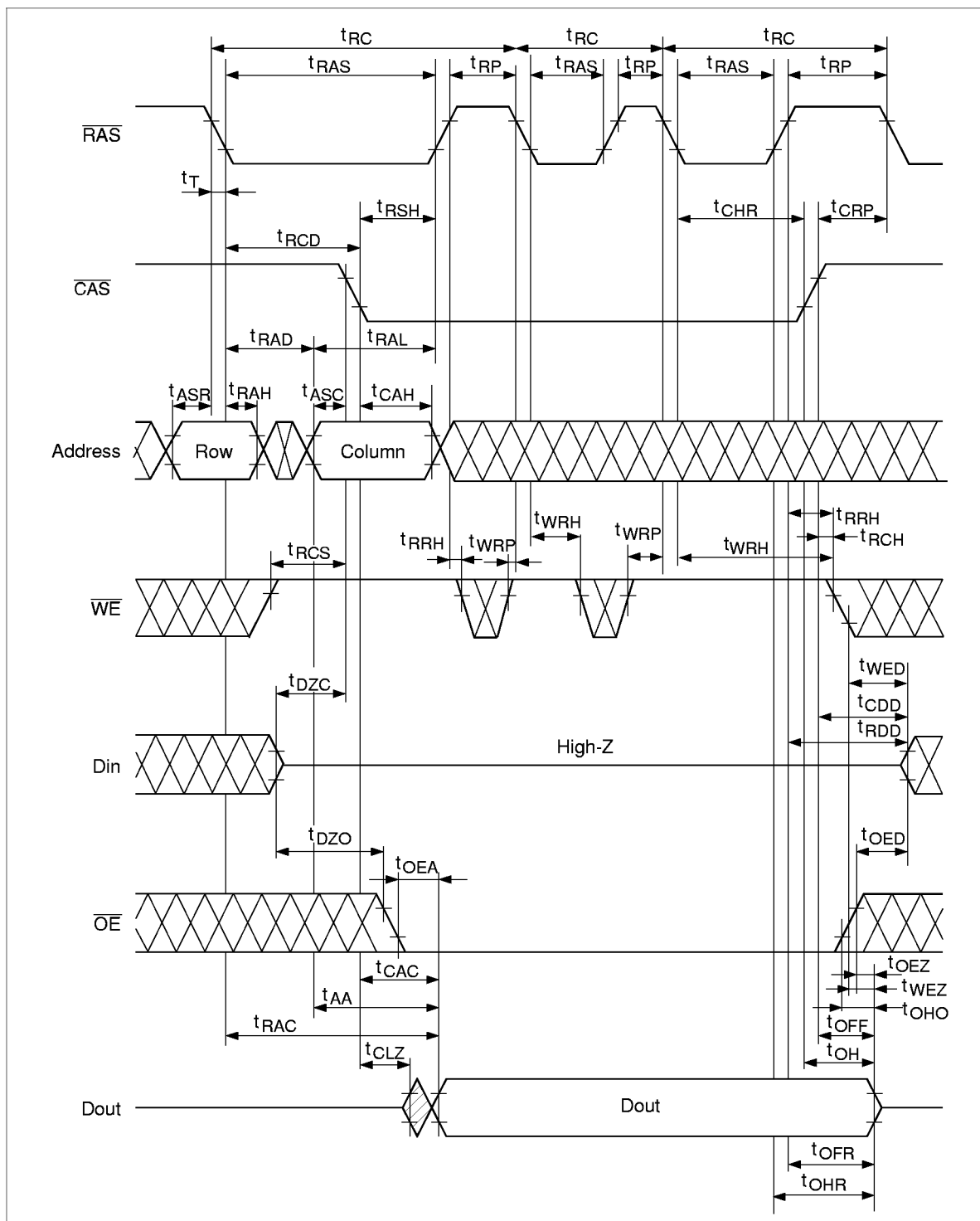


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$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

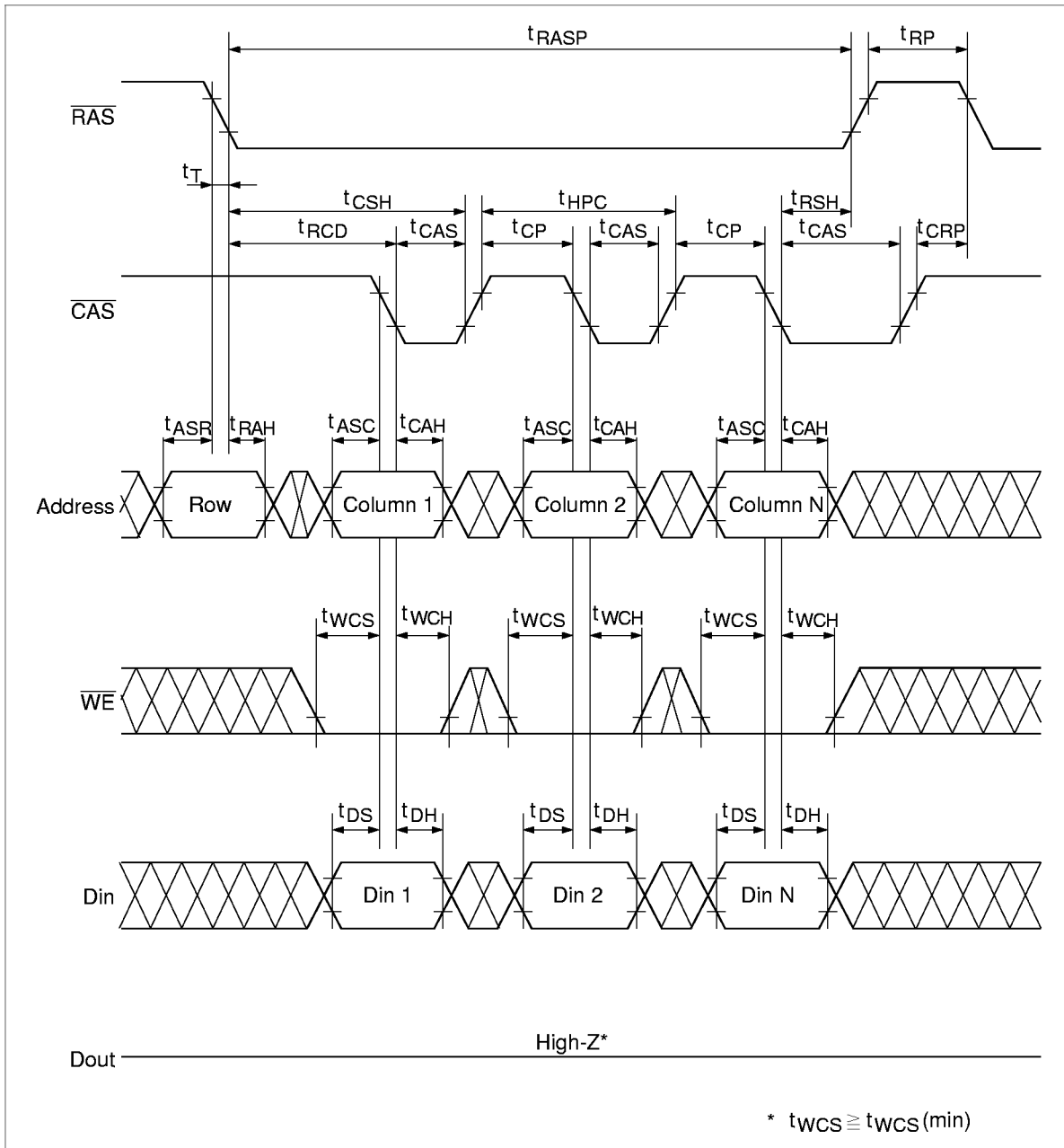


Hidden Refresh Cycle



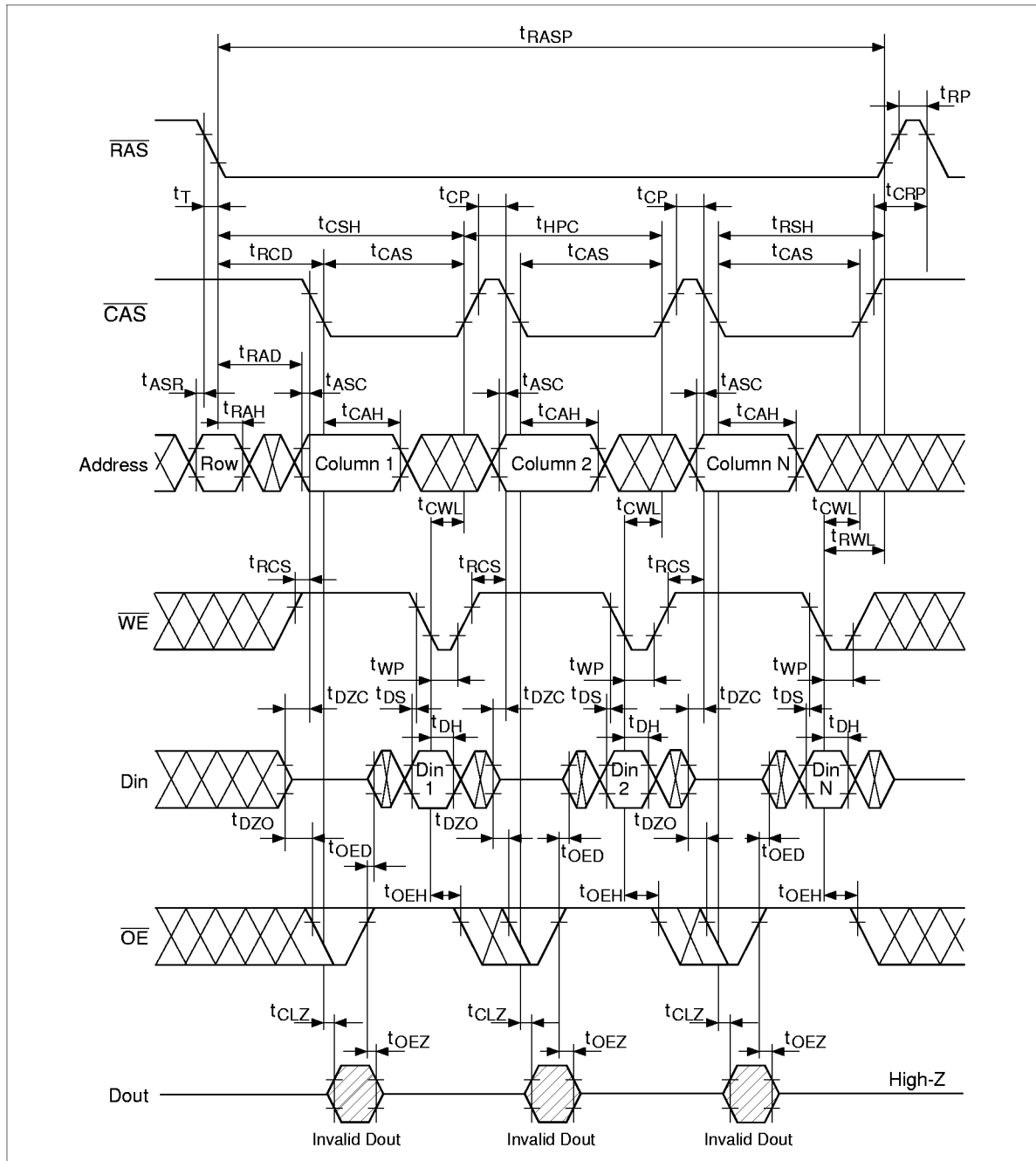
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EDO Page Mode Early Write Cycle



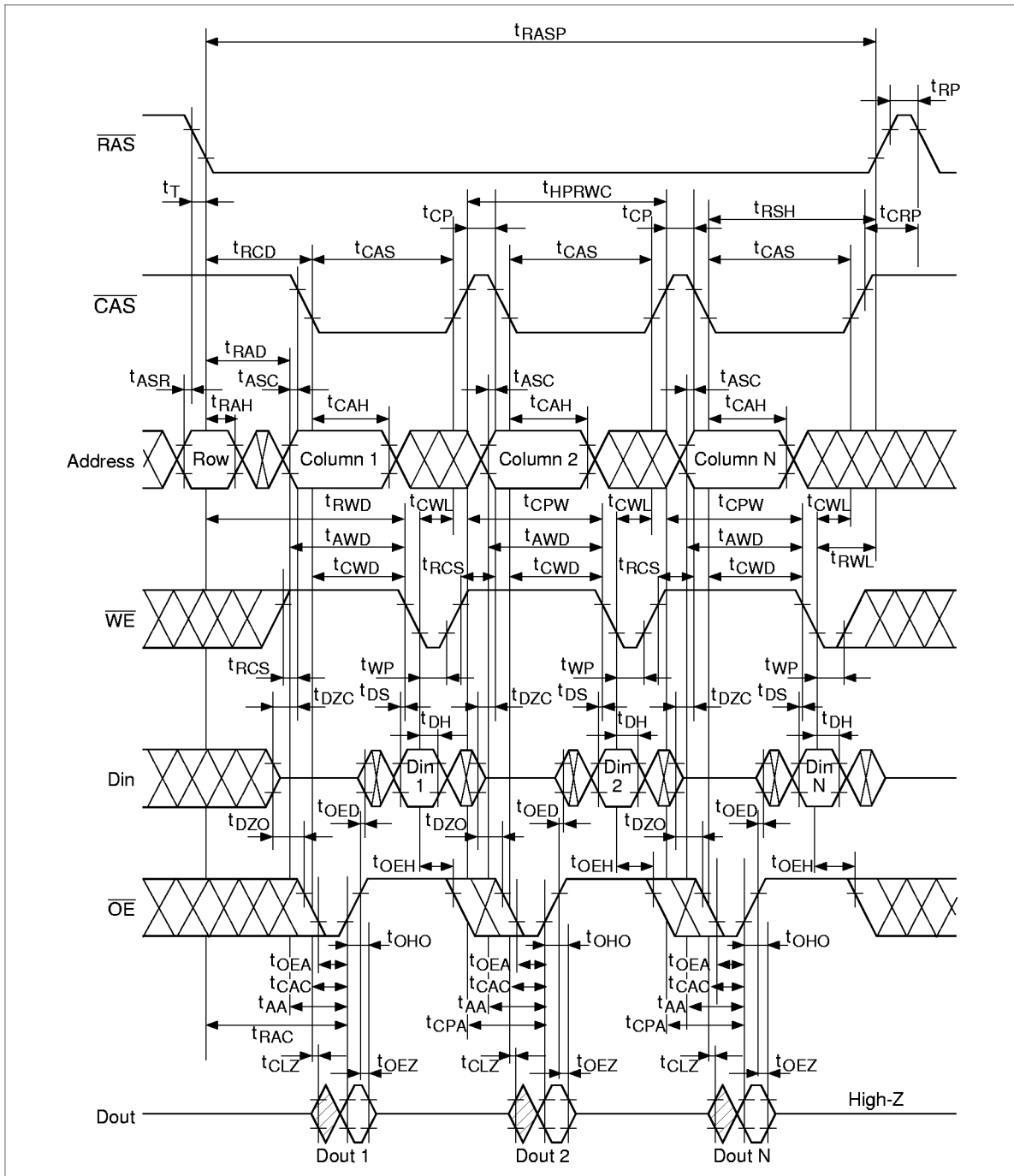
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EDO Page Mode Delayed Write Cycle*18



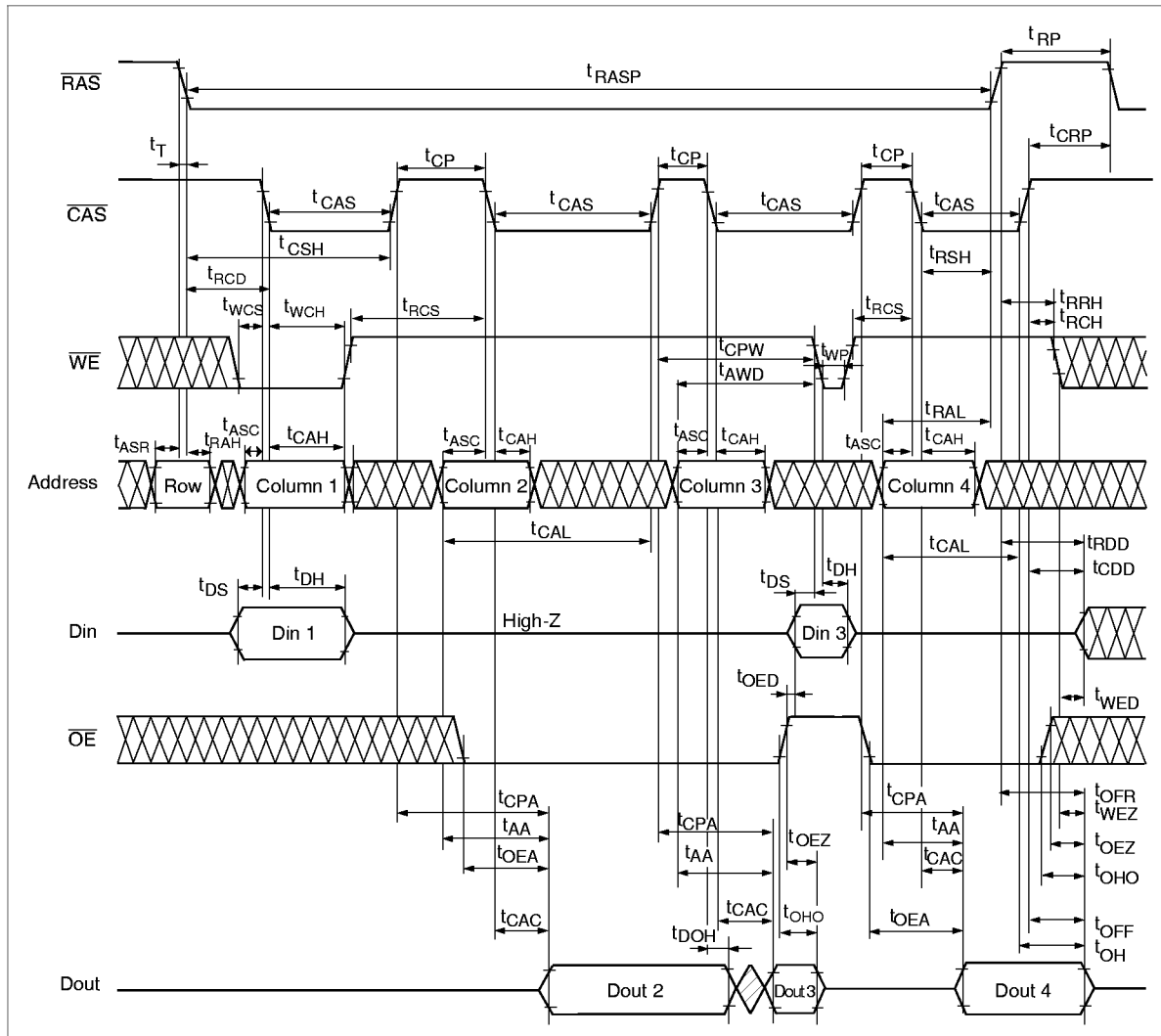
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EDO Page Mode Read-Modify-Write Cycle*18

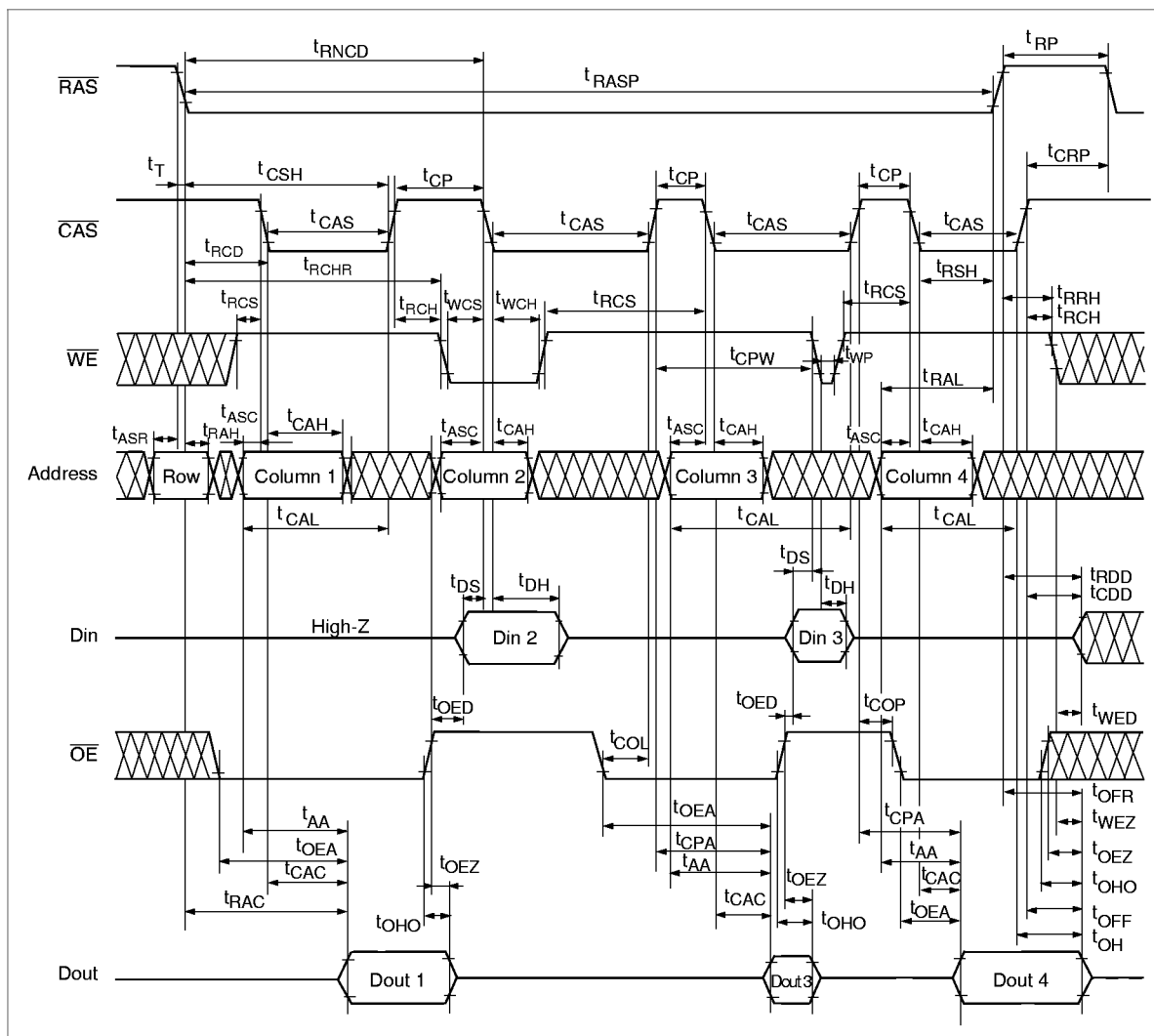


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EDO Page Mode Mix Cycle (1)

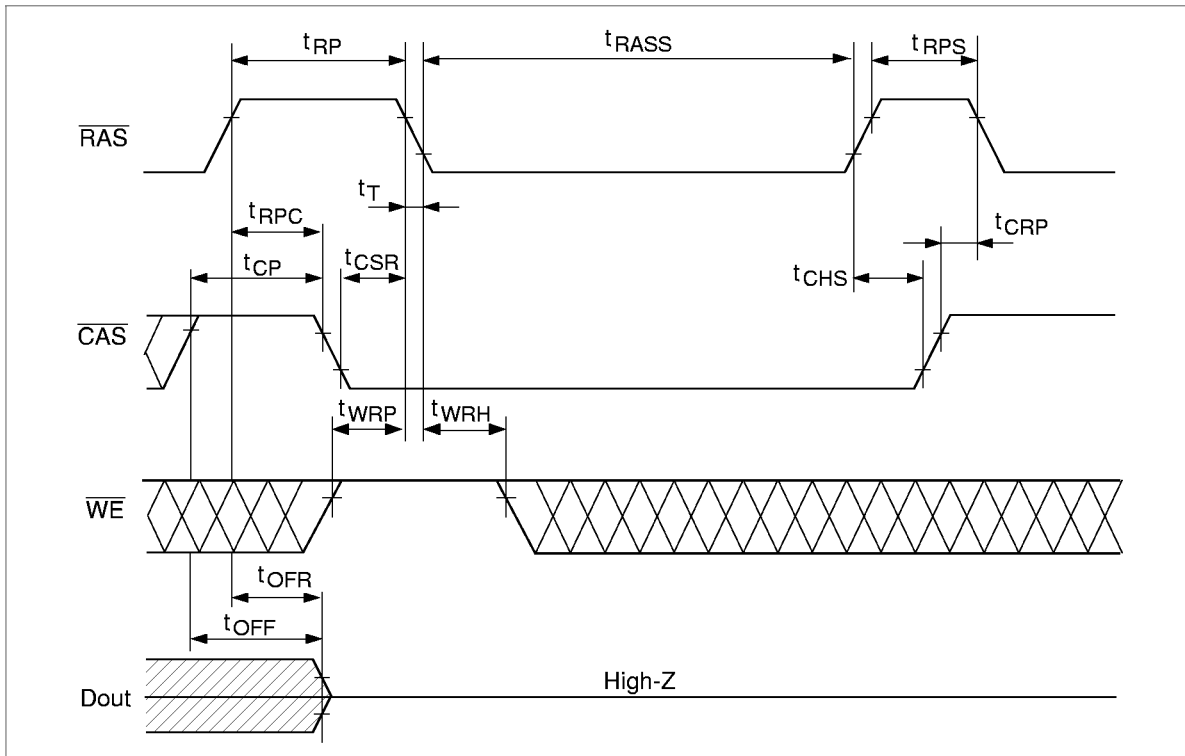


EDO Page Mode Mix Cycle (2)



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Self Refresh Cycle (L-version)* 23, 24, 25, 26



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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.0	Jan. 27, 1997	Initial issue	S. Tsukui	K. Tsuneda
2.0	Jun. 9, 1997	(referred to HM51W16405/HM51W17405 rev 3.0) Change of Serial PD Matrix	S. Tsukui	K. Yoshizaki
3.0	Nov. 1997	Change of Subtitle		